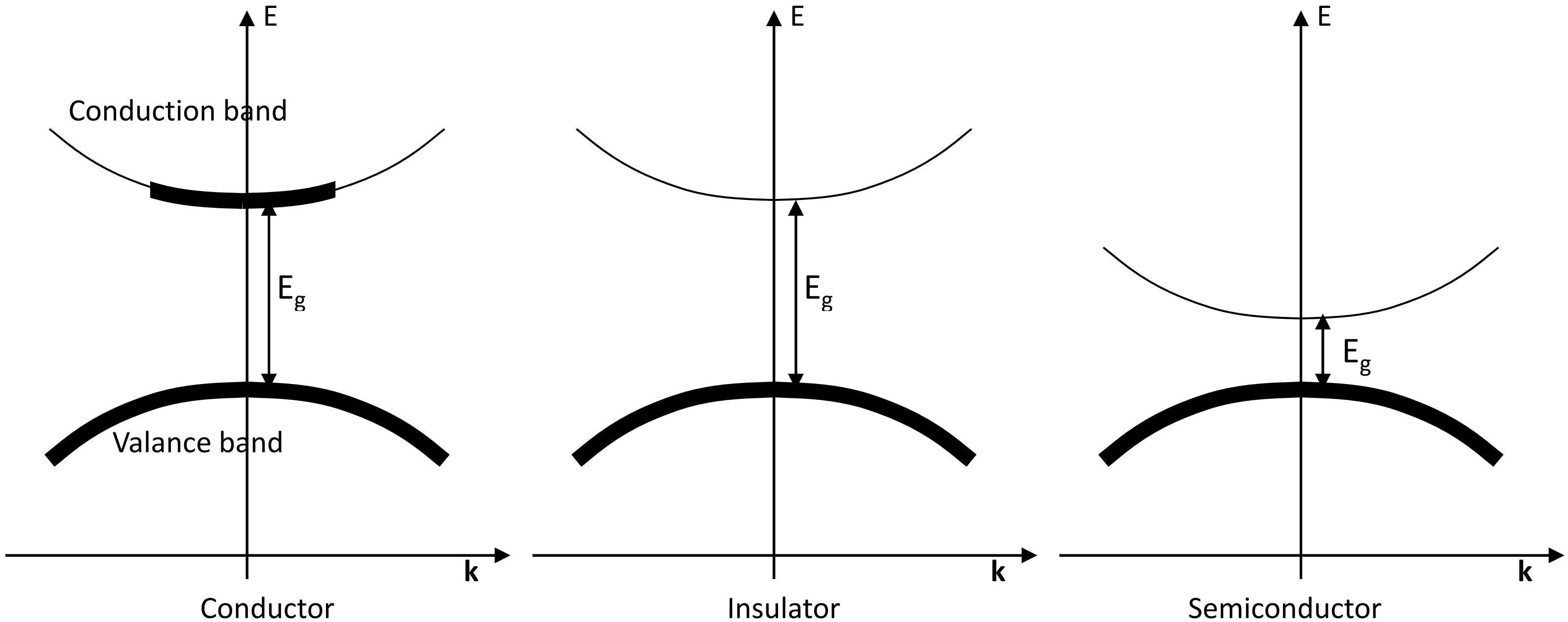
Insulator, semiconductor, and conductor

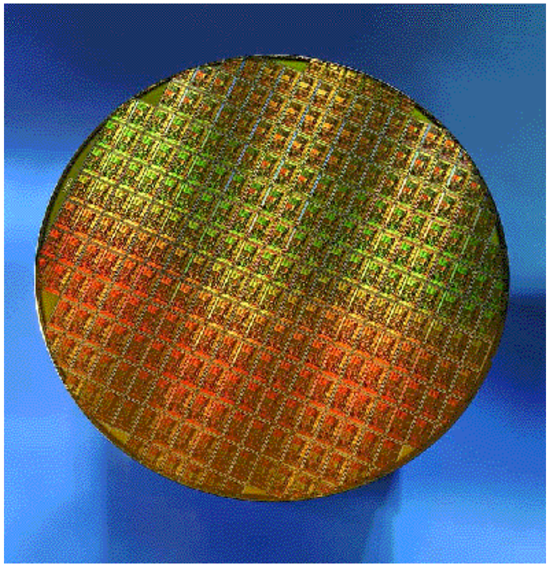


Semiconductor is an insulator with a energy small gap. It conducts slightly at high temperatures because thermal excitations create electrons in the conduction bands, and holes in the valance band.

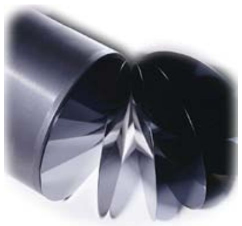
Example

Two common types of semiconductors found in electronic components:

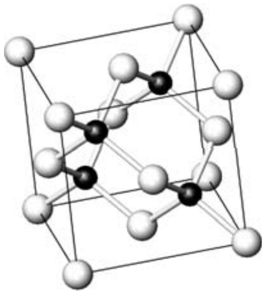
Ge with E_g = 0.66 eV



Si with E_g =1.11 eV

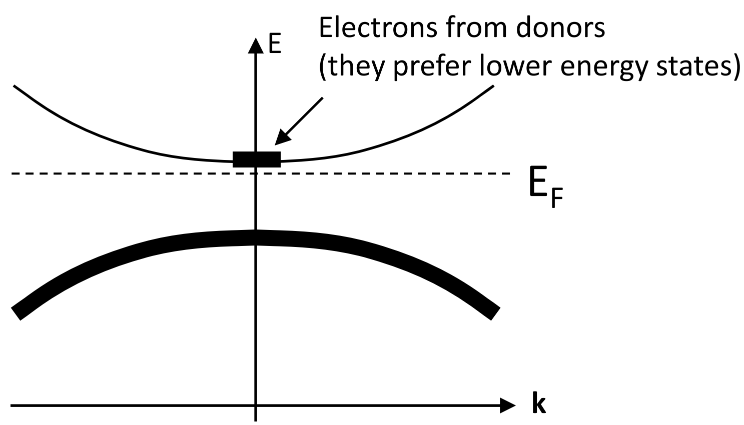


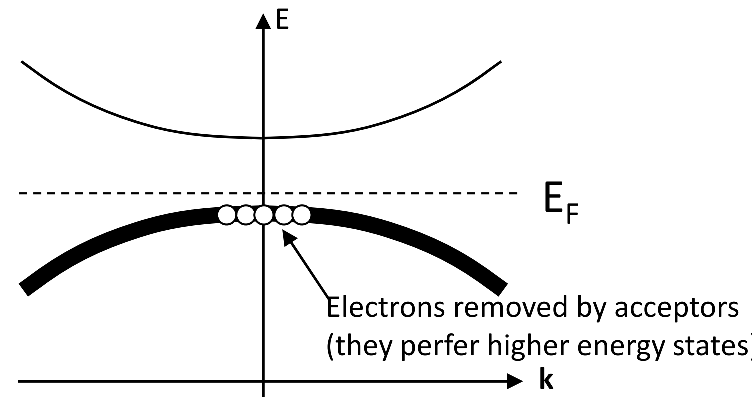
GaAs with E_g =1.43eV



Doped semiconductors

Two types of doped semiconductors:





n-type

Carrier: electrons in conduction band.

Carrier charge: negative

p-type

Carrier: vacancies in valance band (holes).

Carrier charge: positive

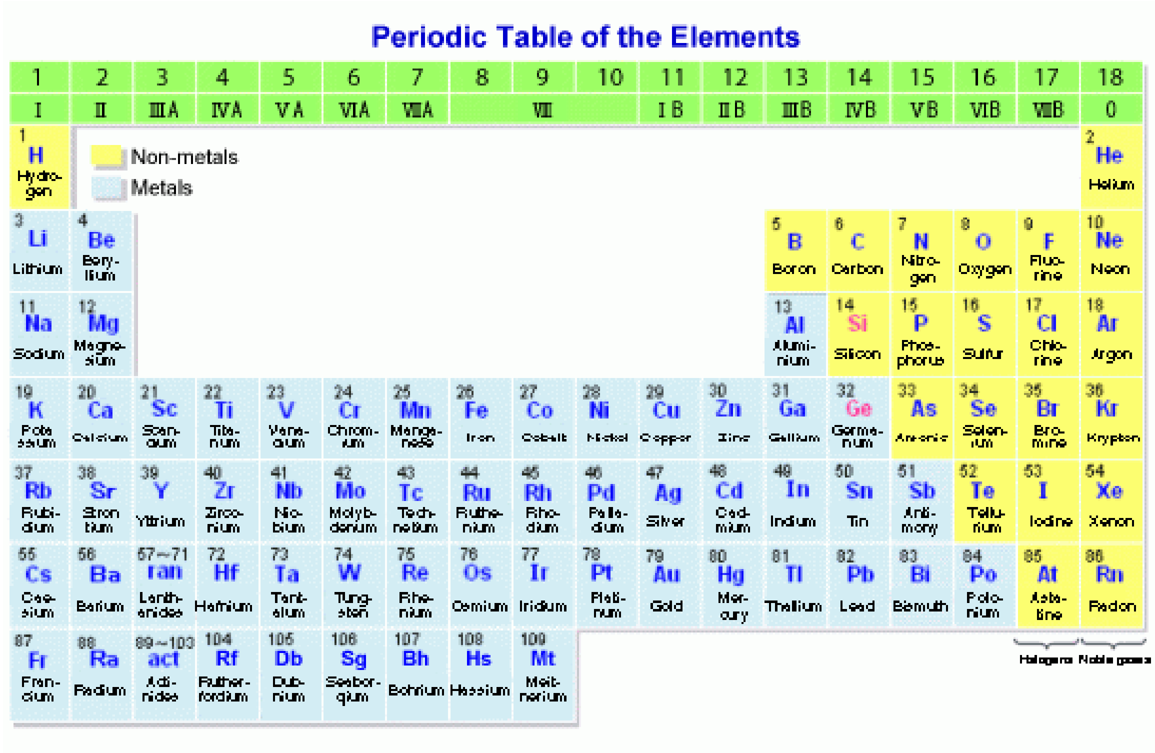
In the same electric field, n-type and p-type carriers move in opposite directions, but they carry current in the same direction!

Example

Si is in group IV.

If it is doped with B (group III element), B will accept electrons from Si and make Si becomes a p-type semiconductor.

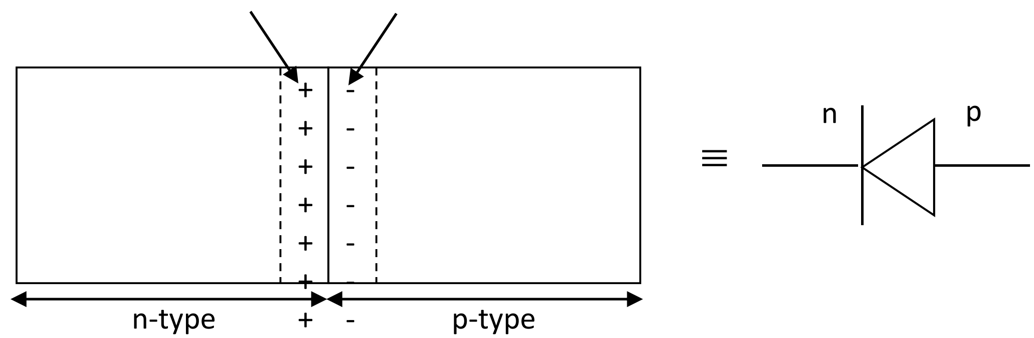
If it is doped with P (group V element), P will donate electrons to Si and make Si becomes an n-type semiconductor.



Joining n- and p- type semiconductors together – Diode I

Positive charges formed by:
(i) positive donors left by electrons migrated to p-side.
(ii) holes migrated from the p-side.

Negative charges formed by:
(i) negative acceptors left by electrons migrated to p-side.
(ii) electrons migrated from the n-side.

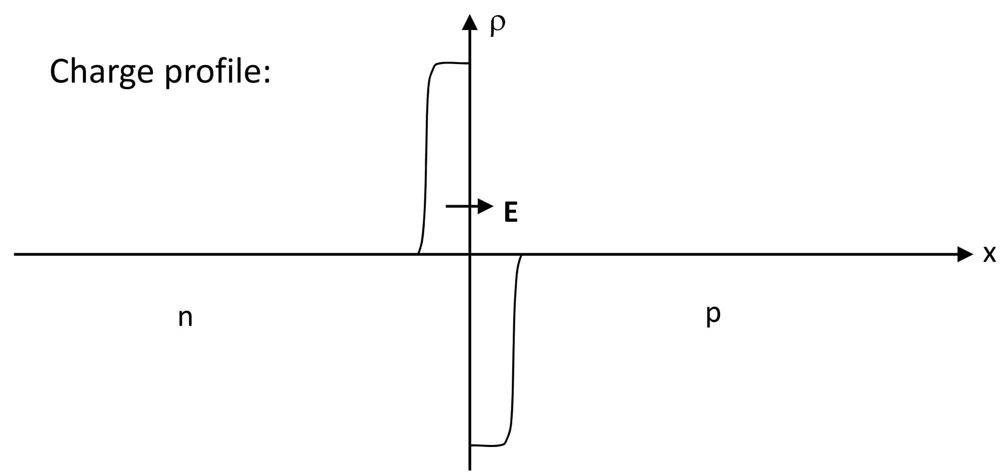


Notes:

1. Carriers of opposite sign do not recombine easily because they live in two different bands.

2. Carriers cannot migrate further because of Coulomb attraction and a depletion layer is formed at the interface.

Charge profile:



Example

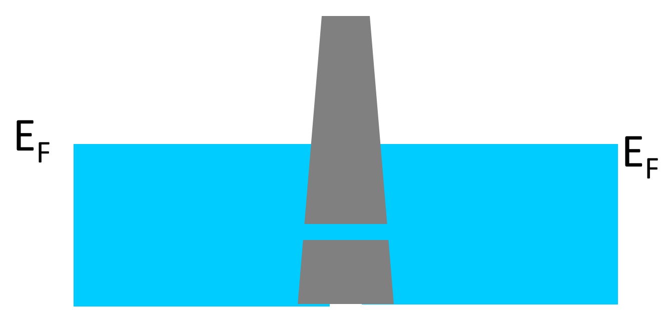
When will the migration stop?

The Fermi level of an n-type semiconductor is closer to the conduction band. The Fermi level of a p-type semiconductor is closer to the valance band.

When the n-type semiconductor touch the p-type semiconductor, the Fermi levels at the two sides are not aligned and the charge carrier will flow from one side to the other. As this happens, the Fermi level at the n-side will fall and the Fermi level at the p-side will rise.

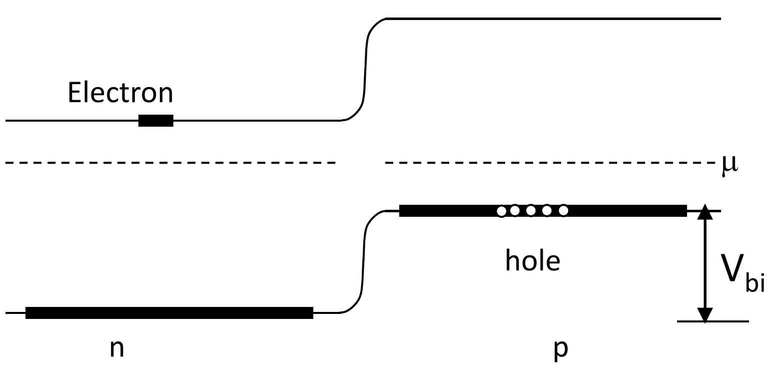
When the Fermi levels at the two sides are aligned, the carrier flow will become equilibrium and the migration will stop.

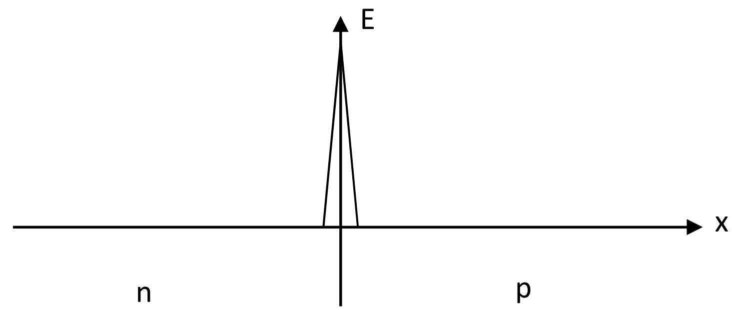
Think of water flow:



Joining n- and p- type semiconductors together – Diode II

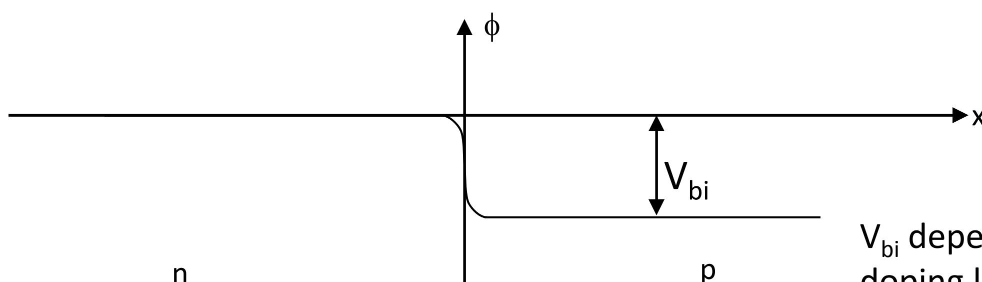
What happen when the energy bands:





$$E = -\frac{d\phi}{dx}$$

Potential at the depletion layer prevents electrons flowing from left to right, and holes from right to left:



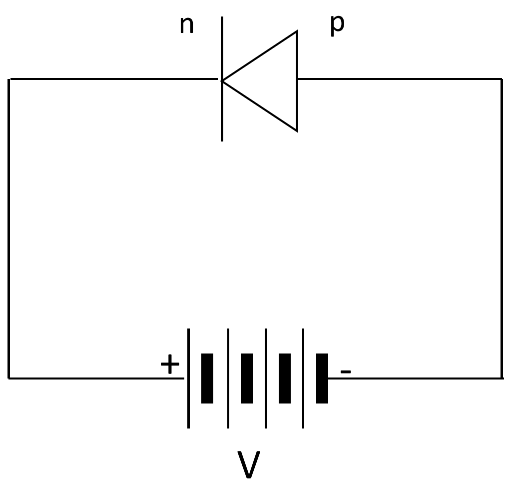
V_{bi} depends on the gap Eg, and doping levels of the semi conductor.

Example (important)

V_{bi} for most diodes equal to 0.6 eV.

Reverse bias

Reverse bias is the condition when you connect a positive potential to the n-side and negative potential to the p-side of a diode:

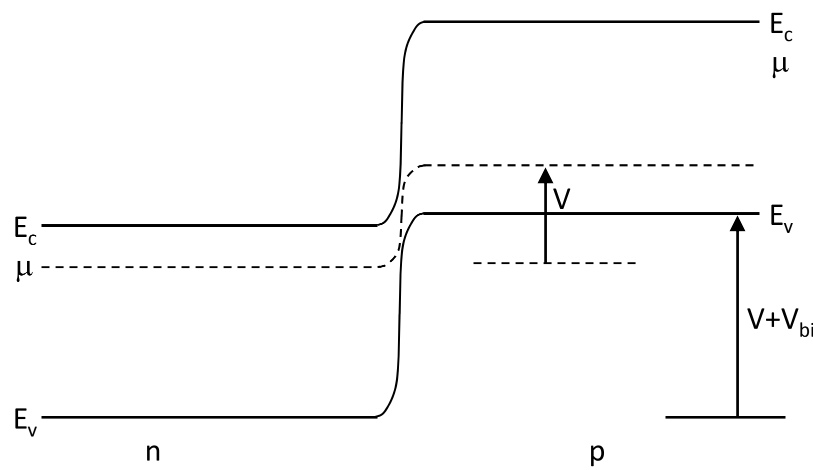


There is no current flowing through the junctions when the diode is reverse biased. Note that most of the external voltage V is "consumed" across the depletion layer, but not at other parts of the diode.

Charge density: The external voltage will push electrons towards right and holes towards left. More recombination occurs and more static charges are resulted. The depletion layer will grow thicker.

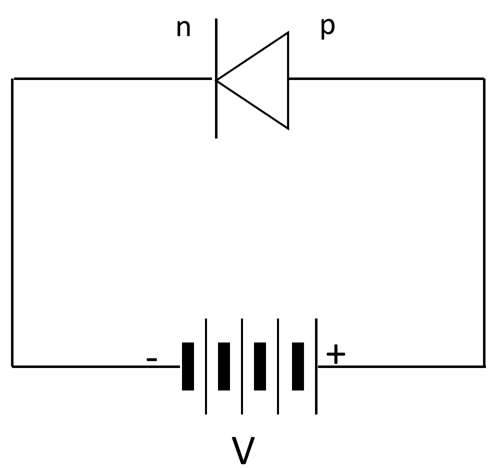
Electric potential: the potential step across the depletion layer will increase from Vbi to V+ V_{bi}.

The external potential add an electric field in the *same* direction of the intrinsic field inside the depletion layer. Hence the electric field in the depletion layer will become stronger, further preventing electrons and holes traveling to the opposite side.



Forward bias

Forward bias is the condition when you connect a positive potential to the p-side and negative potential to the n-side of a diode:

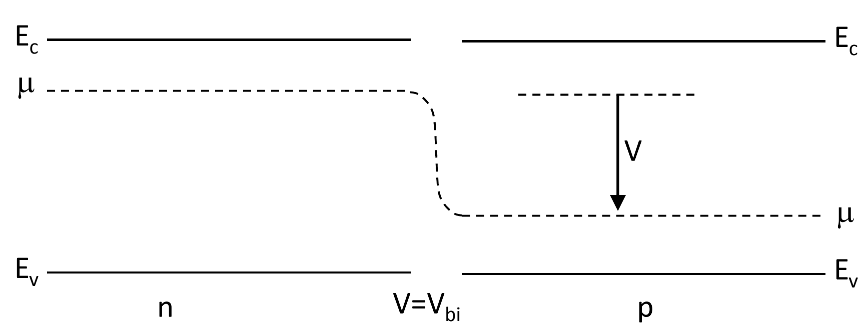


There is no current flowing through the junctions when the diode is reverse biased. Note that most of the external voltage V is "consumed" across the depletion layer, but not at other parts of the diode.

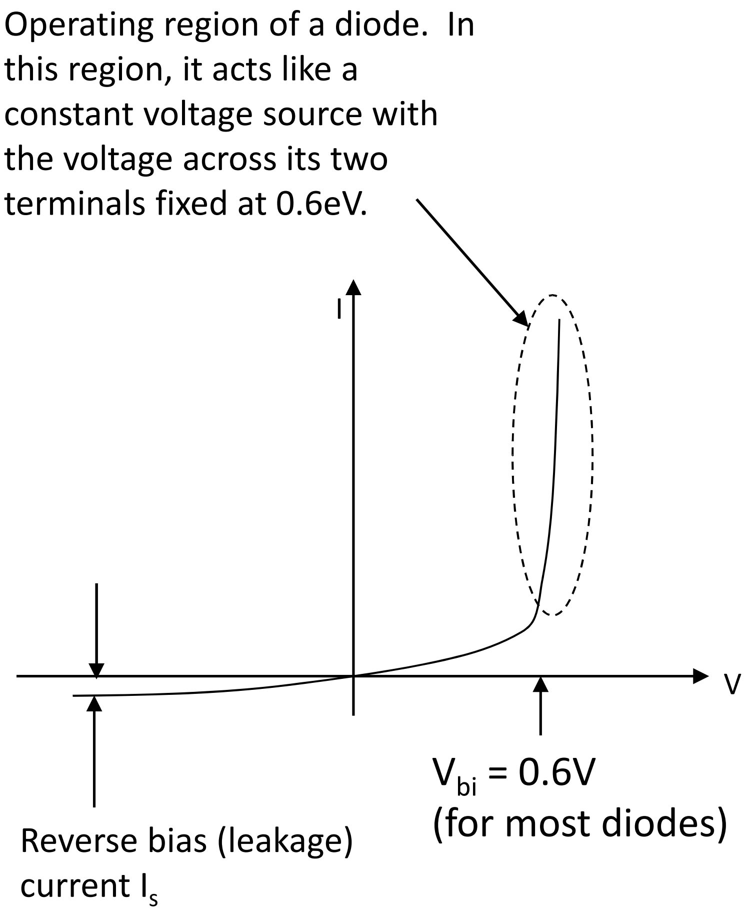
Charge density: The external voltage will remove electrons and holes from the depletion layer. The depletion layer will become thinner.

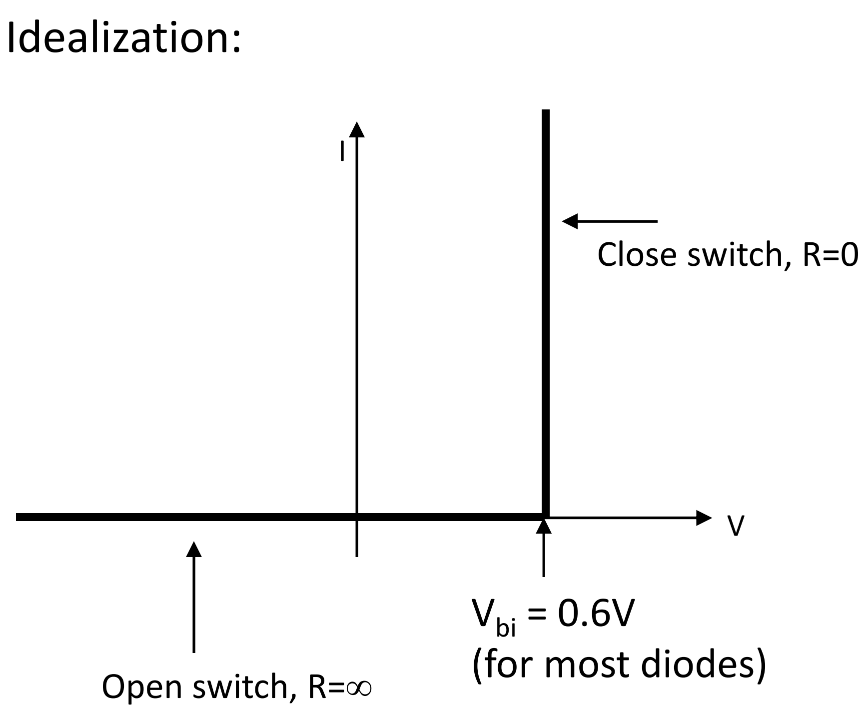
Electric potential: the potential step across the depletion layer will decrease from Vbi to V- Vbi. *When V is larger than Vbi, the barrier is removed and electrons and holes can move freely across the junction.*

The external potential add an electric field in the *same* direction of the intrinsic field inside the depletion layer. Hence the electric field in the depletion layer will become stronger, further preventing electrons and holes traveling to the opposite side.



Characteristics of a diode

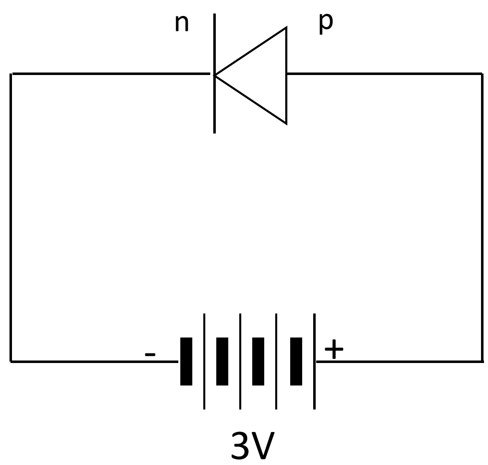


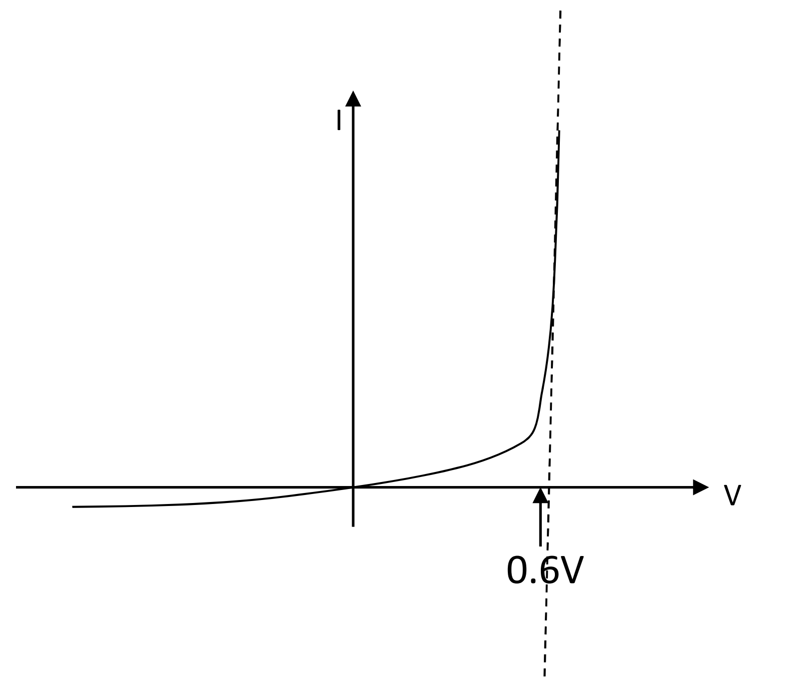


$$I = I_s\left[e^{eV/k_BT} - 1\right]$$

Example (important)

If you do this,



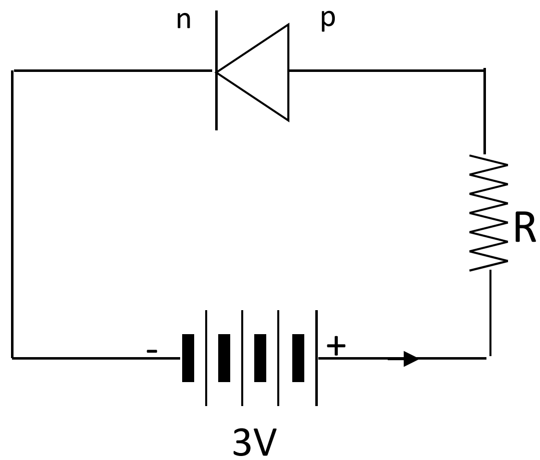


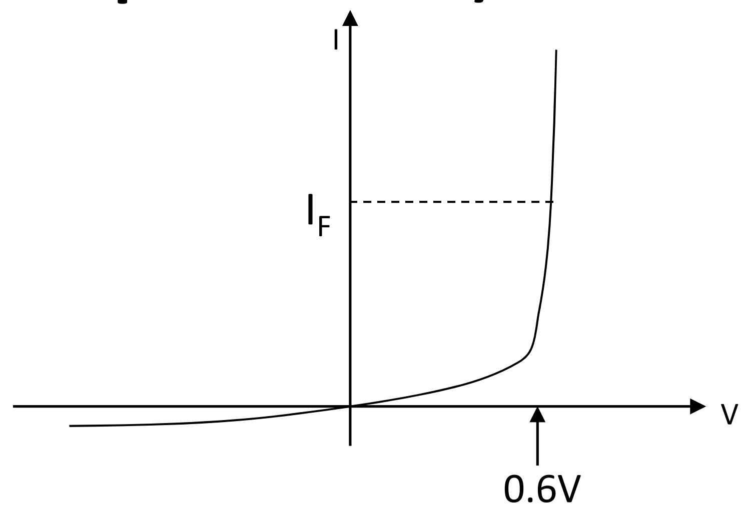
you will burn out the diode easily because 3V>>0.6V. If the diode survives, it is because the power supply has a large output impedance.

$$\frac{1}{\text{slope}} = \text{“resistance” of diode}$$

Example (important)

Proper way to do it:





1. Look up the forward bias current from manual of the diode, say, 10mA for this example. This is the current I you want to maintain in the circuit loop.

2. Apply Ohm's Law (or Kirchoff's voltage rule), *assuming a voltage drop of 0.6V across the diode*:

$$3 = 0.6 + (10\times10^{-3})R \Rightarrow (10\times10^{-3})R = 2.4$$

$$\Rightarrow R = 240\Omega$$

If I_F is not given, you can make a guess from quantities like maximum forward current etc.