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Muon g-2 Note No. 207

Title: **A Deadtimeless Multihit TDC for the New g-2 Experiment**

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A DEADTIMELESS MULTIHIT TDC FOR THE NEW G-2 EXPERIMENT

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Abstract

A deadtimeless, 1ns resolution Multi-hit Time-to-Digital Converter (MTDC) has been developed for the new g-2 experiment (E821) at Brookhaven National Laboratory. The module is based upon a GaAs ASIC developed at Boston University for the DUMAND project. This 27 channel device is packaged as a 9U, triple-wide VME module. Both NIM and differential ECL inputs are provided, selectable in groups of four. Inputs can be configured to record both leading and trailing edges (for time over threshold) or leading edge only. Enable, Disable, and Clear inputs are provided for memory management. The standard memory depth is 128k transitions, with provision to allow expansion to 1M transitions. Multiple levels of buffering and intrinsic zero-suppression make this device ideal for recording bursts of events with 1ns resolution.

Introduction

The new muon g-2 experiment (AGS 821) involves the construction of a unique, high precision storage ring for 3 $\frac{Gev}{c}$ muons. The goal in precision is a measurement of the muon g-2 value or $a_\mu(= \frac{g-2}{2})$ to 0.35 ppm, which would be an improvement by a factor of 20 compared to the present experimental accuracy of 7.3 ppm from a previous CERN experiment.

The heart of the g-2 measurement is the precise, rate-independent measurement of muon decay electron arrival times. It is also necessary to measure the electron energies with modest resolution in order to select high-energy electrons, which have the highest asymmetry. To meet these requirements a 400MHz Waveform Digitizer (for amplitude measurement - not discussed further here) and an 800MHz Multihit TDC (MTDC) system have been designed and constructed by the Electronics Design Facility at Boston University. The details of this time digitizer are the focus of this document.

MTDC Specification

The MTDCs (also called "digitrons") record the arrival times of decay electrons passing through scintillation counters. Light from the scintillation counters is converted with a PMT to an electrical pulse. These pulses are then discriminated and measured with the MTDC in both leading-edge and time-over-threshold (for pile-up rejection) modes. Shown in Table 1 are these two classes of input channels, with different requirements. The channels have thus been named "precision" and "non-precision" to signify that extremely low systematic error is required for the former, whereas the systematic error requirement is less stringent for the "non-precision" channels.

Basic functional requirements of the MTDCs are:

- Record time of rising and falling edges on non-precision inputs, and leading edge only on precision inputs.
- Provide data storage available for readout over VME bus.
- Provide sufficient control of features via VME bus I/O, and support at least A24, D16, and D32 VME access. Also, VME bus block transfers will be available.
- External ENABLE, DISABLE, VETO, and CLEAR inputs.

*With acknowledgements to the muon g-2 (BNL E-821) and DUMAND (Deep Underwater Muon And Neutrino Detector) Collaborations

precision channels		notes
number of channels	12	
least count	5 ns	
systematic error	$\leq$ 20 ps	1
electrical	100 Ω diff ECL	2
non-precision channels		
number of channels	12	
least count	$\leq$ 1.25ns	3
systematic error	$\leq$ 250 ps	
electrical	50 Ω NIM fast logic	
general		
instantaneous rate	$\leq$ 400 MHz	3
average rate	$\leq$ 50 MHz	4
on-board storage	128K transitions	5

Notes:

1. Maximum permissible timing shift caused by external factors (data, rate) over approximately 1 ms long recording period.
2. Compatible with LeCroy ECLine standard, i.e. 0.1 inch spacing header connectors, 100 Ω balanced input.
3. This is implied by the least-count of 1.25ns; i.e. 400 MHz clock, input sampled on both clock edges.
4. Sum of rates on all inputs. Estimated using *Monte Carlo* queueing loss simulation[4].
5. Depth based on $\approx$ 92K transitions (rounded up) using above *Monte Carlo* queueing loss simulation.

Table 1: MTDC (digitron) specifications.

The VME compatible module is based on a new GaAs ASIC developed for the DUMAND[1] experiment at Boston University. This ASIC is implemented in a Vitesse VGFX200K gate array[2] customized as described in more detail elsewhere[3].

For the high-precision channels, we plan to use a separate synchronizer ("de-randomizer") circuit to achieve the required low systematic errors. The output of this synchronizer circuit is then recorded with the same module (the MTDC) as the non-precision channels.

MTDC Module

General Description

The MTDC is a 9U Eurocard module, 400mm in depth. The module is triple width (1.2"), in order to accommodate the ASIC heat-sink in a single VME package. A block diagram of the MTDC is shown in Figure 1. Table 2 lists the module inputs.

Digitizer ASIC

At the heart of the MTDC is an ASIC developed for the DUMAND II experiment.[5] This device is shown in schematic form in Figure 2. Information flows from right to left and the function of each block is described below.

Data Inputs. The PMT signals are received on the MTDC in both differential ECL and NIM form. The NIM signals are converted to differential ECL and the differential ECL signal simply buffered before going into the ASIC. All 27 ASIC inputs are encoded identically, although there is some variation in signal definition.

Edge Detector. This block assigns the asynchronous signals coming from the PMTs to discrete time bins. To avoid possible systematic errors in the time binning, the precision channels go through an external "de-randomizer" module, which then unambiguously assigns a PMT hits to the correct, unbiased time bin. The edge detector also provides zero-suppression by triggering the circuit only when a transition occurs on an input. Inputs are sampled on both rising and falling edges of the clock, using separate portions of the circuit.

Time Stamp. A ten bit time stamp is recorded for each clock interval ($1.25ns$) containing valid data. The ten-bit time will roll over every ($1,024 \times 1.25ns = 1.28\mu s$), and a special word is inserted in the data stream when this occurs. This word is used outside the ASIC to increment an extension counter, allowing this 10-bit time to be arbitrarily extended. This will be discussed in greater detail below.

First FIFOs and Tag FIFO. These blocks provide buffering for bursts of input data. The priority encoder services one channel per $2.5ns$ clock cycle, which implies a need for queuing if transitions arrive in bursts. For DUMAND, the expected time distribution of input data led to the decision to put 10 words worth of buffering in

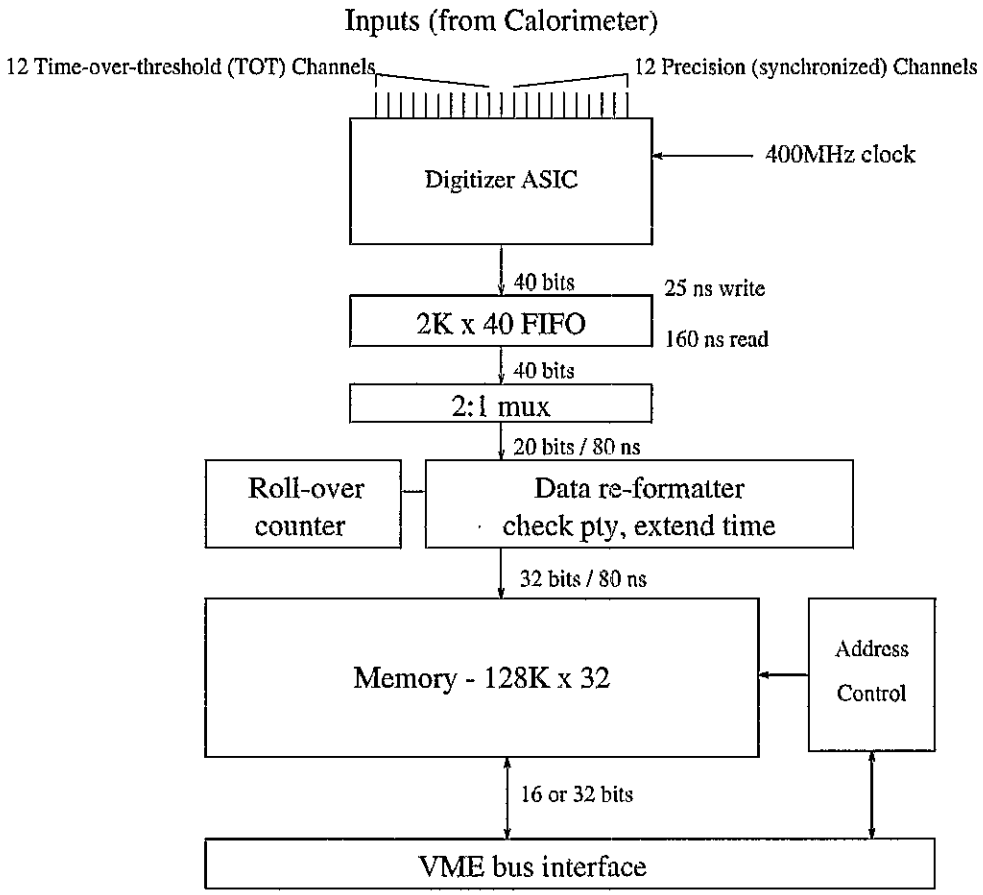


Figure 1: A block diagram of the MTDC. Data flows from the inputs at the top into RAM, from which it is accessable from the VME bus at the bottom.

front of the priority encoder. For g-2 the adequacy of this buffering has been simulated and seems sufficient. Two separate FIFOs ("Odd" and "Even") store data recorded on rising and falling clock edges. Since two FIFOs may each contain a different number of words, a mechanism is required for reading them in time-order. The tag fifo provides this mechanism.

Priority Encoder. This block identifies those channels where a transition took place. If there is more than one transition within the same $1.25ns$, the priority encoder emits a separate word for each transition, in order from low to high channel numbers. Since this is a true priority encoder, no scanning of empty bit locations is required, and each transition requires only $2.5ns$ to encode.

Second FIFO. The priority encoder generates data in bursts, and the second fifo buffers data until it is read off chip. The depth of 100 transitions was set by considerations specific to the DUMAND application, but appears more than adequate for g-2. Data is read from the ASIC using a simple two-line handshake mechanism at a rate of 40MHz.

Data Format

The output of the ASIC is a 40-bit word containing two transitions. It is stored in memory in a format more convenient to the g-2 DAQ system, shown in Figure 3. In particular, the 10-bit time is extended to a 20-bit time with inclusion of the time from the extension counter. The extension counter is incremented by each roll-over word that is read out from the ASIC.

The MTDC produces one 32-bit word per input transition, giving channel number, time and an up/down bit which tells whether the transition was a leading or trailing edge. The time is measured by a free-running counter inside the digitizer ASIC. The time is in units of one-half clock cycle, so for the 400MHz clock rate the least count is 1.25ns.

Status and Control Functions

The MTDC is controlled and read out via the VME bus. Table 3 lists the VME bus functions. The address space

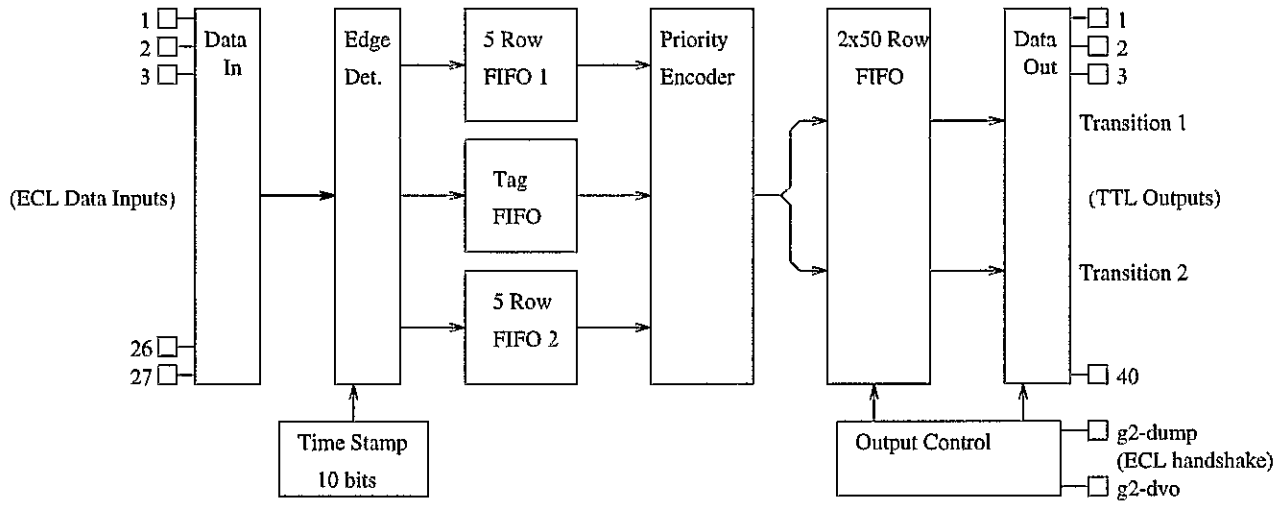
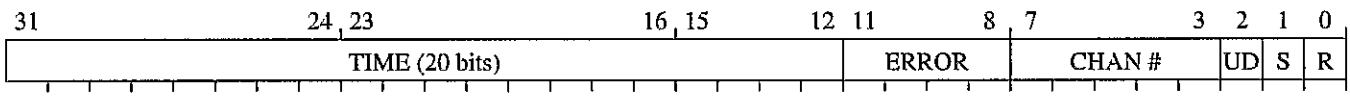


Figure 2: A block diagram of the MTDC Digitizer ASIC.



R	Reserved: not currently used
S	Synchronization error
UD	Up/down bit: 0 - leading edge; 1 - trailing edge
CHAN #	1..12 Precision inputs 13..24 Non-precision inputs 25 Reset 26 ENABLE 27 DISABLE 28 20-bit time (mili-second) roll-over word
ERROR	bit 8 - 5-row FIFO overflow (OVFL1) bit 9 - 50-row FIFO overflow (OVFL2) bit 10 - External FIFO overflow (FFOVFL) bit 11 - parity error (PTYERR)
TIME	bits 12..21 - 10-bit ASIC time bits 22..31 - 10-bit Extended time

Figure 3: MTDC output data format.

inputs		notes
Synchronizer inputs	(12) ECL diff 100Ω	
TOT inputs	(12) NIM standard	
clock	200MHz sine	1
ENABLE, DISABLE	NIM or diff. ECL	2
VETO	NIM	3
CLEAR	NIM	4

Notes:

1. 200MHz sine provided by common clock distribution module and frequency doubled on the MTDC. The ASIC will run up to 500MHz, however 400MHz has been deemed adequate for g-2.
2. These start and stop recording, and each records a unique time stamp in the data stream.
3. Disables inputs when active.
4. Resets module: disables recording, empties memory, and resets word count to zero. Note: this does not alter state of the control register.

Table 2: MTDC input configuration in the g-2 baseline.

is mapped with PALs to allow optimum use of address space for the amount of memory installed.

Data Memory

The module provides memory for 128K transitions. This memory is filled with data from the digitizer chip, at increasing addresses beginning at the address specified by the WADDR register. The memory is also accessible directly from the VME bus, and occupies 512K byte addresses. The memory may be read or written from the VME bus, although writing is disabled when module inputs are enabled (as indicated by the ENA_ST status bit). Simplistically, writing to memory is enabled by receipt of ENABLE and disabled by receipt of DISABLE. The Enable signal also resets the extension counter to zero.

Crate, Power and Cooling

As described above, the module is packaged as a triple-wide x 9U high VME module. Power supply requirements are listed in Table 4 below.

The ASIC dissipates about 15 watts, and requires a modest heatsink.

Data Rates

A queueing simulation was performed to ensure that the expected data rates in g-2 would not exceed the buffer capacities in the MTDC. In the g-2 experiment, muons are injected into the storage ring in bunches, resulting in initial data rates which may approach 10MHz in each calorimeter. The rate decays exponentially after injection as $e^{-t/64}\mu s$. A *Monte Carlo* simulation was run, which generated simulated decay electrons, passed them through a calorimeter model, and produced simulated output pulses. A model of the MTDC ASIC and PCB was written in 'C', and the data was fed through it. The loss in each FIFO was monitored. The simulation showed that the most significant bottleneck occurred at the output of the ASIC. Figure 4 shows a plot of the overflow rate vs readout speed at the ASIC output. Based on these results, a readout period of 25ns was chosen.

Testing

Test Bench

A test station was assembled for the MTDC prototype system and one configuration of which is shown in Figure 5. Given the space limitations of this paper, only a subset of the testing procedures and results shall be presented here. The configuration shown consists of four main pieces and some signal level/cable converters. The Clock Generator produces a very stable reference sine-wave for the clocked components of the system. The "Gimzo" then uses this clock to produce a series of computer-adjustable pulses with respect to the clock phase. The Synchronizer then uses the clock out from the "Gizmo" to quantize the output pulses to 5ns time-bins. Finally, these "de-randomized" pulses are sent into the MTDC for recording.

Clock Generator. This is a custom NIM module with a stable 200MHz oscillator and a frequency doubler. The 200MHz is used to drive the "Gizmo" and the 400MHz is used to run the MTDC.

The Rate Test "Gizmo". The g-2 rate test fixture (a/k/a the "Gizmo"), incorporates a variable delay element implemented using Motorola 10E195 and 10E196 delay ICs. A delay from $0 - 6700ps$ in steps of $17.5ps$ may be

name	*segment*	*function*	*description*	*notes*
control register	Byte 0	ASIC Control	Reset, Roll-over word disable	1
	Byte 1	ASIC Test	Serial-input test-pattern generator	2
	Byte 2	MTDC Config	Run/interrupt mode control	
	Byte 3	DAQ Control	Initiate/halt data acquisition	
status register	Byte 0	ASIC Config	ASIC functional status	1
	Byte 1	MTDC DAQ status	acquisition/error status	
	Byte 2	NIM/ECL select	NIM/ECL input used, by 4 channels	
	Byte 3	Edge/TOT select	Leading Edge or both, by 4 channels	
	Byte 4	RW Value	ASIC chan # used as "Roll-over word"	3
	Byte 5	Stop Value	ASIC chan # used "Event Stop"	3
	Bytes 6,7	MRWD time/channel	msec roll-over word time/channel	4
	Bytes 8-11	Next/Interrupt Addr	Next RAM write/Interrupt Addresses	5

Notes:

1. Control register is read/write and Status register is read only.
2. Serial data and clock to load test pattern. Separate trigger input to allow re-triggering.
3. Allows flexibility in defining roll-over/stop word channels in the data stream.
4. Extension counter value and channel which are injected into the data stream when the 20-bit time rolls over, approximately every 1 *ms*
5. Address at which next RAM write from ASIC will occur in bits 0..19, and VME interrupt code in bits 24..31.

Table 3: MTDC Control and Status registers.

Voltage	VCC (+5V)	VEE (-5V)	VTT (-2V)	+24V	-12V
Current	5.0A	2.5A	7.5A	60mA	60mA
Power	25W	12.5W	15W	960mW	300mW

Table 4: MTDC power specifications

programmed digitally. In addition, a "fine tune" adjustment is available, which provides an additional $0 - 100ps$ delay, which is adjustable in $24fs$ steps (clearly jitter and noise precludes precise delay settings in the sub-ps range). The delay element is programmed via a 3-bit optically-isolated serial interface.

Pulse Synchronizer (De-randomizer). A creation of the Instrumentation Group at Brookhaven National Laboratory, this device is conceptually an ideal D-flip-flop. The details are quite subtle and beyond description here, and tests have shown this device to be quite close to an ideal pulse synchronizer.

MTDC Prototype. A rack-mounted version of a DUMAND digitizer prototype, designed to test the performance of the "g-2 mode" of ASIC readout. The following testing pushed the limits of what might be hoped for from this prototype, since numerous electrical compromises had to be made to allow this to work (e.g. the inputs for DUMAND are fiber-optical receivers and had to be extensively modified to allow processing of fast NIM and ECL input signals). It is anticipated that the performance of the production VME board should be even better.

Test Results

Tests are ongoing and will continue for the forseeable future. The discussion here focusses on three fundamental tests: differential non-linearity, rate dependence, and crosstalk.

Differential Non-Linearity. The differential non-linearity (DNL) testing is based on the random arrival times of $\beta-$ particles emitted from a Strontium-90 radioactive source, as measured with an scintillator and a photomultiplier tube. The tube output is discriminated and either placed directly into the MTDC or alternately run through a data synchronizer ("de-randomizer"). The test is allowed to continue until on the order of 10^{10} events have been recorded. The arrival times are placed by the MTDC into 1.25 ns "bins", or alternately by the de-randomizer into 5ns bins. If there is very small DNL in the system, then each time bin should contain the same number of entries within statistics. Initial results show excellent linearity in the width of the MTDC time bins (less than one part in 10^5), as shown in Figure 6. Note that this is within statistical errors.

Rate Dependence. The MTDC will be used to measure events at up to a 10MHz rate; as such, it is important to assess the dependence of the MTDC on input rate. In this test, the input is the worst case 10MHz (100ns period) burst of programmable lengths up to $100\mu s$. The MTDC system is used to measure the arrival time of a final pulse occurring at $100\mu s$ after the start of the burst. As different burst lengths are used, the test measures any change in the final pulse measurement. Further, a set of pulses that decay exponentially in time over a $640\mu s$ period has been applied to an input channel of the MTDC to simulate the actual decay rate spectrum of E-821. Preliminary indications are that no time boundary shifts $> 20ps$ occur at input rates up to 10MHz.

Crosstalk. This test is designed to assess the amount of crosstalk occurring in the Synchronizer and MTDC circuitry. One channel of the Synchronizer is stimulated with a fixed-width input pulse, which is recorded via the MTDC. Next, a second channel of the de-randomizer is stimulated with the same pulse, but at varying arrival times via cable delay. This second input to the MTDC is not recorded; rather, its effect on the original input channel is measured. The cable delays used range from 1 to 11 ns, enough to allow testing across 2 full time bins of 5ns each. Preliminary results indicate that the crosstalk has no effect on the input signal greater than +/- 7ps, the measured error in the clock boundaries of the system.

Conclusions

The design for the production MTDC has been extensively simulated and the layout completed. The boards are in fabrication as of the writing of this document. Initial testing of the prototype has exceeded expectations for performance and is hoped to be even better for the production module. All specifications that have been tested have been met or exceeded. Further exhaustive testing is expected to proceed over the next 6-9 months to commission this time measurement system for the precision $g-2$ measurement to be performed.

References

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[4] E. Hazen "Queuing Loss Simulation for the g-2 MTDC", EDF Internal Note 94-7. To be published as a g-2 Note.

[5] G.S. Varner *et. al.*, "A New Multihit Digital TDC in a Gallium Arsenide ASIC," Proceedings of the 1993 IEEE Nuclear Science Symposium, Vol. I, 620-624

[6] W. E. Earle, "A Four Channel, 200MHz Waveform Digitizer with a VME bus Interface", Boston University EDF Memo

[7] W. E. Earle, "WFD power requirements", Boston University EDF Memo, Feb 22, 1993

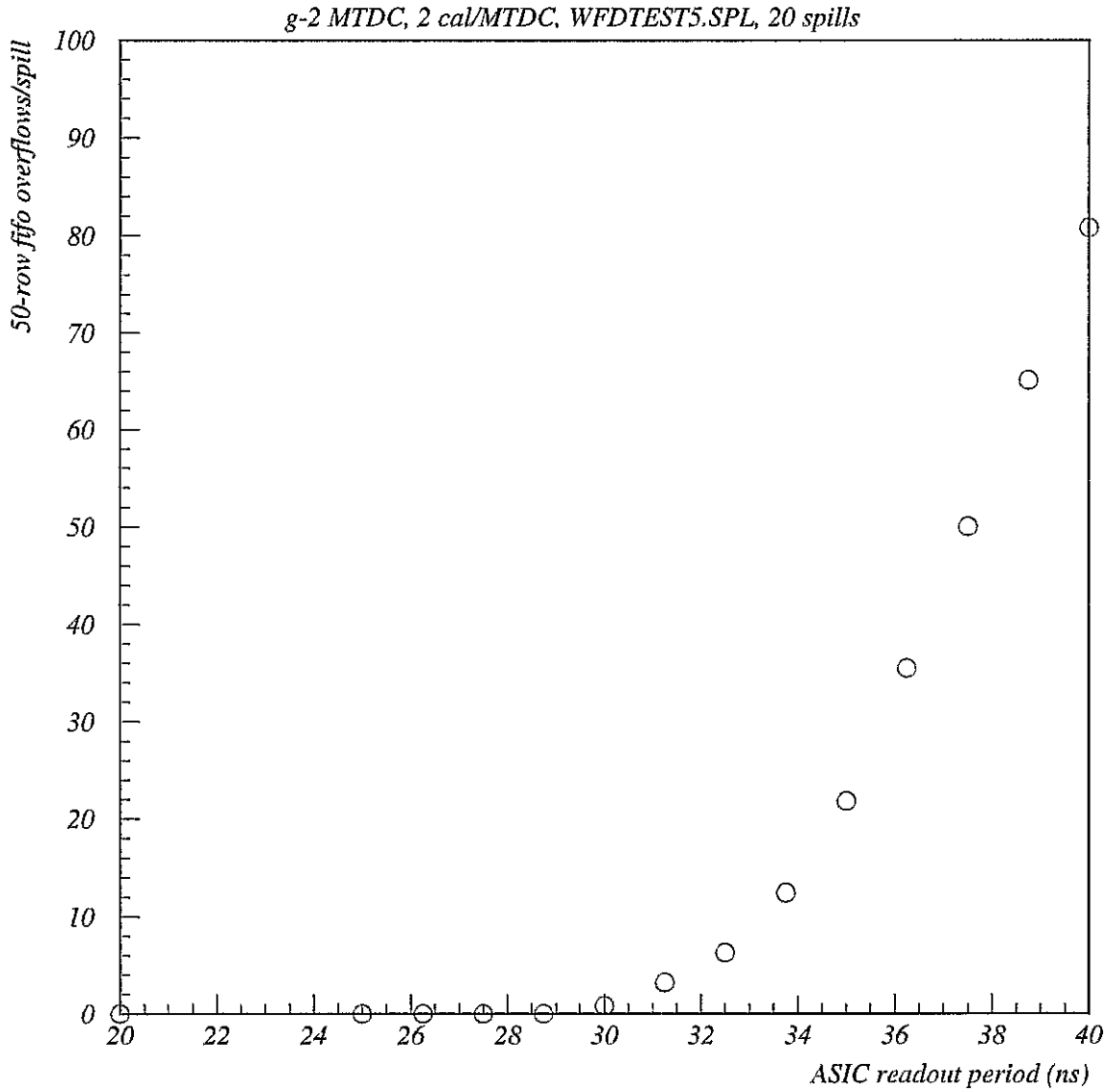

Figure 4: The queuing loss simulation for the ASIC at various readout rates. Note that this is for 2 calorimeters at an initial spill rate of 10MHz.

MTDC Basic Test Set-up

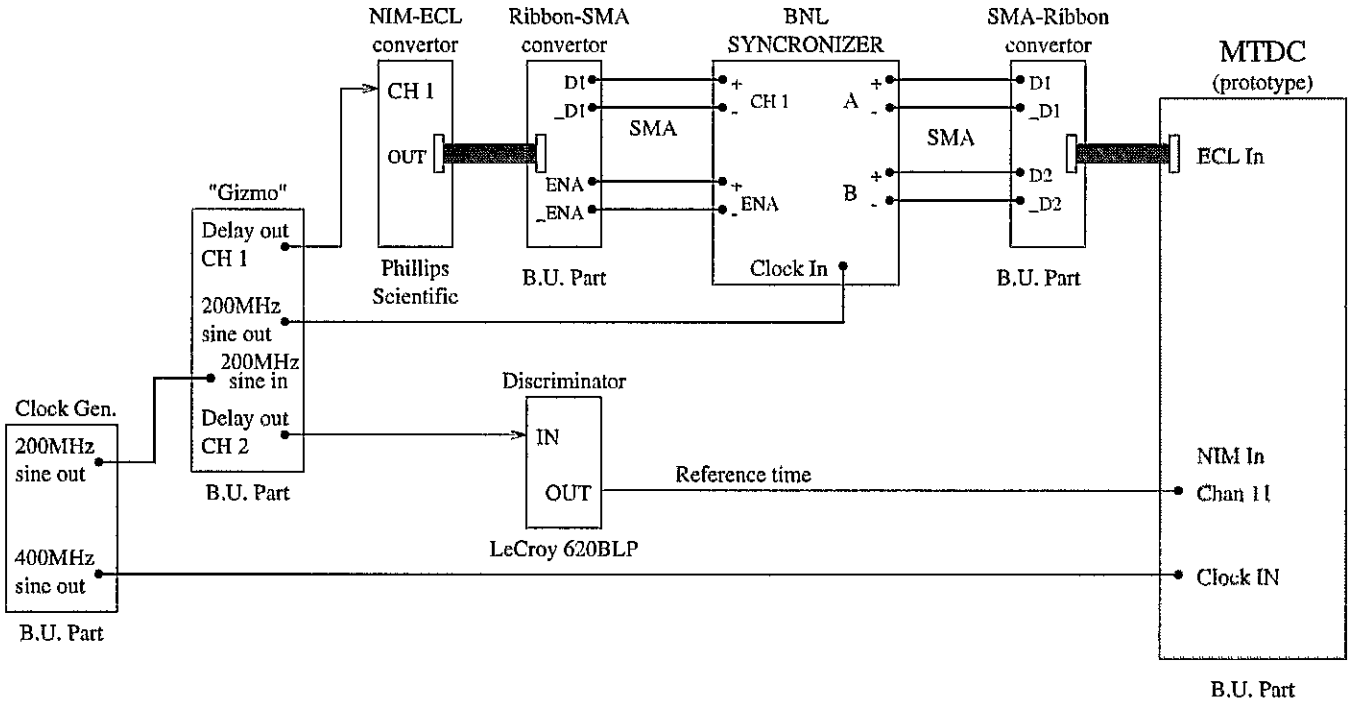

Figure 5: The test set-up used for evaluating the MTDC.

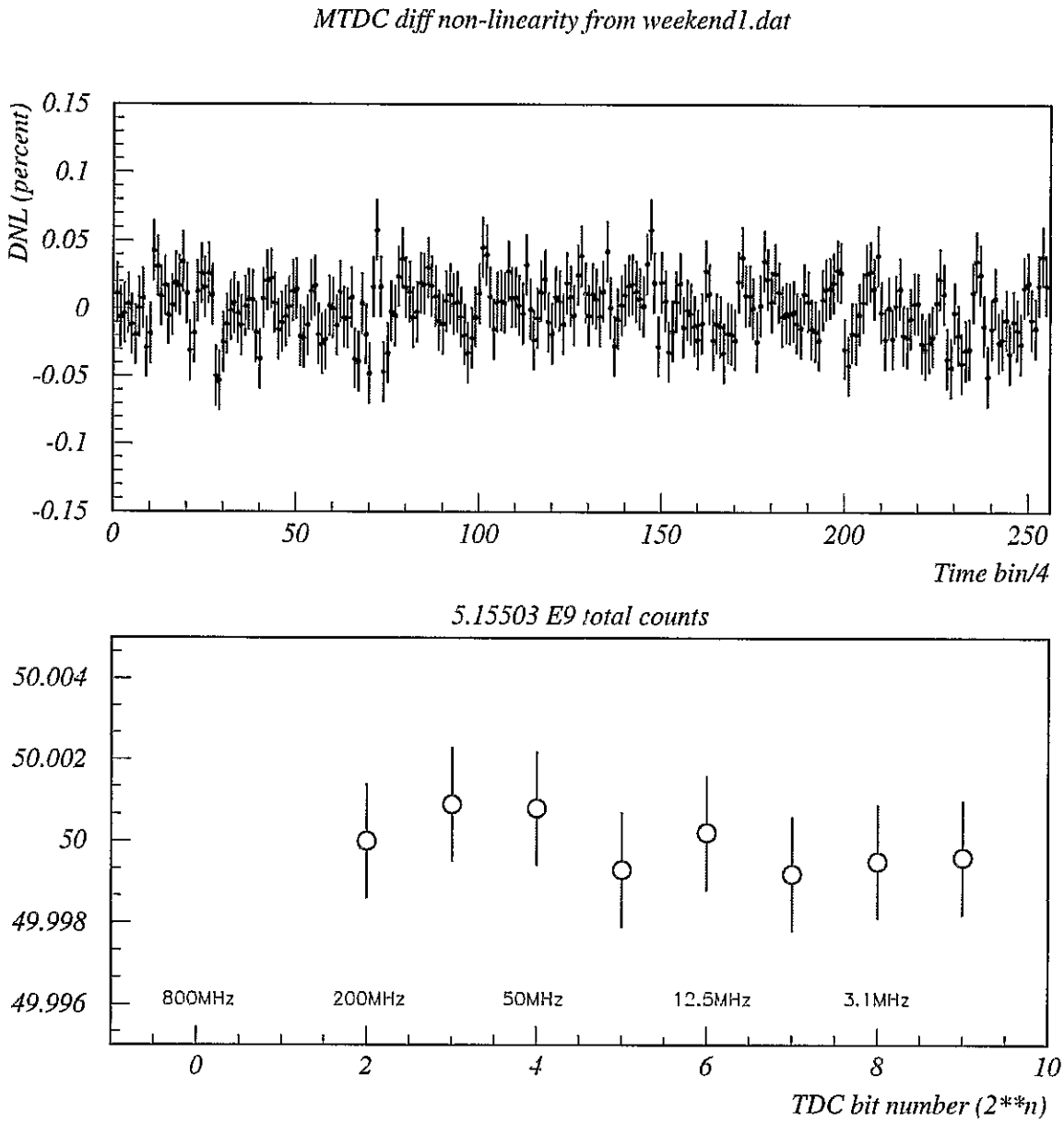

Figure 6: A demonstration of the excellent Differential Non-linearity of the Derandomizer/MTDC system.