For Internal Distribution Only

Brookhaven National Laboratory

Associated Universities Incorporated

Upton, New York 11973

Muon g-2 Note No. 269

Title: **VMEbus Specification for the MACRO Waveform Digitizer (WFD)**

Author(s): **William E. Earle**

Affiliation: **Boston University**

Date: **October 7, 1996**

VMEbus Specification for the MACRO Waveform Digitizer (WFD)

William E. Earle

October 7, 1996

Contents

List of Tables

1 Introduction

The MACRO WFD is a VMEbus slave module designed to digitize and store four channels of analog input data at a rate up to 200 megasamples per second for each channel. Each channel performs its digitization using a 200 MHz, 8 bit, flash A/D converter. After every four conversions, the digitized data is stored as a parallel group of four bytes, allowing a 50 MHz rather than 200 MHz storage rate. At the time each group of four data bytes is stored, a 16 bit time word (incremented every 5ns) plus two bytes of discriminator information are also stored, resulting in a total of eight bytes of information being stored at a rate up to 50 MHz. Each channel of the module is allotted 64K bytes of storage, 32K for samples and 32K for time and discriminator data.

The purpose of this specification is to describe the manner in which the VMEbus interfaces to the MACRO WFD module for purposes of reading this stored data and for sending control information to the module. This specification does not cover other details of the WFD. The module adheres to the IEEE 1014-1987 version of the VMEbus standard.

2 VME Features Supported

The following VMEbus features are supported:

- Data Transfer: D08(EO), D16 and D32 transfers, including unaligned transfers (UAT) and block transfers (BLT).
- Addressing: A16, A24 and A32 modes using the address modifier codes shown in Table 1.
- Interrupter: D0(O) only. Any one of the I(1)$\cdots$I(7) interrupt request lines is switch selectable. The status/ID code is also switch selectable.

3 Address Allocation

The byte addresses used by the WFD are divided into a sample storage area of 256K bytes (64K per channel) and a control storage area of 128 bytes (32

bytes per channel). The base addresses for these two areas are set by two switches located on the WFD module.

3.1 Data Storage

The data storage area consists of 256k bytes of contiguous storage divided into four 64K blocks, one per channel, with each of these blocks subdivided into two 32K blocks, one for the A/D samples and the other for the time and discriminator information. Table 2 shows the storage layout for the sample information. These 8 bit samples are stored four bytes at a time, ADC(0)–ADC(3), with ADC(0) always being the most recent sample. Note that these bytes are stored in decreasing address order; that is, the most recent bytes and groups of bytes are at the lowest addresses. This reverse storage order is intentional in order for a block-read to be able to read the samples in the order of most recent to least recent.

The time and discriminator information is stored as shown in Table 3. Note that this information is offset by 8000 (hex) bytes from the corresponding sample information shown in Table 2. For a particular group of four A/D samples, the time word has a fixed, but unspecified, relationship to the time at which the four corresponding samples are taken. That is, it always corresponds to the same point in the time interval for obtaining the four samples, but the location of this point is not specified. The two discriminator bytes DISC(0,1) and DISC(2,3) contain the output levels of the threshold comparators at the time of sampling. Since there are four discriminators per channel, there are four threshold levels or bits associated with each sample. The data formats for DISC(0,1) and DISC(2,3) are shown in Table 4.

The data storage area may be read via VMEbus but cannot normally be written.

3.2 Control Storage

The control storage area occupies 32 bytes for each channel, but only the most significant byte of each four byte group is used, namely VMEbus BYTE(0). Four discriminator threshold settings and one byte for the control register may be written to this area in accordance with Table 5. Note that there are four possible locations for writing to each channel's control register.

The discriminator thresholds contain the eight bit threshold settings for the DAC's used with the comparators. Table 5 is somewhat misleading in that writing to any one of the threshold addresses actually writes to a buffer register rather than to the threshold register itself. The data in the buffer register is only transferred to the actual threshold register by then toggling bit 7 of the respective control register high and then low. For example, to set the discriminator 0 threshold of channel 1, one would first write the data to any one of the four discriminator 0 addresses, 0FFF0, 1FFF0, 2FFF0 or 3FFF0 (this writes the data to the buffer). Then bit 7 of the channel 1 control register is clocked high and then low to transfer the buffer contents to the final threshold register. Note that the same buffer data could be successively transferred to all four discriminator 0 registers by successively clocking bit 7 of each control register high and then low without having to reload the buffer register.

The control register for each channel is used to control zero suppression, interrupt enabling, module resetting, time word rollover, stop-enable time word writing, clocking the threshold DACs and two special functions. Bit 0 of the control register enables zero suppression when set (the discriminator thresholds are effectively set to zero if this bit is cleared). Bit 1 enables interrupts when set. Bits 2 and 3 of the control register control the special functions described below. Bit 4 is used to enable time word rollover when set. Time word rollover means that when the 16 bit time word rolls over from all ones to all zeros, a forced sample storage cycle occurs in order that the rollover condition can be noted in the sample data. When bit 5 of the control register is set, the module is reset. This bit is not latched so the reset action is momentary. Bit 6 of the control register, when set, enables the stop function for all four channels. This function causes an additional cycle to occur after the channels are stopped in order to write the stop time into the RAM. Thus, the last data in the RAM would contain the stop time rather than the last sample time, which easily could be different from the stop time. Since all channels would record their stop times within 5 nanoseconds of each other, these times could be used to determine time synchronization amongst the channels. If bit 6 of the control register is not set, then the arrival of a NIM stop signal would stop all four timers but would not result in an additional cycle to save the stop times. As mentioned earlier, bit 7 of each control register is used to clock the discriminator threshold data from the buffer into the actual discriminator register. Note that bits 0, 3, 4 and 7 are

unique for each control register, whereas bits 1,2,5 and 6 are common to all control registers and may be set by writing to any one of them.

The control storage area is write-only in terms of VMEbus operations.

Table 6 lists the bit assignments for the control registers.

4 Base Address Selection

Each WFD module has two switches for setting the base address of the sample data and control memory areas.

- SW1 (5 bits) This switch sets the module number within a crate and also sets the 256K offset of the sample memory and the control storage area. When an interrupt occurs, these five bits are returned as the lower five bits of the interrupt status/ID byte.
- SW2 (9 bits) This switch sets the offset of the sample and control memory in 8M increments within the 4000M possible addresses in an A32 VME system.

Table 7 shows the bit assignments for the switches. Note that the data storage and control storage are able to occupy the same address space, since the data storage is read-only while the control storage is write-only.

5 Special Functions

Bits 2 and 3 of any control register control two special functions, testing the data storage memory and reading the internal memory address.

Normally the data storage memory operates in a read-only mode, but if bit 2, the read-write bit, of any control register is set, the data storage area changes to a read-write mode, allowing VMEbus to perform both write and read cycles to verify proper memory operation. However, once in this read-write mode, the control storage is no longer addressable, so bit 2 of the control register cannot be cleared directly to escape from this mode. The mechanism for resetting bit 2 and returning to the normal read-only mode is to execute a read cycle to address FFFF. Thus, a possible memory test sequence might consist of setting bit 2 of any control byte, writing test data

into locations 0000 through FFFF for a particular channel, and then reading and verifying the data in locations 0000 through FFFF. Upon reading the data in the last location, FFFF, the data memory reverts to its normal read-only mode of operation. Note that the address space for each channel must be tested individually; that is, after testing any 64k block (one channel's address space), the read-write bit will have been cleared and will have to be set again before testing the next 64k block of memory.

If bit 3 of a control register is set, then any read operation from that channel's data storage memory returns the current memory address (**address**) for that channel as a 15 bit value (mod 4). The exact address used by VMEbus during this read operation is unimportant but it must lie within the address space of the channel from which the memory address is to be obtained. Bit 3 must be explicitly cleared to revert to normal memory reading.

address contains the address of the next stored sample data. For example, if the WFD has just received a stop signal and the contents of **address** is read as 0108, then this indicates that the most recent four sample bytes were written into addresses 0110-010C and the corresponding time and discriminator information was written into addresses 8110-810C. Normally **address** is used as the starting address for reading back the most recent sample data. Note that **address** is a 15 bit, mod 4 value since the sample storage area for each channel consists of 32K bytes of samples; being mod 4, however, the lower two bits are always zero, so that sequential values of **address** would be 0108, 010C, 0110, etc. It should also be noted that this value will roll over from 0000 to 7FFC when samples are being stored and that this range is the same for all four channels of a module. This means that the user must add a channel offset of 10000 (hex) per channel to this address to get the actual address within the 32K sample area. As an example, if **address** for channel 3 is read as 0108, then the most recent data as far as the VMEbus is concerned is at 3010C (hex) and the corresponding time and discriminator data is at 3810C. This should become clearer by referring to Table 8, which shows the complete data storage area for one module.

6 Interrupts

The MACRO WFD contains a VMEbus interrupter, which can interrupt the CPU when a STOP input occurs. The VMEbus defines eight interrupt

request lines (I(1)$\cdots$I(7)) of different priority. The WFD can use any one of these lines, as determined by the setting of the switches in SW3. In addition, the VMEbus module must return a status/ID code when generating an interrupt in order for the interrupting module to be identified. The WFD generates only 8-bit D08(O) status/ID codes. The bits of the status/ID code are defined as follows:

7	6	5	4	3	2	1	0
SW3(1)	SW3(2)	SW3(3)	SW1(1)	SW1(2)	SW1(3)	SW1(4)	SW1(5)

SW1 is also the module number in the crate. The interrupter may be enabled or disabled by clearing the interrupt bit (bit 1) in any of the control registers.

Table 9 shows the correspondence between SW3 switch settings and the interrupt priority.

7 Comments

The WFD module must be in its stopped state whenever VMEbus is being used to read data or to output control settings. If the module is not stopped, then VMEbus data transfers will result in a BERR* rather than a DTACK* response to the master.

There is no provision for setting **address** for any channel to an arbitrary value. However, a NIM_RESET signal may be used to set all addresses to FFFF. Normally **address** only changes when new data from the A/D converter is stored; however, **address** may be read, as mentioned earlier, in order to know where to start a VMEbus read operation.

Note that the sample data memory for any channel rolls over at 7FFF to 0000, so when reading across this boundary, care should be taken to reset the lower 15 bits of the VMEbus address to 0000. For example, if **address** for channel 0 is read as 7FFC, then to read the most recent 16 bytes of sample data, one would read bytes 7FFC through 7FFF and then bytes 0000 through 000B. If one were to read bytes 7FFC through 800B, one would get

four bytes of sample data followed by 12 bytes of time/discriminator data rather than the next 12 bytes of sample data.

Similarly, the discriminator/time-word data memory rolls over at FFFF to 8000, so when reading across this boundary, the lower 15 bits of the VMEbus address should be reset to 8000 to avoid reading sample data from the next channel.

A low level on SYSRESET* resets the interrupt request bit but otherwise does not reset or stop digitizing by the waveform digitizer. The DAC thresholds are not directly affected by SYSRESET*, but if SYSRESET* occurs because of a power loss, then the threshold values are probably incorrect and should be re-sent to the DACs.

Table 1: Allowed Address Modifier Codes

Address Modifier (Hex)	No. of Address Bits	Transfer Type
3F	24	Standard supervisory block transfer
3D	24	Standard supervisory data access
3B	24	Standard non-privileged block transfer
39	24	Standard non-privileged data access
2D	16	Short supervisory access
29	16	Short non-privileged access
0F	32	Extended supervisory block transfer
0D	32	Extended supervisory data access
0B	32	Extended non-privileged block transfer
09	32	Extended non-privileged data access

Table 2: A/D Sample Storage

Byte Address	VMEbus Byte	A/D Converter Byte	
⋮	⋮	⋮	⋮
00FF	BYTE(3)	ADC(3)	
0100	BYTE(0)	ADC(0) more recent	more
0101	BYTE(1)	ADC(1)	recent
0102	BYTE(2)	ADC(2)	data
0103	BYTE(3)	ADC(3) less recent	group
0104	BYTE(0)	ADC(0)	
⋮	⋮	⋮	⋮
0303	BYTE(3)	ADC(3)	
0304	BYTE(0)	ADC(0) more recent	less
0305	BYTE(1)	ADC(1)	recent
0306	BYTE(2)	ADC(2)	data
0307	BYTE(3)	ADC(3) less recent	group
0308	BYTE(0)	ADC(0)	
⋮	⋮	⋮	⋮

Table 3: Discriminator and Time Storage

Byte Address	VMEbus Byte	Time/Disc Byte	
⋮	⋮	⋮	⋮
80FF	BYTE(3)	DISC(2,3)	
8100	BYTE(0)	TIME (MSB)	more
8101	BYTE(1)	TIME (LSB)	recent
8102	BYTE(2)	DISC(0,1)	data
8103	BYTE(3)	DISC(2,3)	group
8104	BYTE(0)	TIME (MSB)	
⋮	⋮	⋮	⋮
8303	BYTE(3)	DISC(2,3)	
8304	BYTE(0)	TIME (MSB)	less
8305	BYTE(1)	TIME (LSB)	recent
8306	BYTE(2)	DISC(0,1)	data
8307	BYTE(3)	DISC(2,3)	group
8308	BYTE(0)	TIME (MSB)	
⋮	⋮	⋮	⋮

Table 4: Data Formats for DISC(0,1) and DISC(2,3)

DISC(0,1) DISC(2,3) bits	Comparator Number	Corresponding DISC(0,1) Sample	Corresponding DISC(2,3) Sample
7 (msb)	3	ADC(0)	ADC(2)
6	2		
5	1		
4	0		
3	3	ADC(1)	ADC(3)
2	2		
1	1		
0 (lsb)	0		

Table 5: Control Storage for One Module

Address	Channel	Function
0FFE0	0	control register
0FFE4		
0FFE8		
0FFEC		
0FFF0		discriminator 0 threshold
0FFF4		discriminator 1 threshold
0FFF8		discriminator 2 threshold
0FFFC		discriminator 3 threshold
1FFE0	1	control register
1FFE4		
1FFE8		
1FFEC		
1FFF0		discriminator 0 threshold
1FFF4		discriminator 1 threshold
1FFF8		discriminator 2 threshold
1FFFC		discriminator 3 threshold
2FFE0	2	control register
2FFE4		
2FFE8		
2FFEC		
2FFF0		discriminator 0 threshold
2FFF4		discriminator 1 threshold
2FFF8		discriminator 2 threshold
2FFFC		discriminator 3 threshold
3FFE0	3	control register
3FFE4		
3FFE8		
3FFEC		
3FFF0		discriminator 0 threshold
3FFF4		discriminator 1 threshold
3FFF8		discriminator 2 threshold
3FFFC		discriminator 3 threshold

Table 6: Bit Assignments for the Control Registers

Bit Number	Use
7	DAC Clock
6	Stop Enable
5	Reset
4	Rollover Enable
3	Address Enable
2	Read/Write Enable
1	Interrupt Enable
0	Zero Suppression Enable

Table 7: Address Configuration Switches

Switch	Sample Address Bits	Control Address Bits
SW1	A18–A22	A18-A22
SW2	A23–A31	A23–A31

Table 8: Data Storage for One Module

Address	Data	Storage	Channel
0000	ADC(0)		
0001	ADC(1)		
0002	ADC(2)		
0003	ADC(3)		
⋮	⋮	32K bytes	
7FFC	ADC(0)		
7FFD	ADC(1)		
7FFE	ADC(2)		
7FFF	ADC(3)		0
8000	TIME (MSB)		
8001	TIME (LSB)		
8002	DISC(0,1)		
8003	DISC(2,3)		
⋮	⋮	32K bytes	
FFFC	TIME (MSB)		
FFFD	TIME (LSB)		
FFFE	DISC(0,1)		
FFFF	DISC(2,3)		
10000			
⋮		64K bytes	1
1FFFF			
20000			
⋮		64K bytes	2
2FFFF			
30000			
⋮		64K bytes	3
3FFFF			

Table 9: Interrupt Priority Selection

SW3(1)	SW3(2)	SW3(3)	Interrupt Level
off	off	off	(interrupts disabled)
off	off	on	I(1)
off	on	off	I(2)
off	on	on	I(3)
on	off	off	I(4)
on	off	on	I(5)
on	on	off	I(6)
on	on	on	I(7)