Synchronization tests with new ACQ1002 modules

Kabir, Irakli, Vince

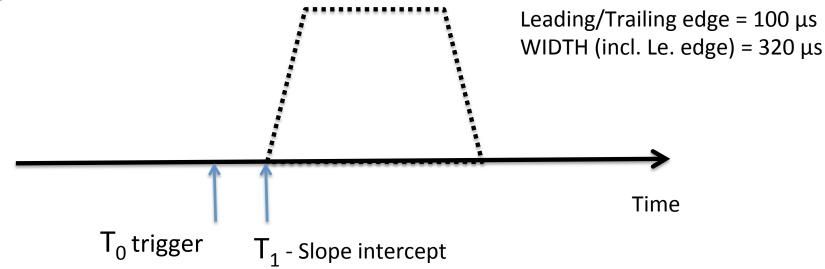
Introduction

Trying to measure synchronization between Master Clock at 32 MHz and the ACQ435 module clock w/ sampling rate 64kHz

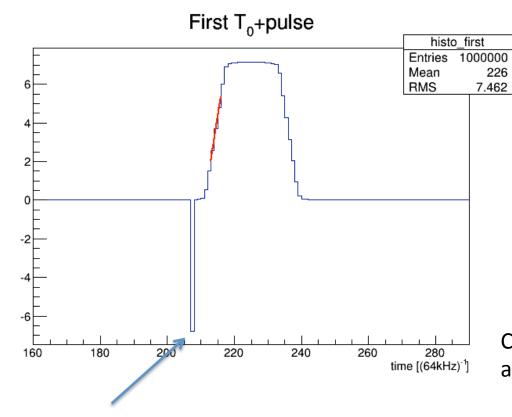
Testing or trying to confirm that in "synchronized mode" jitter between T_0 and First sampled point is from 0 - 32 MHz

In "Non-sync mode" jitter is expected to be from 0 – 64 kHz

Using hp 8161A Pulse Generator borrowed from nEDM (Vince) we have triggering at 60Hz and "modified square pulse" synchronized with the generated trigger



test signal from ADC and algorithm



Because RC delay from generator Leading edge starts $\sim 40 \mu s$ from T₀

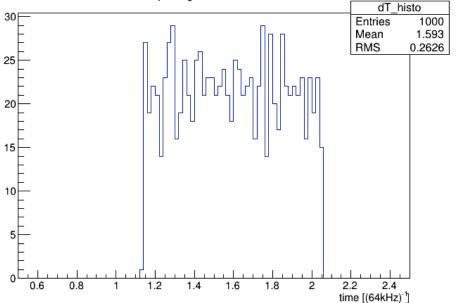
Fitting middle (3 bins) of the Leading edge by pol1 and calculating the y=0 intercept

Calculating $\Delta T = T1 - T0$ for every pulse

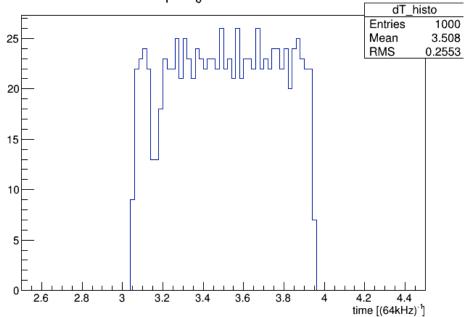
Comparing ΔT distributions between "sync" and "non-sync" modes

Header – serving as T0

NON-SYNC $T_1 - T_0$ distribution



SYNC $T_1 - T_0$ distribution



ΔT distribution

X-axis in units of 1/64kHz

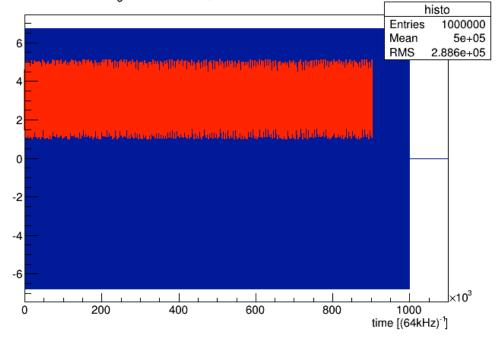
Expected spread:

- ~ 1/64kHz for NON-sync
- ~ 1/32MHz for SYNC, i.e. much smaller

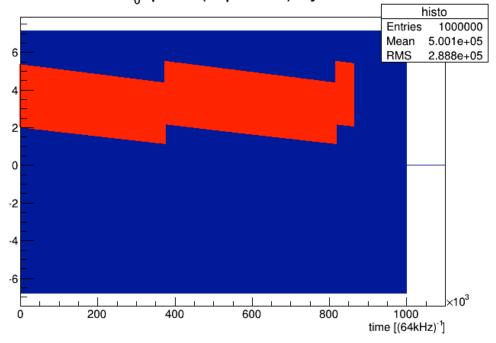
But both appear to be of the same size ~ 64kHz

No synchronization?

T₀+pulse (expanded) NON-sync.



To+pulse (expanded) Sync.



All pulses w/ fits

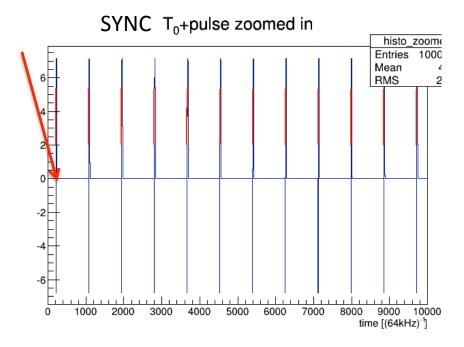
In Non-sync mode samples appears to be randomly distributed after T_0 with width ~ 1/64 kHz... as expected

In Sync mode it is systematically shifting and then "resetting" back and shifting again...resulting in the similar width

But if truly synchronized shouldn't we see also random distribution of samples with respect to T_0 with width of 32 MHz?

Last night Vince pointed out that "drifting cycle" is suspiciously close to 500 counts. ($500 \times 64 \text{kHz} = 32 \text{ MHz}$)

Could it be that every T₀ trigger samples are drifting away from it by single Master clock tick (1/32MHz) and then resetting????



Just another note: First few pulses

After "START" data sampling starts before First T_0 trigger.

This is sometimes the case even for "SYNC mode" as shown (lower plot)

Kabir noticed that sometimes data sampling does start with the first T_0 trigger for SYNC mode ... but only sometimes!