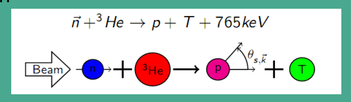
Data Acquisition System(DAQ) for the n-^{3}He Experiment at SNS

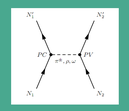
Latiful Kabir, C.B. Crawford, Irakli Garishvili
for the n^{3}He Collaboration

Abstract: *The n3He experiment at the Spallation Neutron Source will measure the parity violating spin asymmetry of the recoil proton in the reaction n+ ^{3}He-->p +T+765 KeV. This is sensitive to ΔI=0 and 1 components of the Hadronic Weak Interaction (HWI), and is expected to be extremely small (~10^{-7}). Protons from the reaction are recorded in current mode in order to achieve a statistical sensitivity of 10^{-8} in a reasonable amount of time. In addition instrumental asymmetries must be suppressed by an additional order of magnitude. The asymmetry is measured as a function of time-of-flight of the neutron to study the energy dependence of any systematic effects. Here we present details and preliminary tests of the 144 channel data acquisition system designed to meet these requirements.*

The n^{3}He Experiment

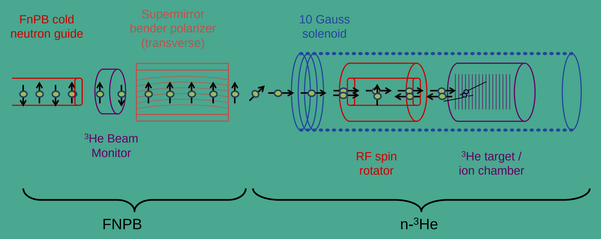
The n^{3}He experiment at SNS is a high-precision measurement motivated to probe the hadronic weak interaction by measuring the parity violating asymmetry of the proton in the reaction-





This asymmetry is expected to be extremely small (of the order 10 $^{-7}$). Our goal is to measure an asymmetry in the reaction to a precision of 2 x 10^{-8}.

Experimental Setup



- n-^{3}He is using a spin flipper with transverse windings which allows for both longitudinal and transverse spin rotation.
- ^{3}He ion chamber – both target and detector
- Detectors work in current mode.

DAQ for n^{3}He : Expectations

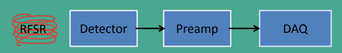
General expectations:

To achieve our goal, following are the expectations form the DAQ in general :

- Capable of dealing with large amount of data at high sample rate but maintain very low ADC noise.
- Has high channel density with simultaneous input.
- Maximum sampling rate but the file size manageable / durable.
- Triggering using software taking accelerator T_0 as input.
- Can take data only in our region of interest.
- Time bin and the number of entries per run can be adjusted.
- Synchronization of all the ADC modules with T_0 .
- Checksum algorithm to detect corrupt data .
- Built in event header.

Expectations for Systematics :

The signal from the front plane will be at full range (10 V). The signal in the back plane will be 0.1% of full range. Size of asymmetry is A ~10^{-7}. Our expected uncertainty in asymmetry is ΔA = 2x 10^{-8} (Statistical). And expected maximum contribution from systematics, ΔA_{sys}= 10% of ΔA.
This makes expected $\Delta A_{sys} < 10^{-9}$



Then the biggest challenge becomes achieving this ΔA_{sys} , provided that the spin flipper in the experiment will be turning on and off at 30Hz.

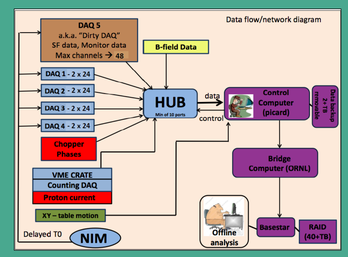
DAQ for n^{3}He : ADC Modules

To fulfill all these expectations we use the DAQ by D-tAcq with the following features:

- Delta sigma technology based ADC (ACQ1002) by d-tAcq Solutions.
- Zynq 7000 –series hybrid FPGA + 2 ARM CPU cores + FMC .
- 24 bit ADC per channel for true simultaneous analog input.
- Maximum sampling rate 128 kSPS (minimum is 8 kSPS) per channel.
- 2x24 Channels per module.
- Signal to noise ratio is 104 dB (high speed) or 108 dB (high resolution).
- 1GB DDR memory on board.
- External clock, trigger, internal clock.
- Runs embedded Linux.
- Firmware on a flash memory, can be updated easily.

- The DAQ can be accessed through ssh or console.
- It has several separate sites for capture and configuration.
- The data is transferred and saved to control computer using TCP/IP connection(e.g. netcat).
- Supports EPICS CSS for controlling the DAQ.
- Data and run time parameters can be viewed in real time using CSS

On the right we show how everything fits into a whole network.



Measurements : ADC noise and rise time

Bare ADC noise was measured to be 27 micro volt at 50 kHz sample rate. Performance of ADC and its noise with different sample rate shows that the noise jumps after a cutoff, this is because it has two different modes (resolutions) of operation. Thus based on counting statistics, running the DAQ at 50 kHz and then averaging 20 successive points will give most optimal ADC noise.

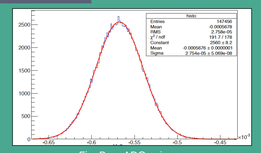


Fig: Bare ADC noise

Fig: ADC noise vs sample rate

Fig: ADC noise after merging 5 points

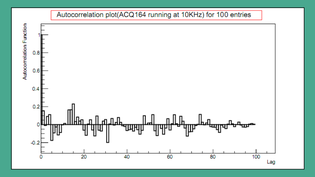


Fig: Autocorrelation Plot

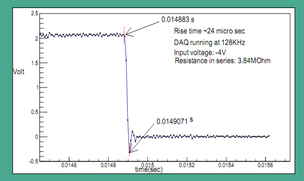


Fig: Plot for rise time

The autocorrelation plot confirms no apparent correlation for ADC noise and the rise time is found to be as expected.

Measurements : Resynchronization and Jitter

The ADC has a 30 MHz internal clock which is used as the reference for the sample clock (rate). Because of the importance of neutron's time of flight for the experiment, a jitter of the order of kHz is too high. So the ADC was customized to resynchronize after each event to give a jitter of the order of MHz.
Following is a test to confirm the desired jitter of the ADC:
60 Hz pulse with ramp, which has a width of 320 μs, a rising edge of 100 μs and a tailing edge 100 μs, was fed to the ADC in repeating gate mode with trigger on leading edge. Then each rising edge of the pulse (5 points in the middle of leading edge) is fitted to the linear equation y=ax+b using least square method. This gives x-intercept and the slope of the leading edge. For each fit ,the x-value for the header is subtracted from the x-intercept of the rising edge. This constitute: $\Delta t = t_i - t_0$ Where, t_i=Intercept from fit t_0= x-value for header. This is done for all the pulses. Finally Δt vs Pulse number is plotted. A histogram for all the Δt is drawn. The histogram shows that the jitter is of the order of 20 nano sec.

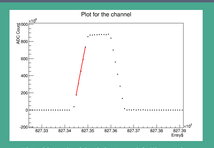
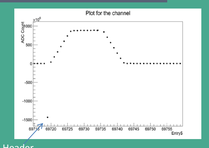


Fig: Signal with rising and falling edge



Header
Fig: Signal with rising and falling edge with header

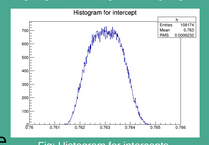


Fig: Histogram for intercepts

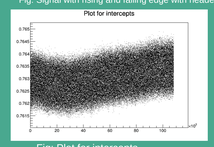


Fig: Plot for intercepts

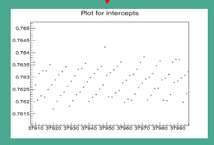


Fig: Zoomed plot for intercepts

Measurements : Averaging & Decimation

To keep the data file size manageable but at the same time utilize the maximum sample rate, the ADC was customized to do averaging and decimation of desired number of entries.
Following are the tests that were performed to confirm this feature:
Suppose we have a pulse/signal as shown on the right . Where all entries are effectively(close to) zero except one entry/point. Here the first diagram (on left) is just one pulse. And second diagram(on right) is what we see if we take data for certain time(in Resync mode) and plot using ROOT i.e. it will squeeze so many pulses in a small range that it will appear as just two lines . Now what we are interested in is just the height of the upper line. Because, if we find the height without any averaging to be 'h' , then when we merge 'x' entries, the height of the upper line will be shifted to 'h/x' . This is exactly what we observe when we enable the averaging option.
Again by plotting data without averaging, with averaging and data from interpolation on a single plot we re-confirmed the same feature.

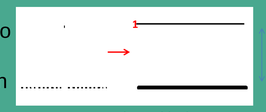


Fig: An ideal case

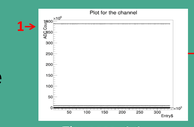


Fig: nacc=1,1

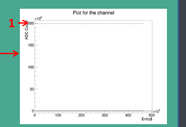
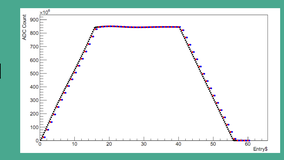


Fig: nacc=2,2



In black circle: nacc=1,1 data
In red circle: nacc =4,4 data
In blue circle : Interpolated data

X axis Unit:
Blue points: 1 EntryŠ = 1 x 1 Entry
Red Points: 1 EntryŠ = 1 x 1 Entry
Black Points: 1 EntryŠ = 4 x 1 Entry

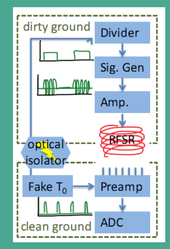
Note: A tiny X+(+0.4) offset for blue points has been added by hand so that we can see both blue and red.

Measurements : Instrumental Asymmetry

Finally our most important test is the measurement of instrumental asymmetry with the spin flipper. Here our sources of false asymmetries can be ground loops, electrostatic couplings, power supply couplings, circuit to circuit couplings and many others.
The schematic of the set up is shown on the right.
Following is the algorithm that we follow in measuring the false asymmetry :

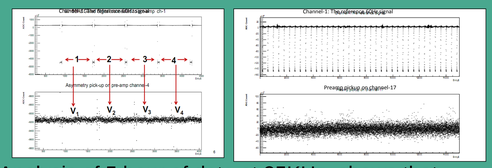
- We took equal number of entries between two T_0 pulses.
- We subtracted two adjacent (ON/OFF)states then normalized by the full scale of the ADC(20 Volts)

$A_1=(V_1-V_2)/20$
$A_2=(V_3-V_4)/20$ ….etc.
Asymmetry, $A=(A_1+A_2+A_3+\ldots\ldots+A_N)/N$



- To calculate uncertainty in false asymmetry, a histogram was drawn for asymmetries of individual pairs, A_K, k-1,2,….N
- Calculated width σ (sigma or RMS) of the histogram. Then finally,

$\Delta A = \sigma / \sqrt{N}$



Analysis of 5 hour of data at 25KHz shows that-
Asymmetry = 2.64 x 10^{-10} ± 1.64 x 10^{-10}

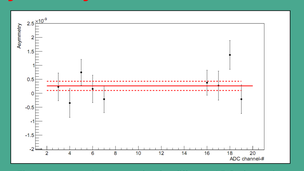


Fig: Instrumental asymmetries for different ADC channels

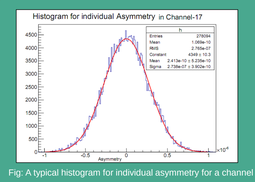


Fig: A typical histogram for individual asymmetry for a channel

Conclusion

We have a DAQ system that fulfills all of our expectations and gives instrumental asymmetry as small as **(2.64 ± 1.64) x 10^{-10} .** Thus we achieved our goal.