Resynchronization Test with Old fpga file

Run Configuration:

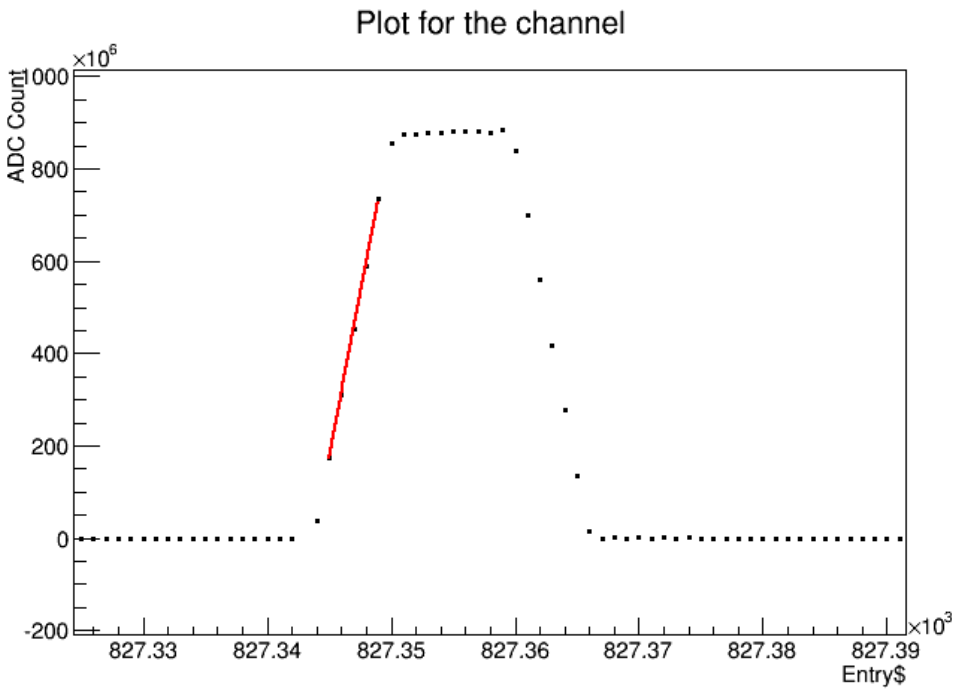
1. ADC running at 50 KHz, Hi Resolution Mode, Resynchronized Repeating Gate Mode(SRTM)
1. Gate Length = 700 entries (actually 664 entries),
2. Triggered on rising edge
3. External trigger = 60 Hz i.e. every 16.66 ms
4. Signal Analyzed (on channel-1) : 60 Hz pulse with ramp which has
   Width: 320 µs
   Leading edge: 100 µs
   Tailing edge: 100 µs

5. Duration of run: 5 minutes of data

The Algorithm:

1. Each rising edge of the pulse(5 points in the middle of rising edge) is fitted to the linear equation y=ax+b using least square method. This gives x-intercept and the slope of the rising edge.

2. For each fit ,the x-value for the header is subtracted from the X-intercept of the rising edge.



Units:

X-axis: 1 Entry= 1 Sample= 1/50KHz =20µs

Y-axis: 1 ADC count= 20Volt /2^{32} = 4.656 x10^{-09} Volt

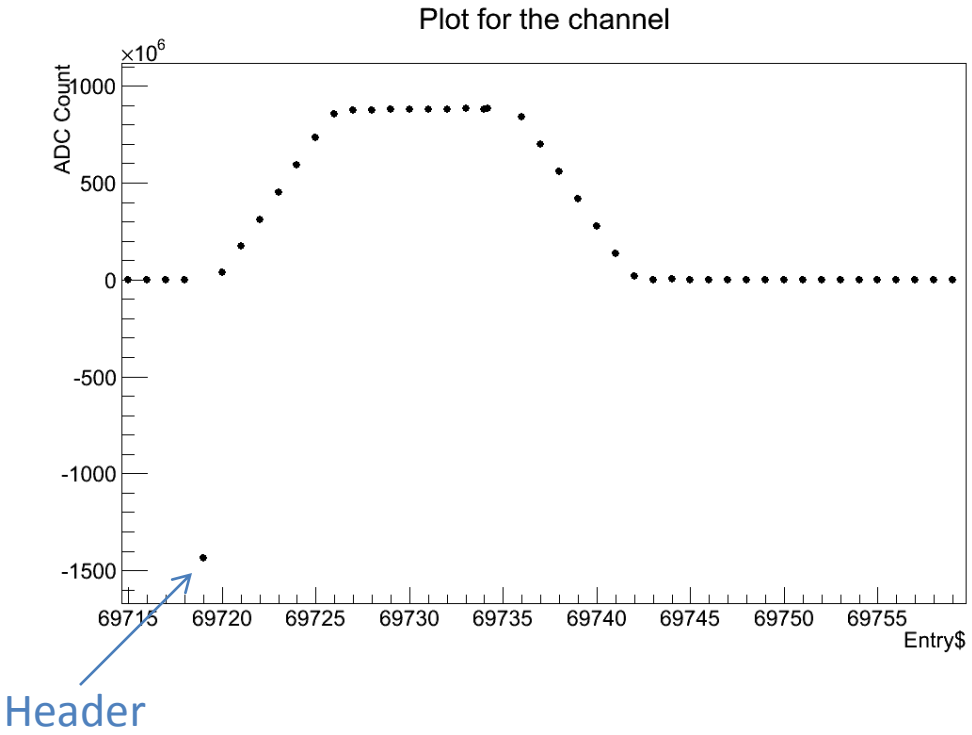
This constitute:

$\Delta t-=t_i-t_0$

Where, t_i=Intercept from fit

t_0= x-value for header

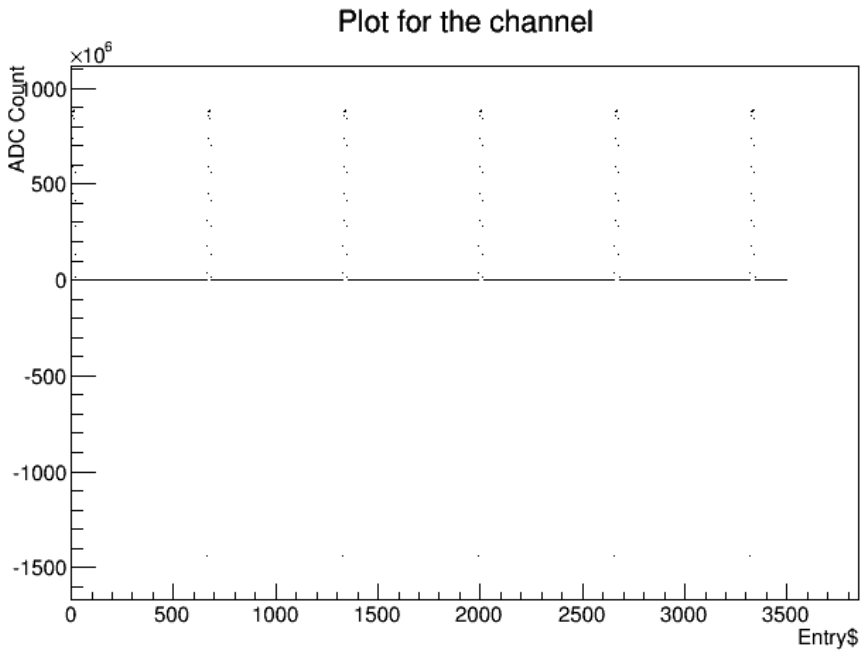
3. This is done for all the pulses.
4. Δt vs Pulse number is plotted.
5. Slope vs pulse number is plotted.
6. A histogram for all the Δt is drawn.



Units:

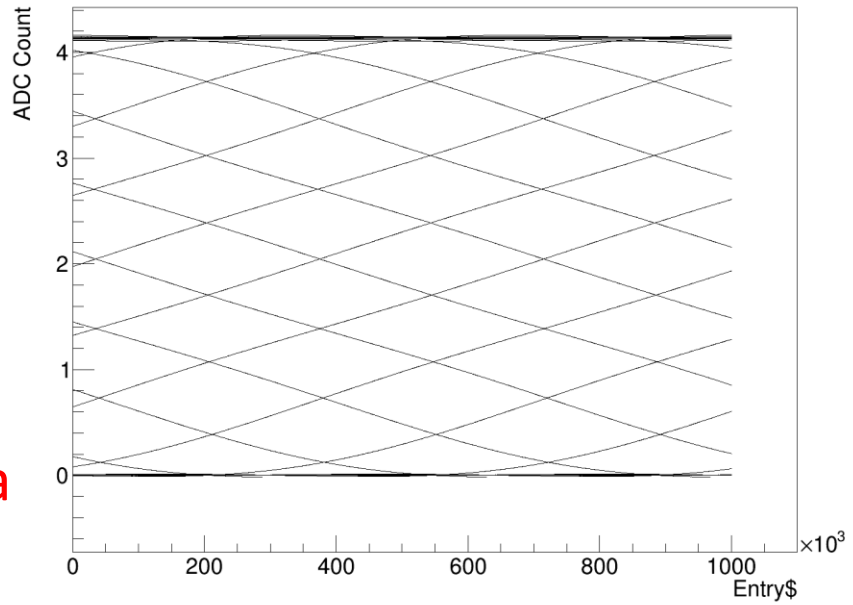
X-axis: 1 Entry= 1 Sample= 1/50KHz =20μs

Y-axis: 1 ADC count= 20Volt /2^{32} = 4.656 x10^{-09} Volt



If you squeeze 1500 Pulses like this You will get the following.
(Compare with new fpga plot and see the difference(Sufficient to understand something was wrong with old fpga))

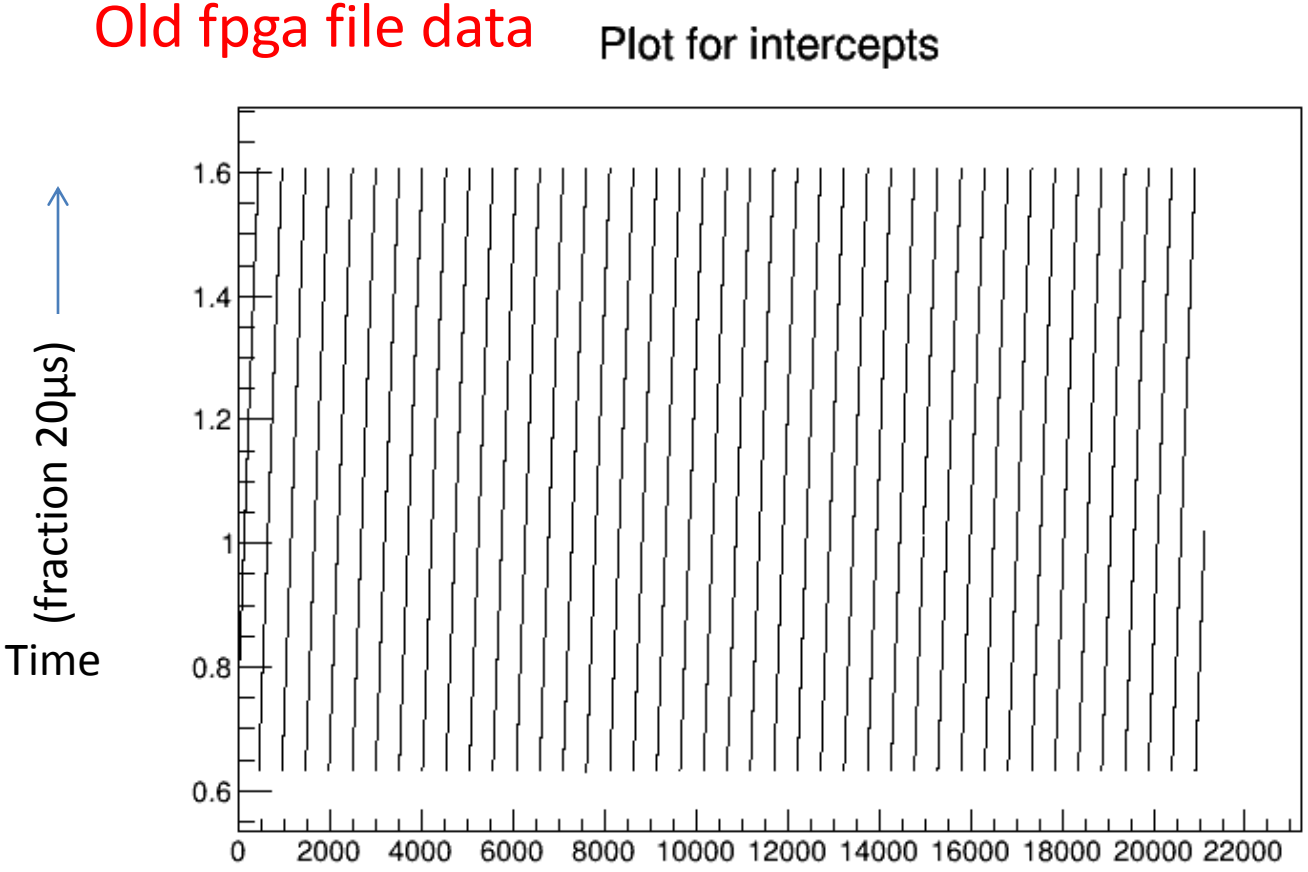
Graph



Units:
X-axis: 1 Entry= 1 Sample= 1/50KHz =20µs
Y-axis: 1 ADC count= 20Volt $/2^{32}$ = 4.656 x10^{-09} Volt

Old fpga file data

Old fpga file data



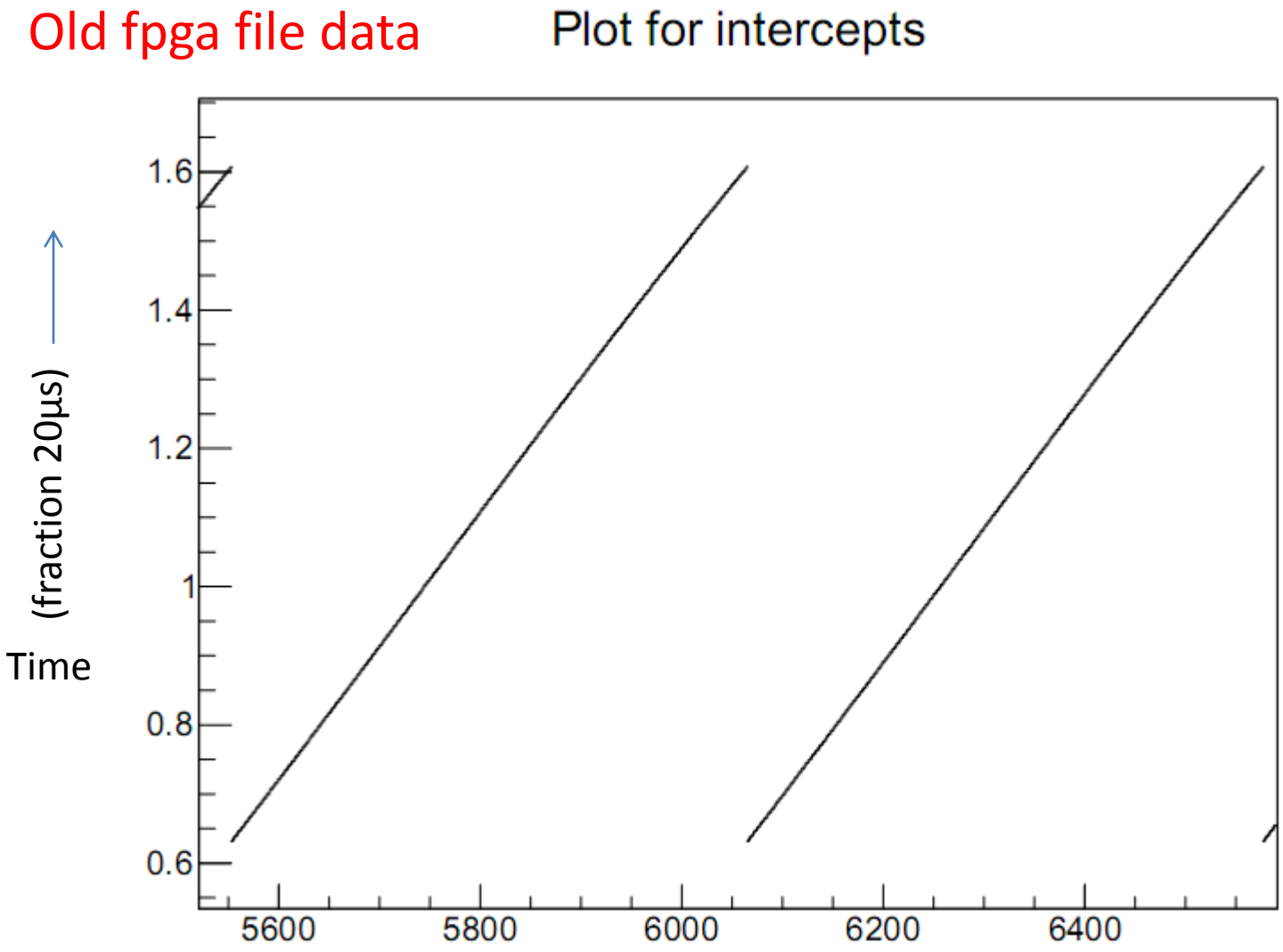
Units:

X-axis: 1pulse=700 Entries= 16.66ms (Including idle time) or 14ms (excluding idle time).

Y-axis: fraction of 20µs = fraction of time equivalent to 1 sample or entry

If we zoom in this part and increase marker size, we get next plot

Old fpga file data

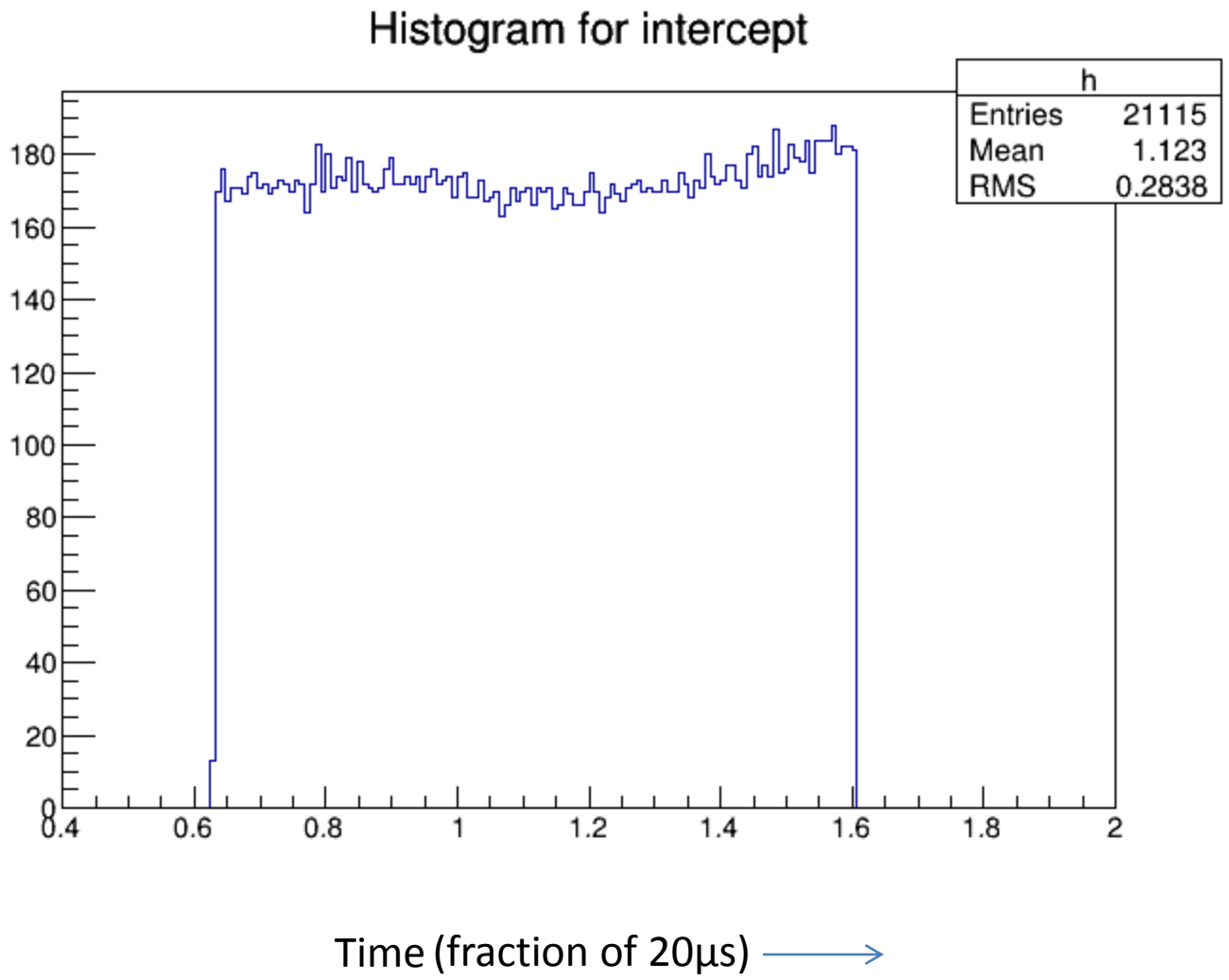


Units: Number of pulse →

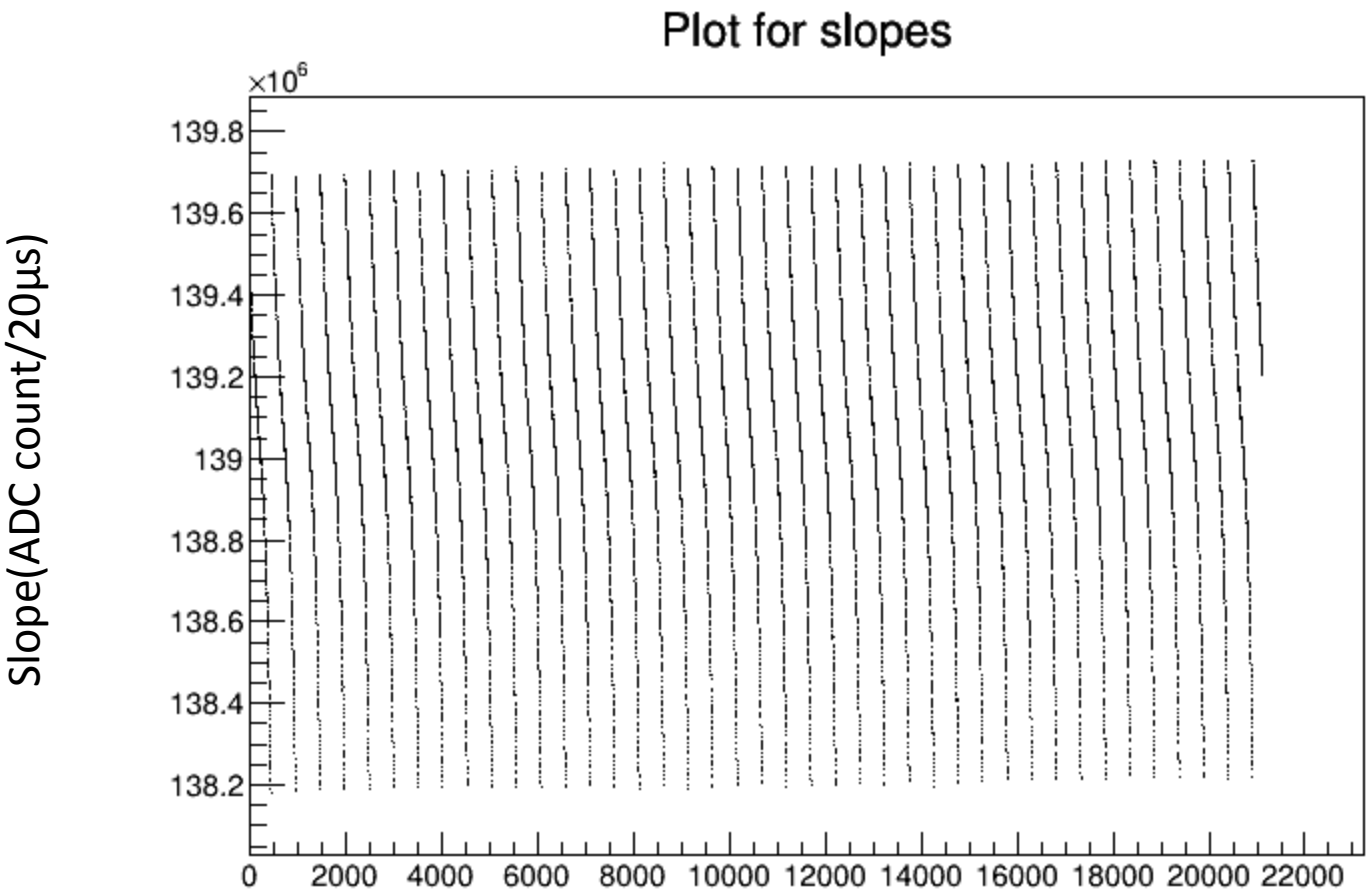
X-axis: 1pulse=700 Entries= 16.66ms (Including idle time)

Y-axis: fraction of 20µs =fraction of time equivalent to 1 sample or entry

Old fpga file data



Old fpga file data



Units:

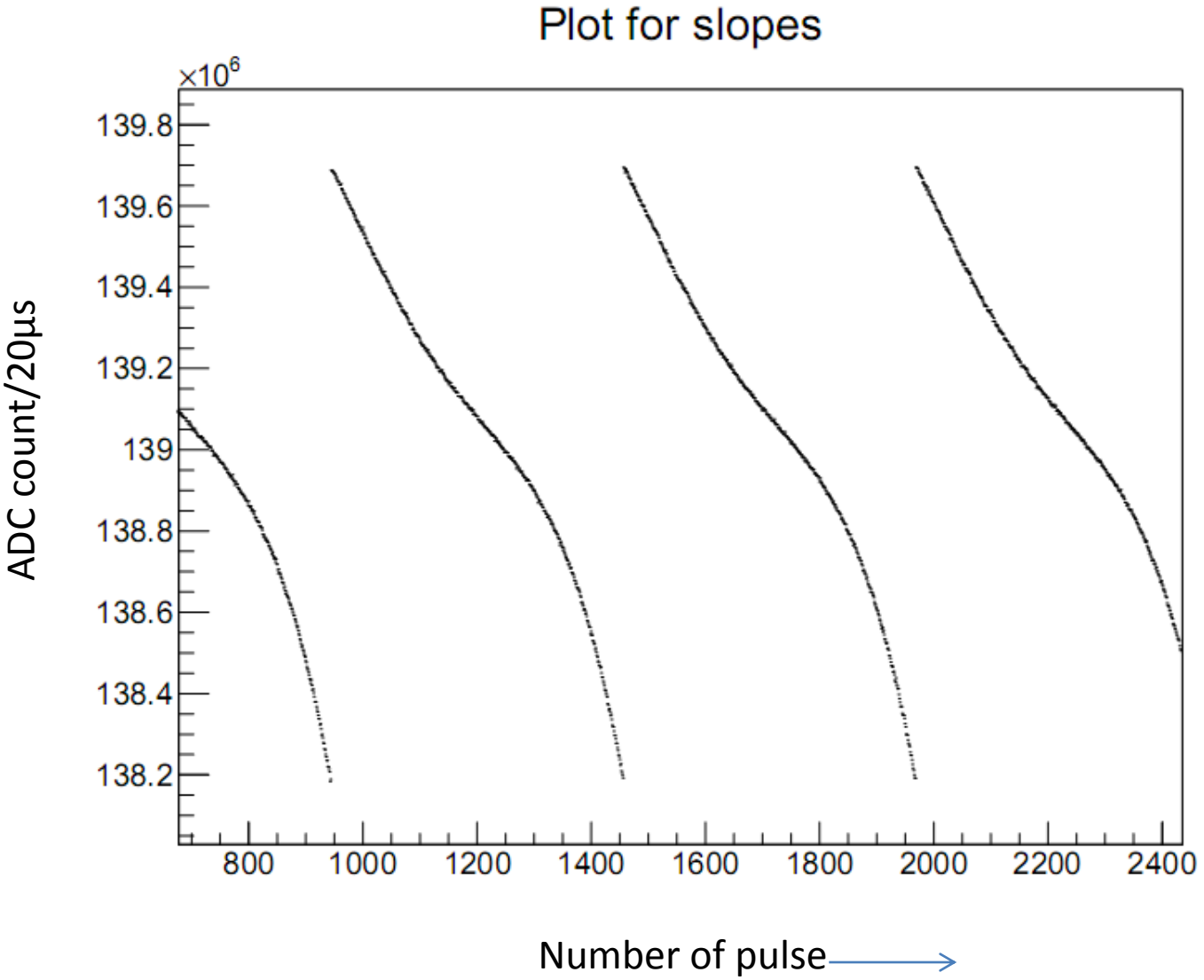
X-axis: 1pulse=700 Entries= 16.66ms (Including idle time) or 14ms (excluding idle time)

Y-axis: ADC count/20µs = ADC count / time equivalent to 1 sample or entry

If we zoom in this part and increase marker size, we get next plot

Old fpga file data

Plot for Slopes (Zoomed version of previous plot)



Units:

X-axis: 1pulse=700 Entries= 16.66ms (Including idle time) or 14ms (excluding idle time)

Y-axis: ADC count/20µs = ADC count / time equivalent to 1 sample or entry