# Resynchronization Test with Updated fpga file

## **Run Configuration:**

1. ADC running at 50 KHz, Hi Resolution Mode, Resynchronized Repeating Gate Mode(SRTM)

- 1. Gate Length = 700 entries (actually 664 entries),
- 2. Triggered on rising edge
- 3. External trigger = 60 Hz i.e. every 16.66 ms
- 4. Signal Analyzed (on channel-1) : 60 Hz pulse with ramp which has Width: 320 μs Leading edge: 100 μs Tailing edge: 100 μs
- 5. Data file size: 18387828736 Byte
- 6. Duration of run: 30 minutes of data

# The Algorithm:

- Each rising edge of the pulse(5 points in the middle of rising edge) is fitted to the linear equation y=ax+b using least square method.
  This gives x-intercept and the slope of the rising edge.
- For each fit ,the x-value for the header is subtracted from the X-intercept of the rising edge.



Units: X-axis: 1 Entry= 1 Sample= 1/50KHz =  $20\mu$ s Y-axis: 1 ADC count= 20Volt  $/2^{32}$  =  $4.656 \times 10^{-09}$  Volt This constitute:

 $\Delta t=t_i-t_0$ Where,  $t_i=$ Intercept from fit  $t_0=x$ -value for header

- 3. This is done for all the pulses.
- Δt vs Pulse number is plotted.
- 5. Slope vs pulse number is plotted.
- A histogram for all the Δt is drawn.





### Plot for intercepts



Units:

Plot for Intercepts (Zoomed version of previous plot)



to 1 sample or entry



Histogram for intercept in Log scale





Units:

### Plot for Slopes (Zoomed version of previous plot) Plot for slopes



Units:

X-axis: 1pulse=700 Entries= 16.66ms (Including idle time) or 14ms (excluding idle time) Y-axis: ADC count/20 $\mu$ s = ADC count / time equivalent to 1 sample or entry

The following three slides are same analysis but with smaller data set (10 minutes)







X-axis: fraction 1 Entry=frac of 1 Sample=frac of 1/50KHz =frac of 20 $\mu$ s



X-axis: 1 Entry= 1 Sample= 1/50KHz = 20µs