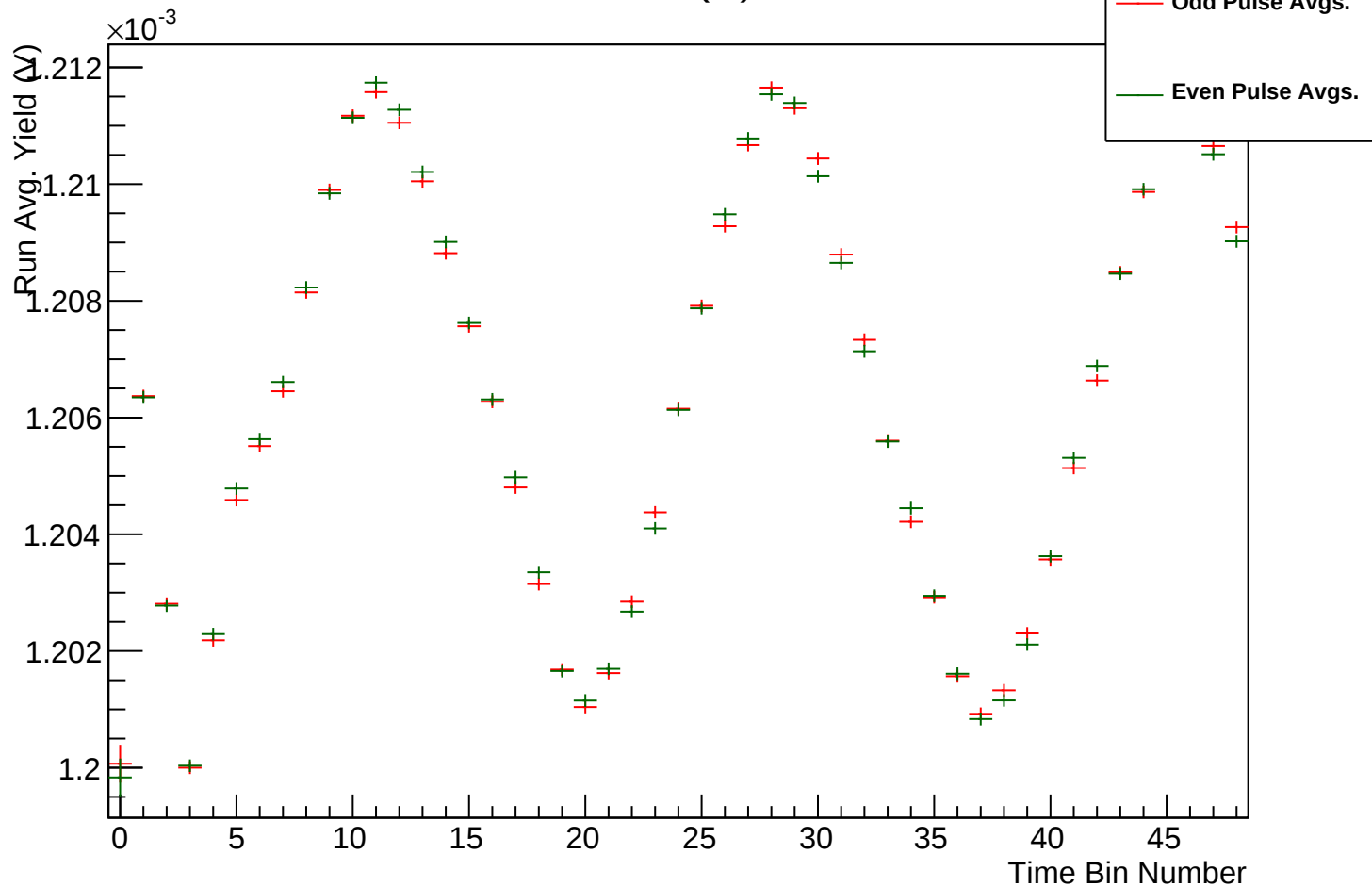
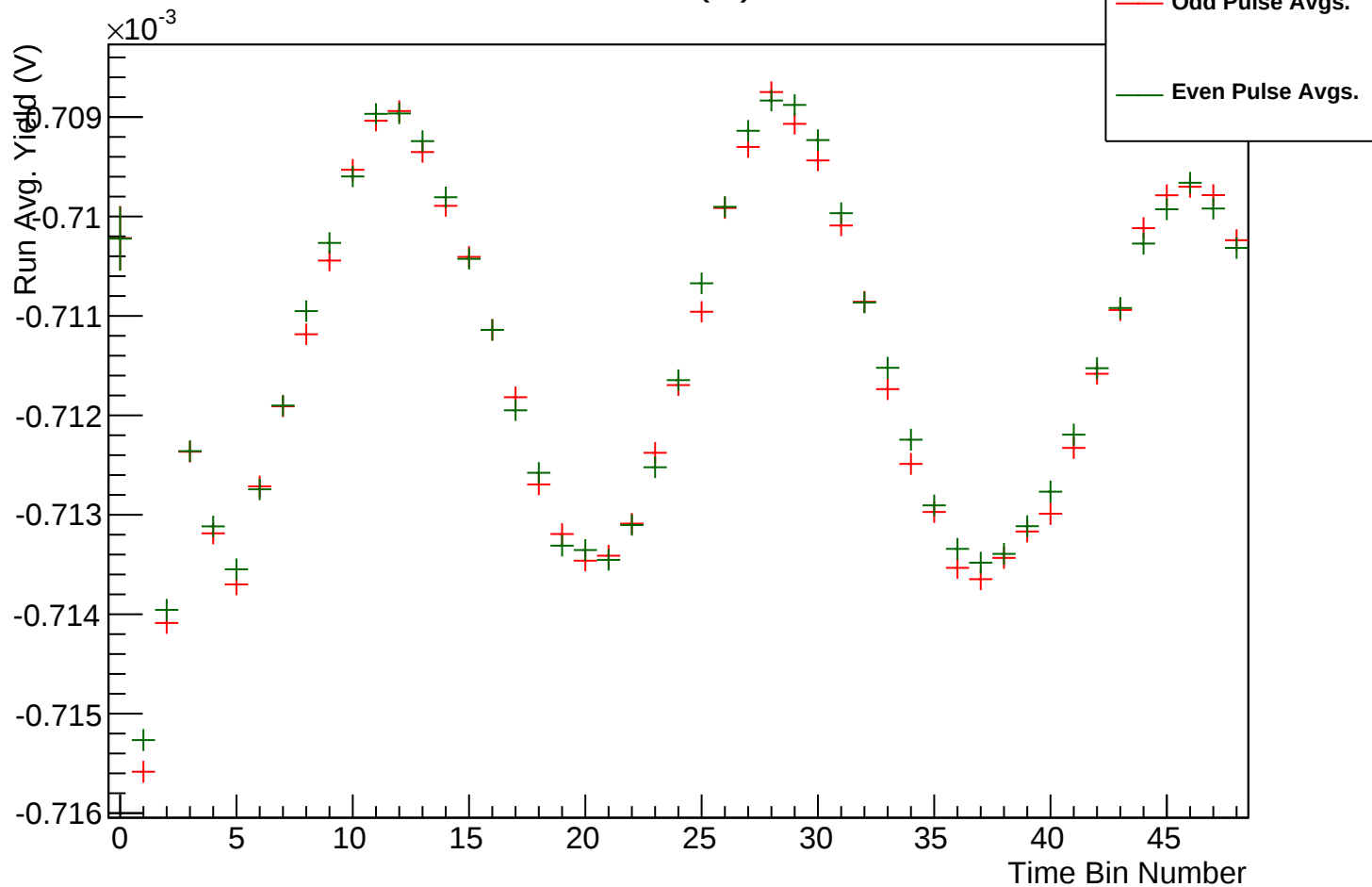


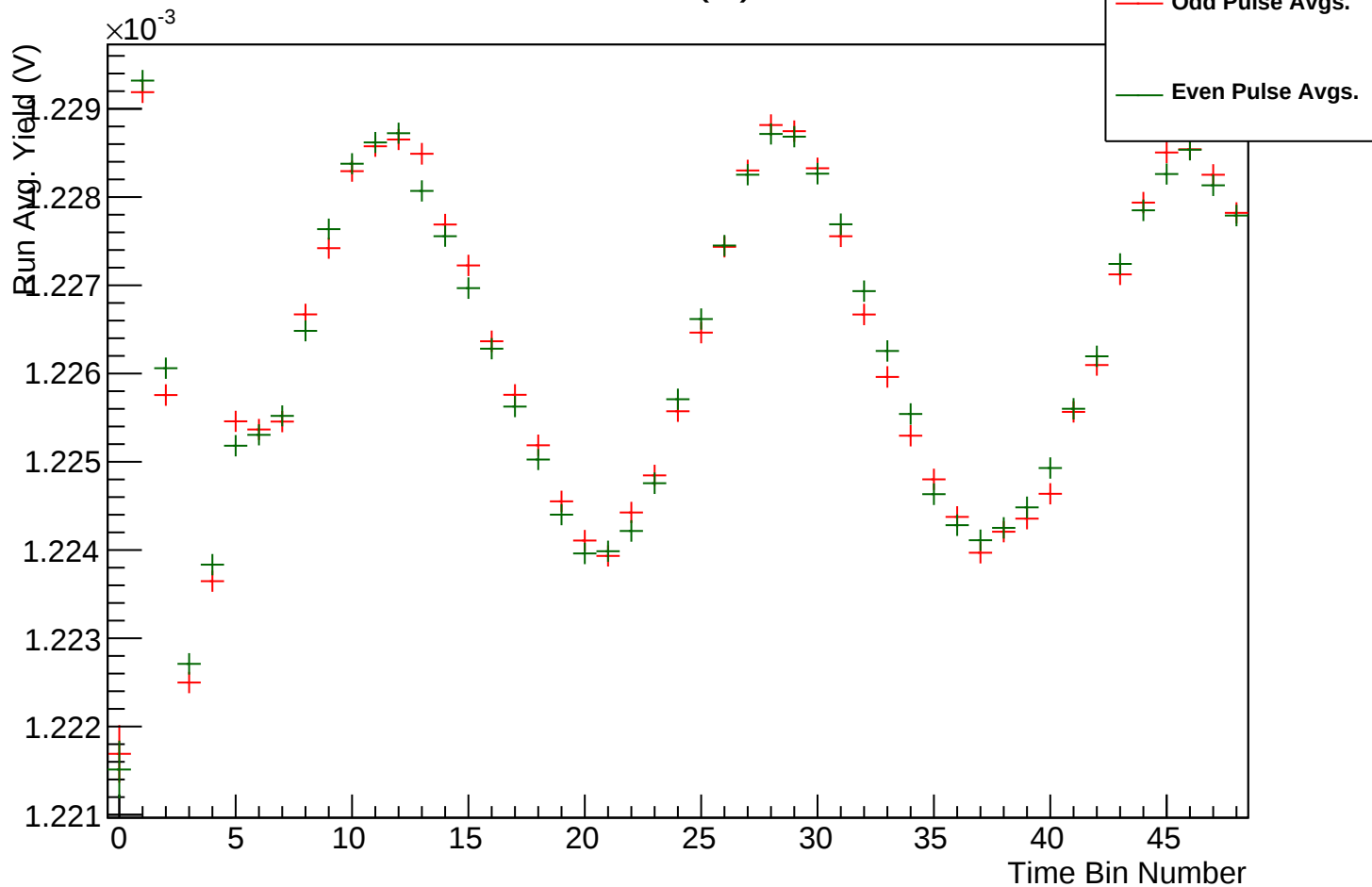
r17784-w0-Yield(V)-OddPulses



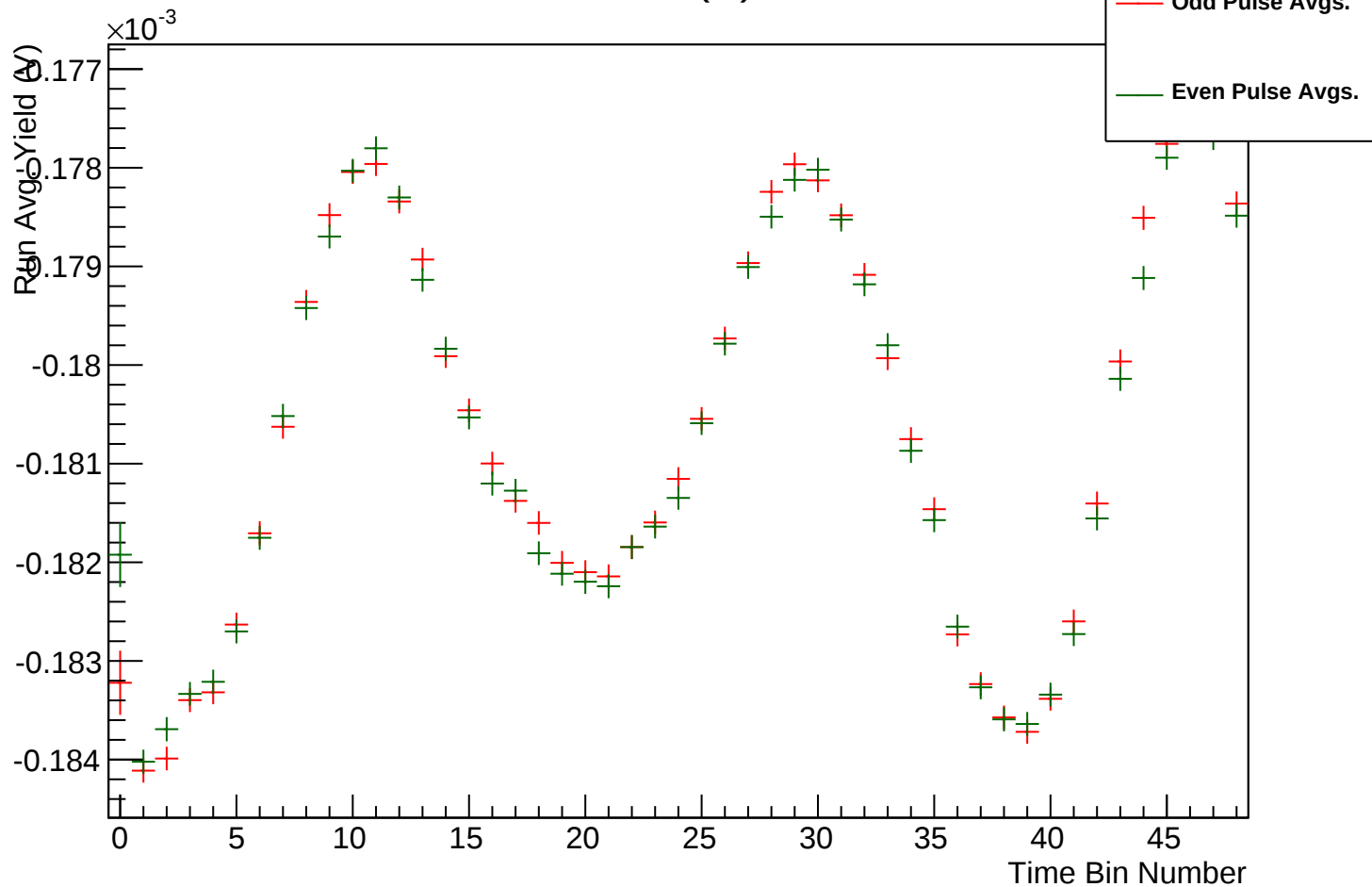
r17784-w1-Yield(V)-OddPulses



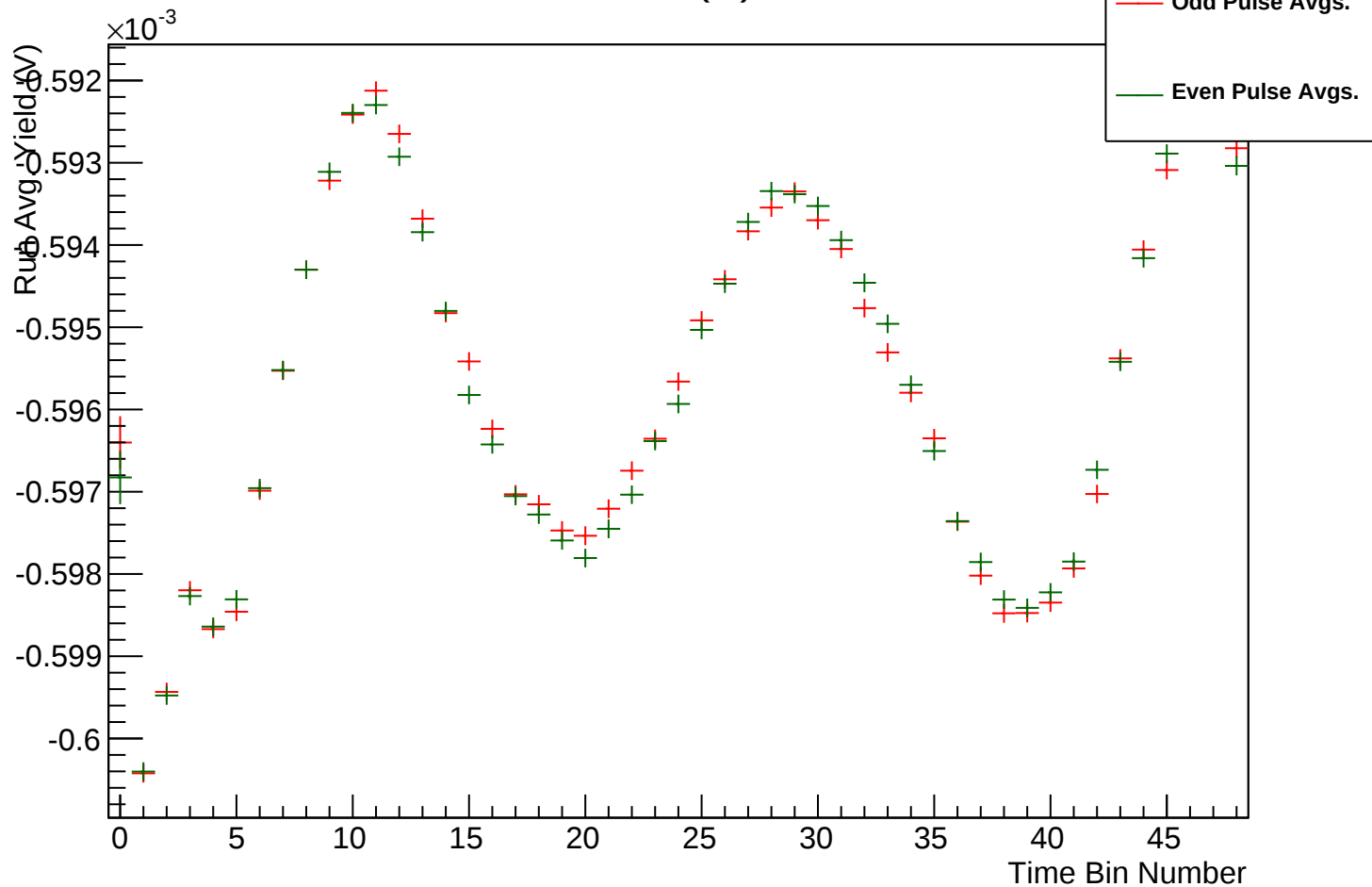
r17784-w2-Yield(V)-OddPulses



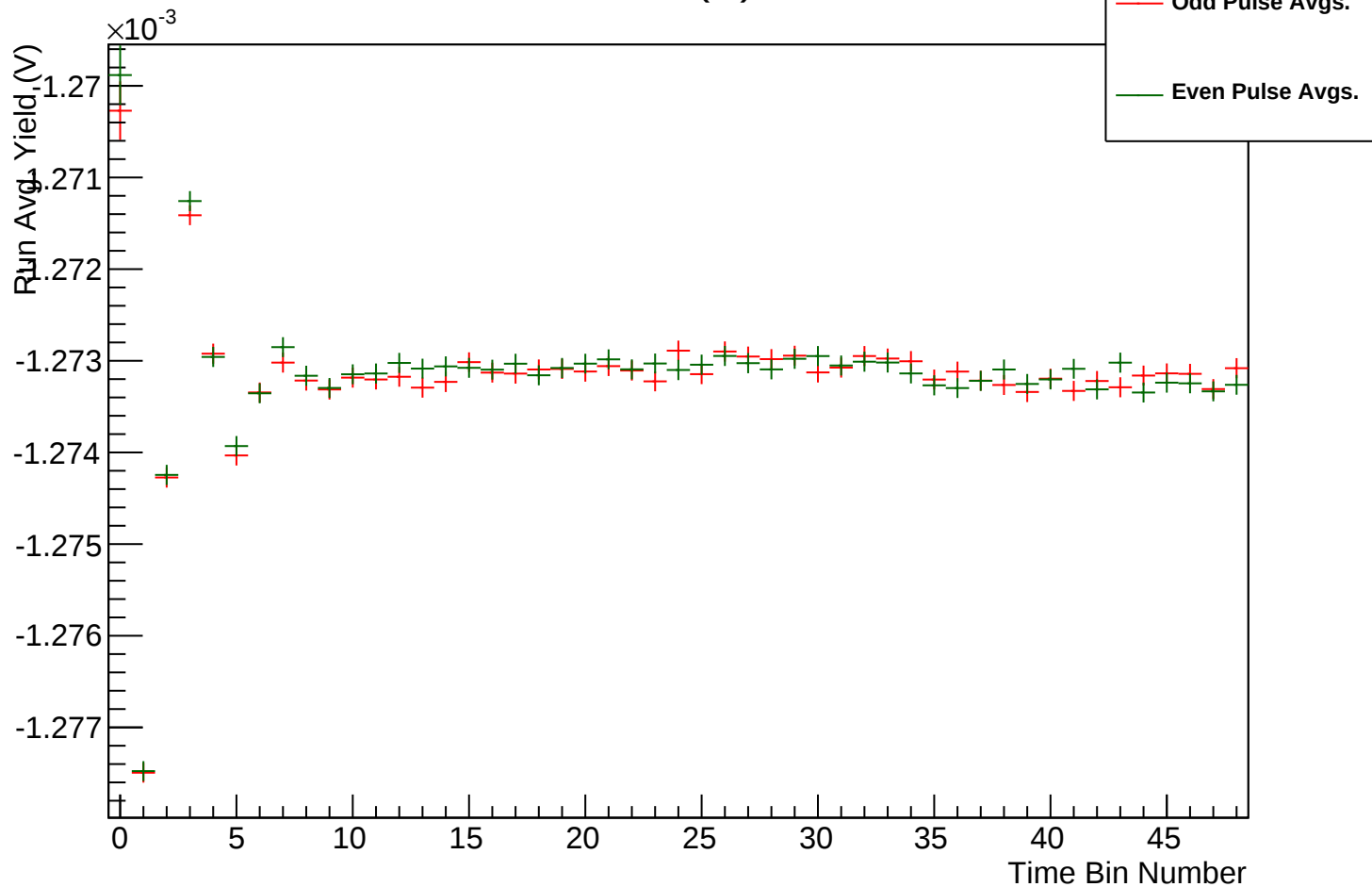
r17784-w3-Yield(V)-OddPulses



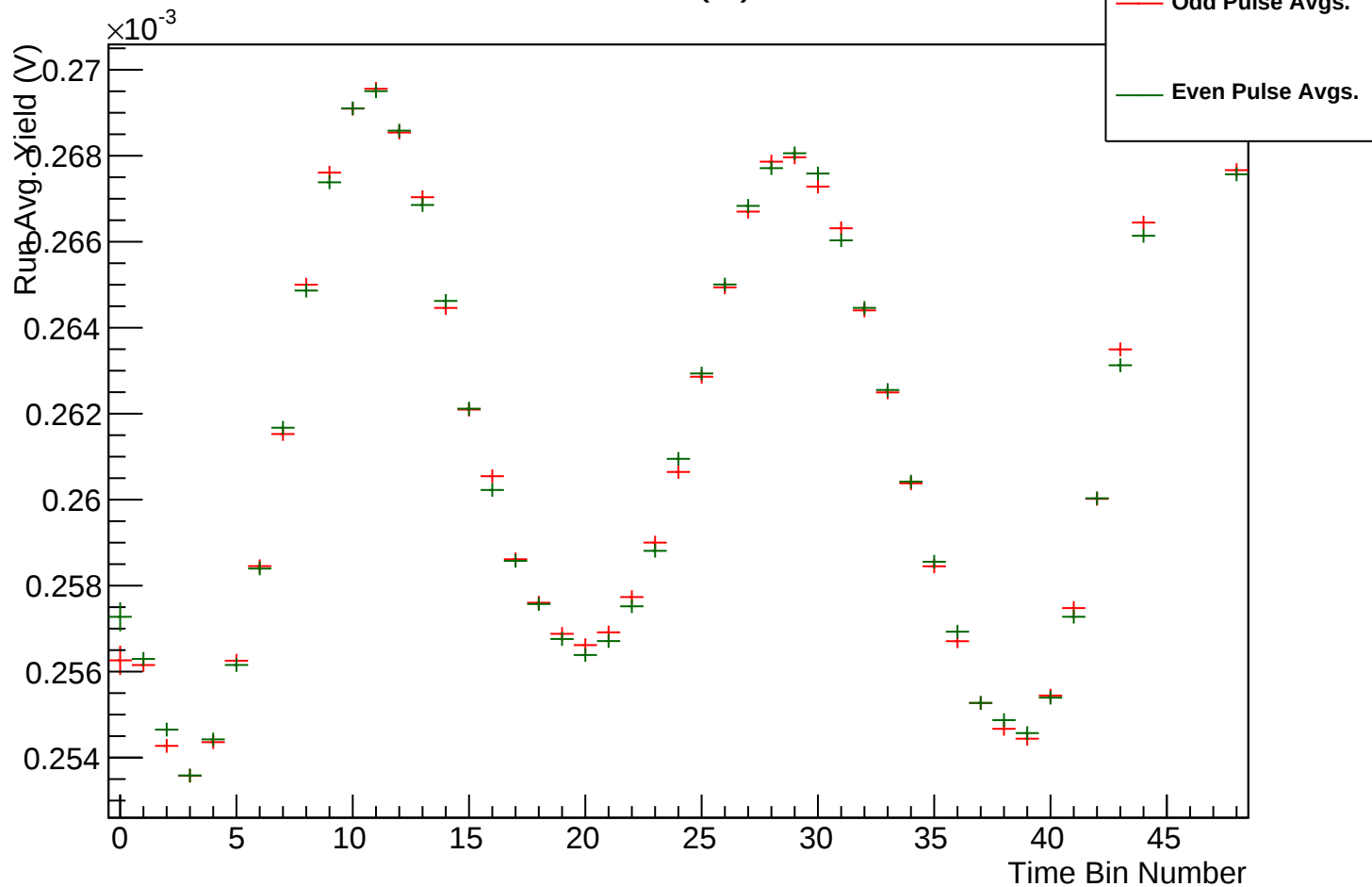
r17784-w4-Yield(V)-OddPulses



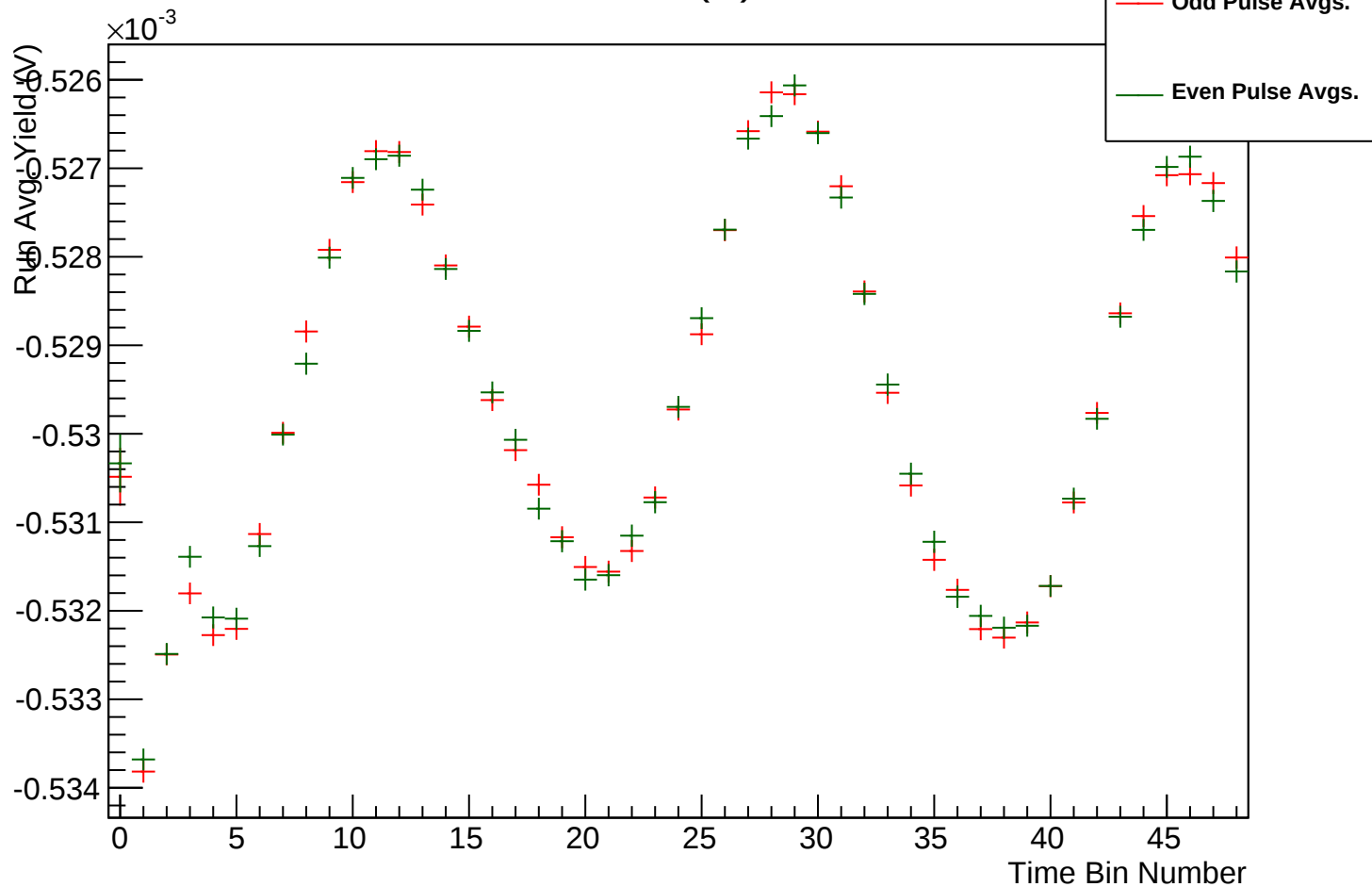
r17784-w5-Yield(V)-OddPulses



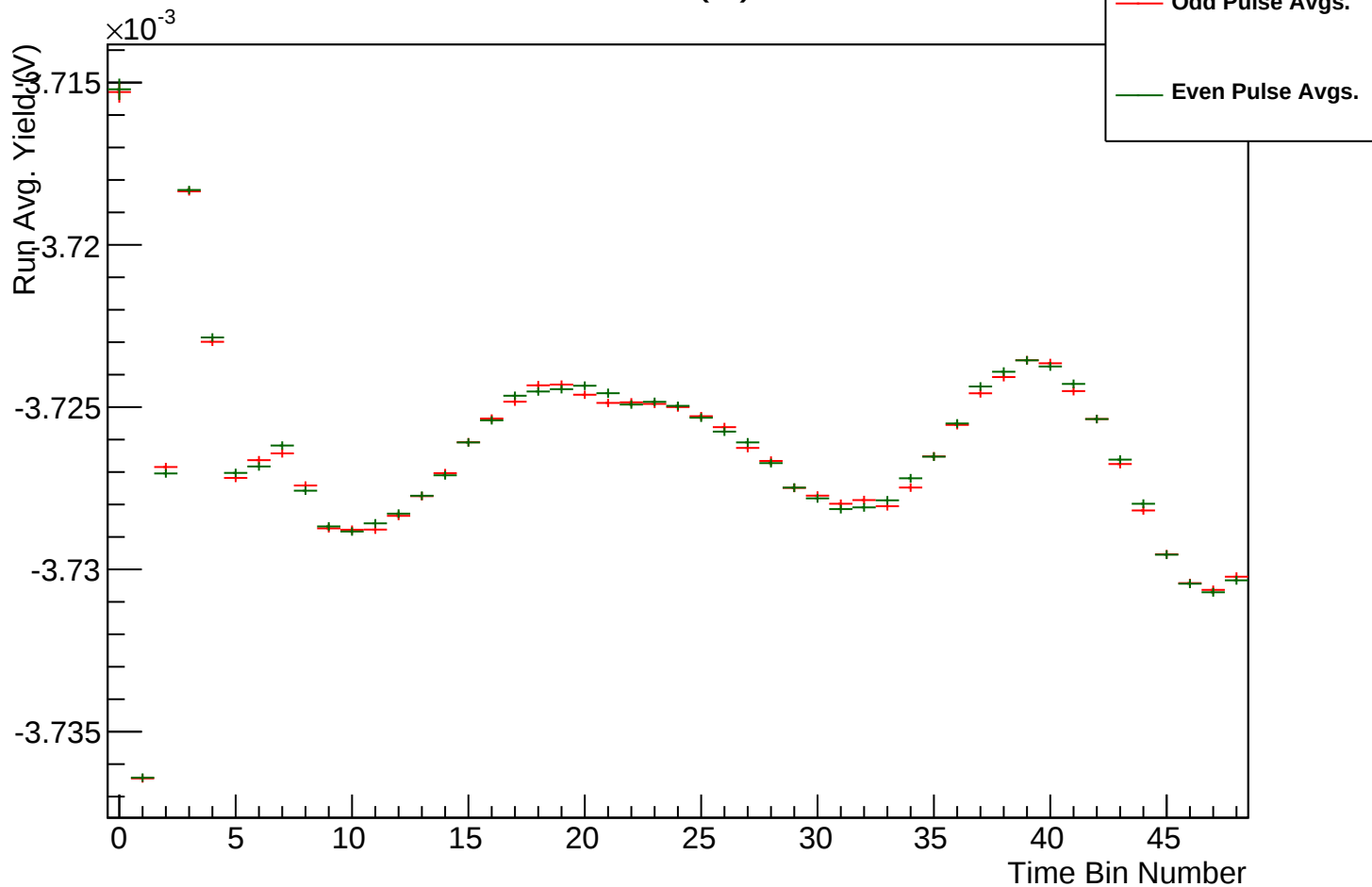
r17784-w6-Yield(V)-OddPulses



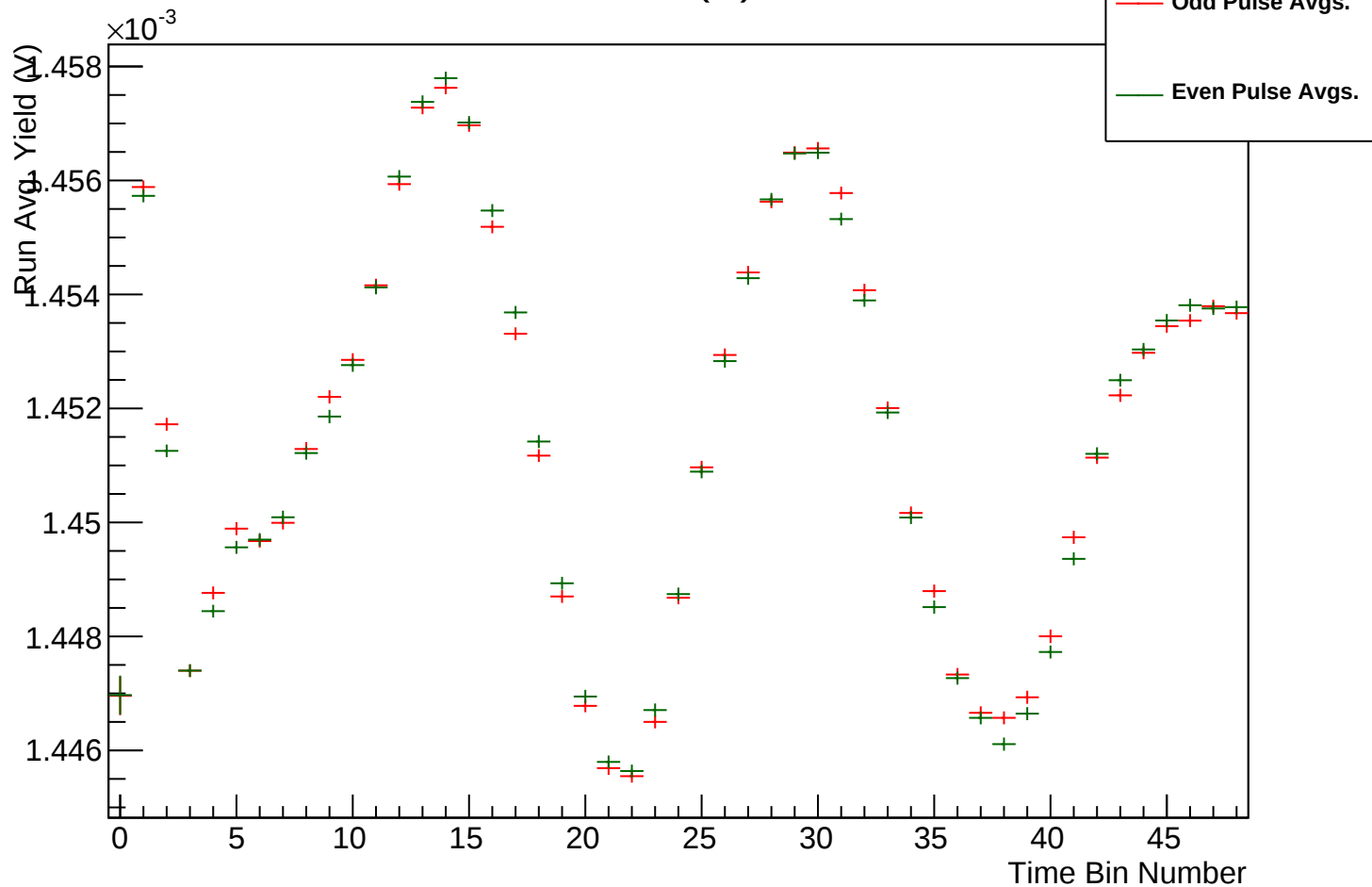
r17784-w7-Yield(V)-OddPulses



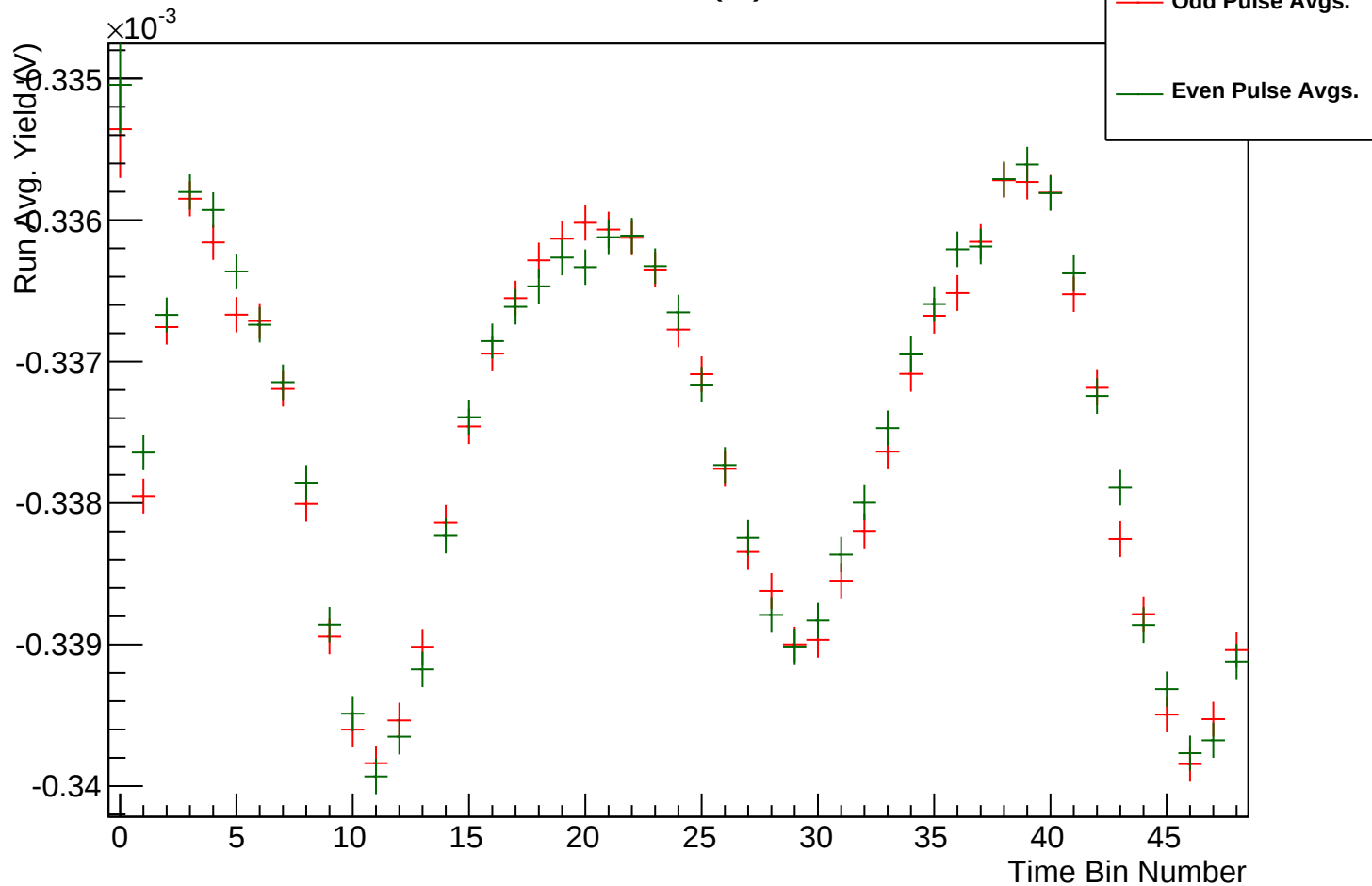
r17784-w8-Yield(V)-OddPulses



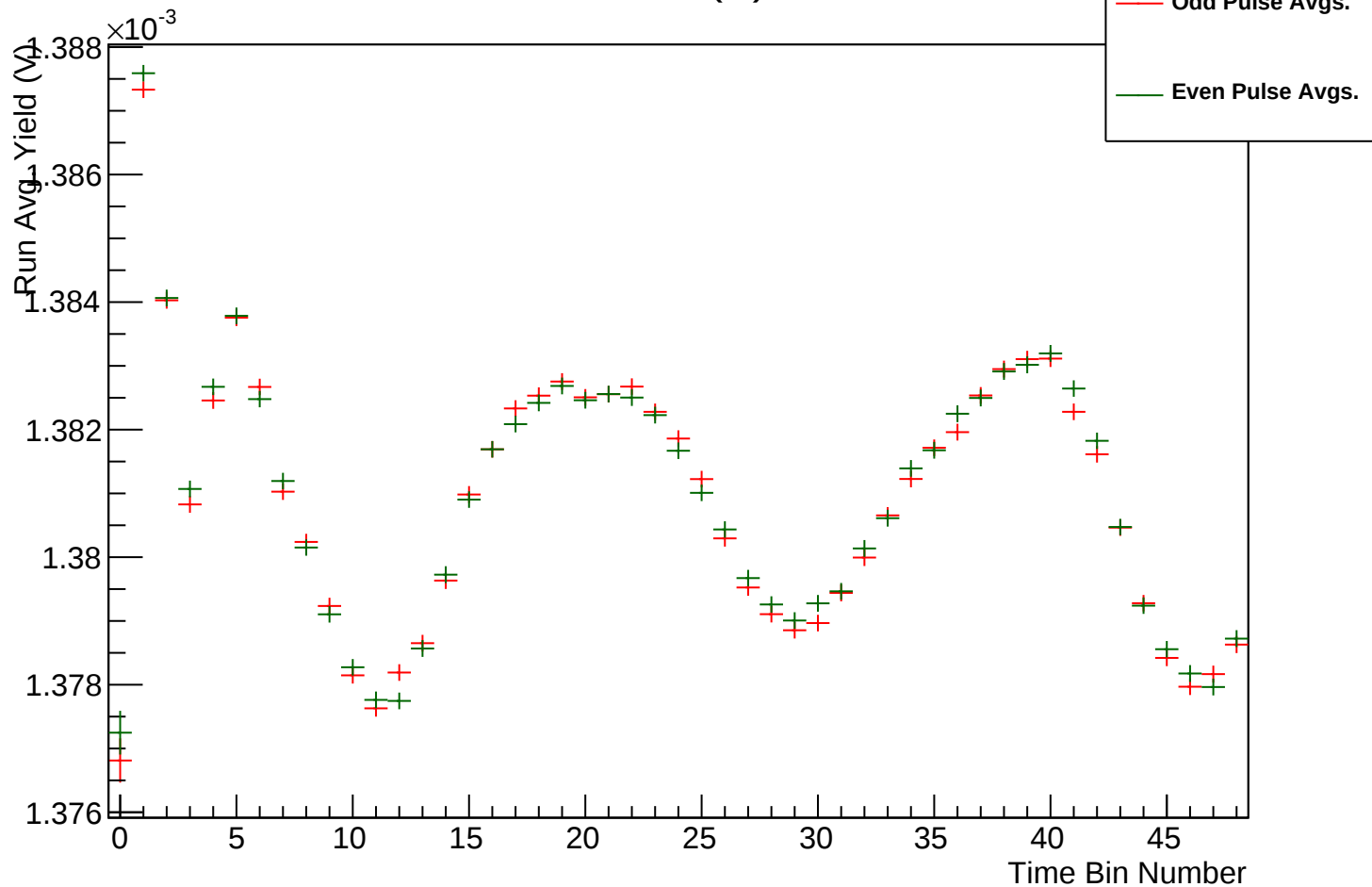
r17784-w9-Yield(V)-OddPulses



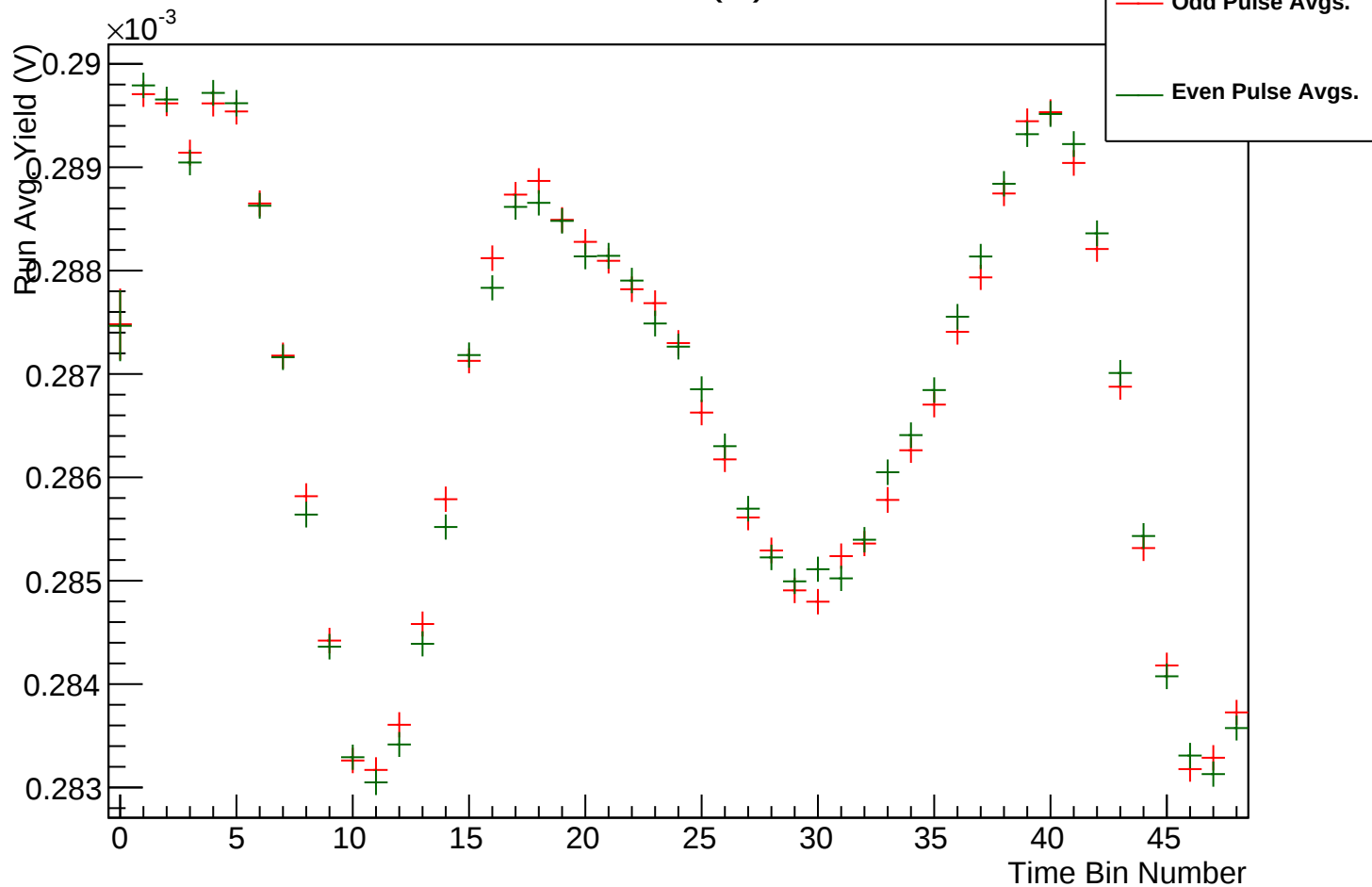
r17784-w10-Yield(V)-OddPulses



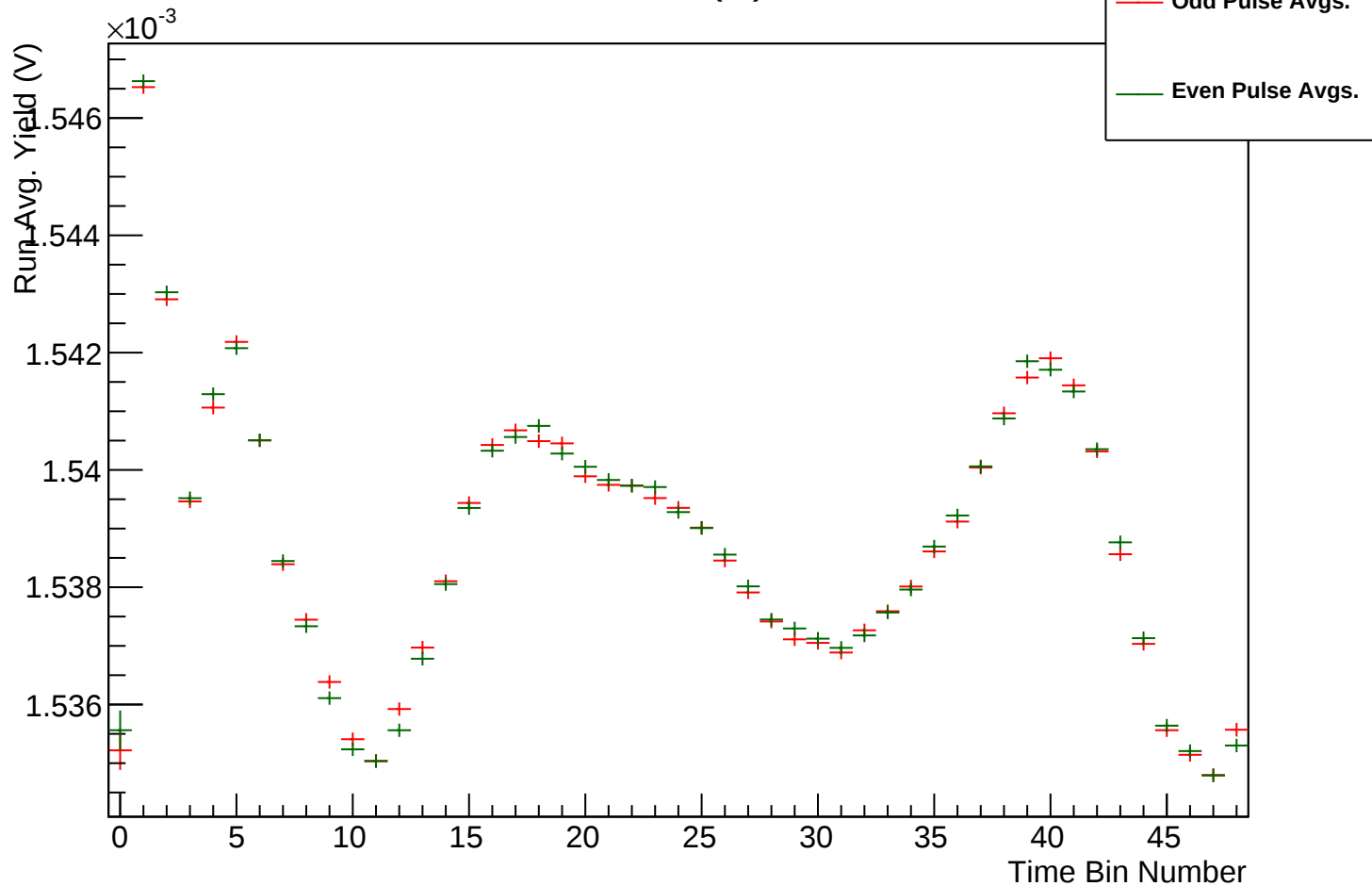
r17784-w11-Yield(V)-OddPulses



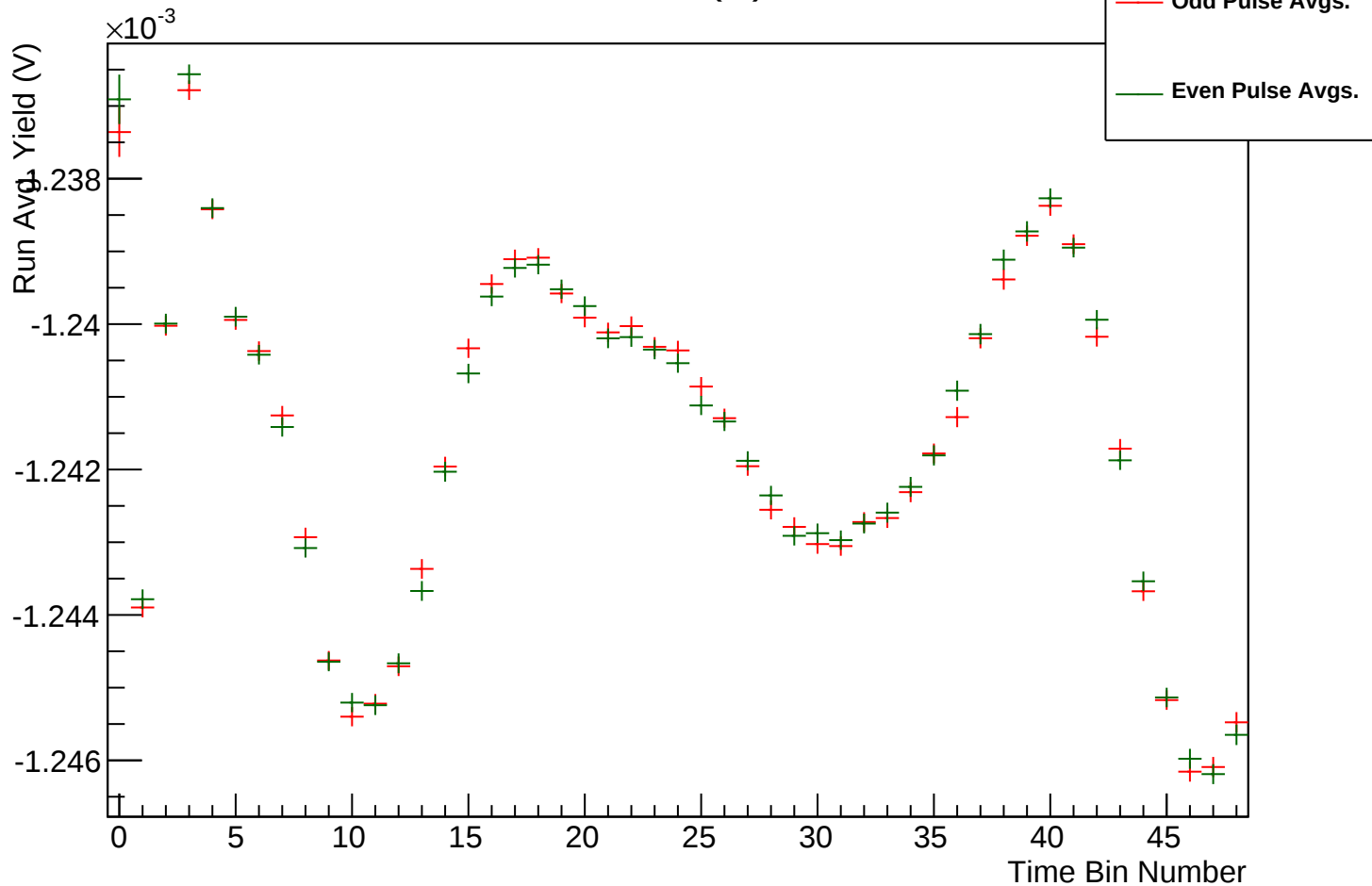
r17784-w12-Yield(V)-OddPulses



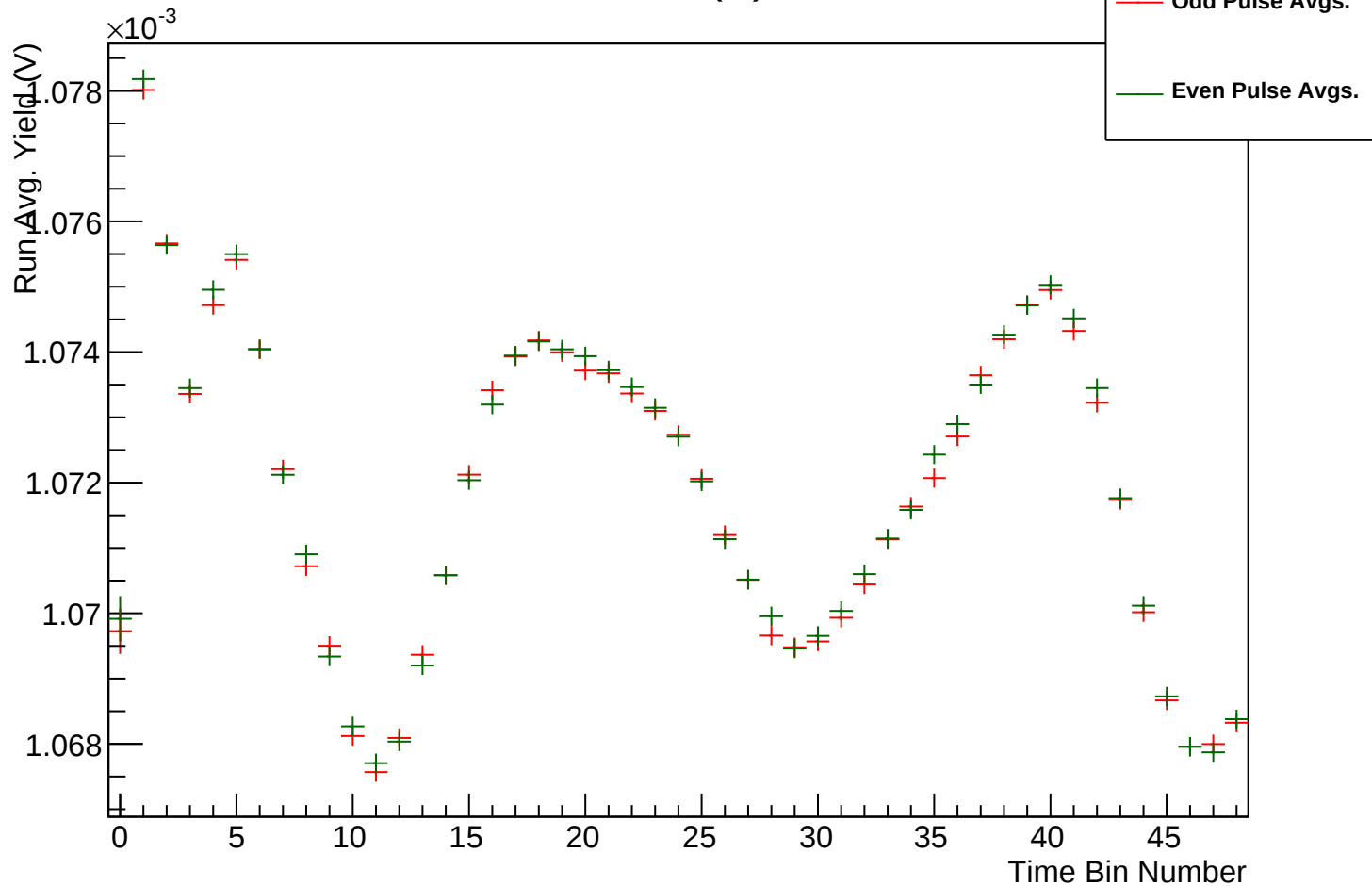
r17784-w13-Yield(V)-OddPulses



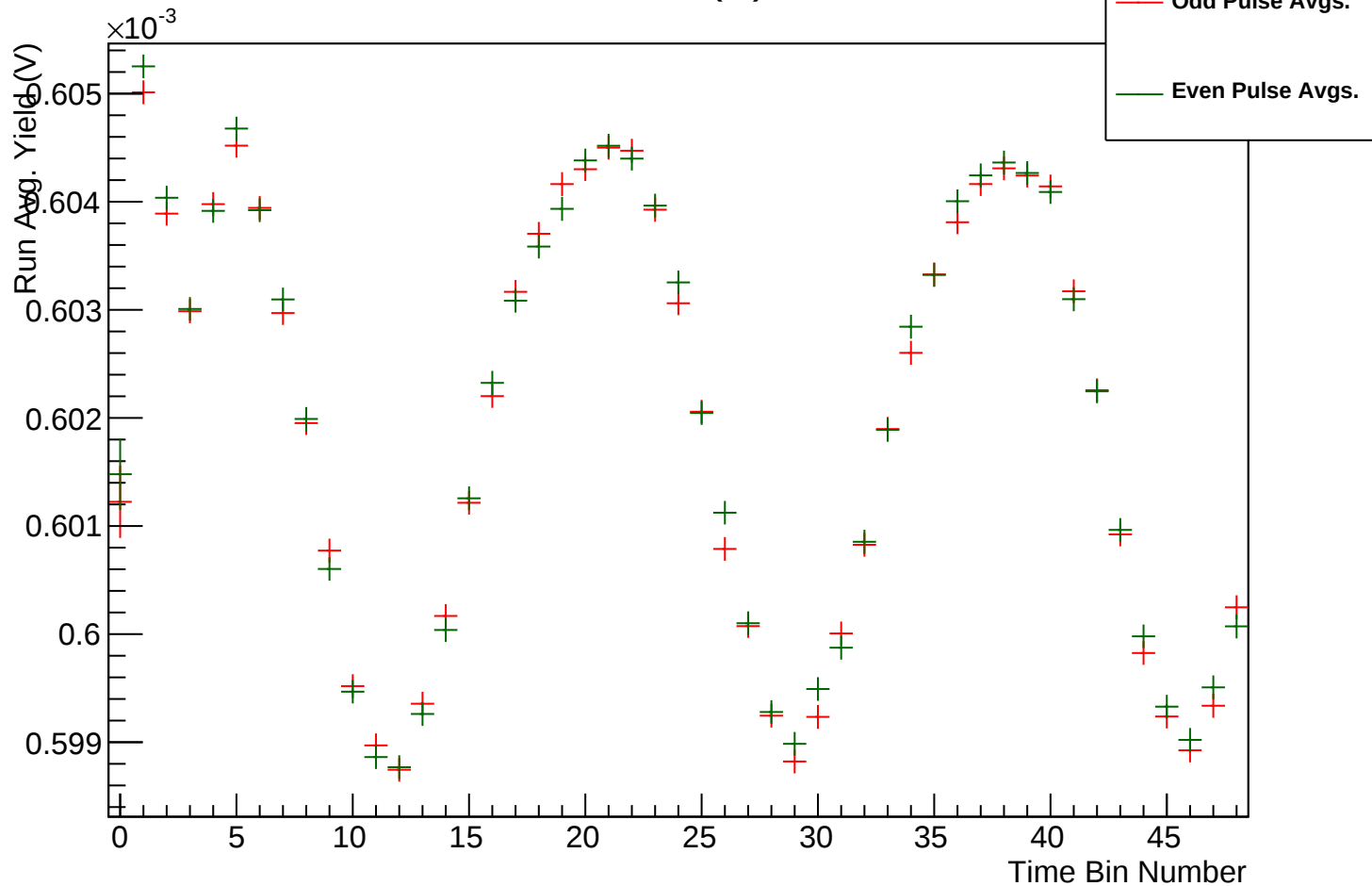
r17784-w14-Yield(V)-OddPulses



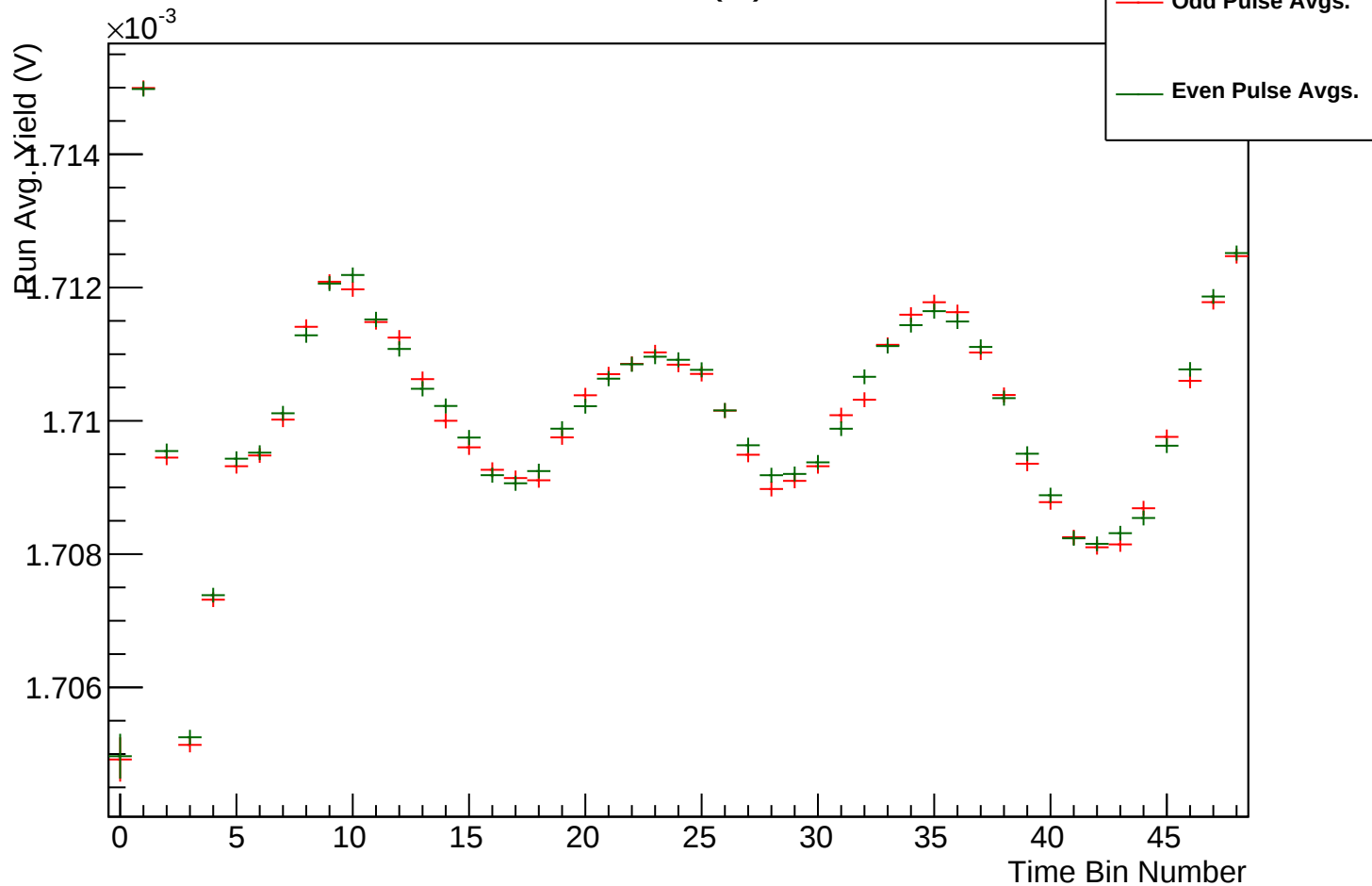
r17784-w15-Yield(V)-OddPulses



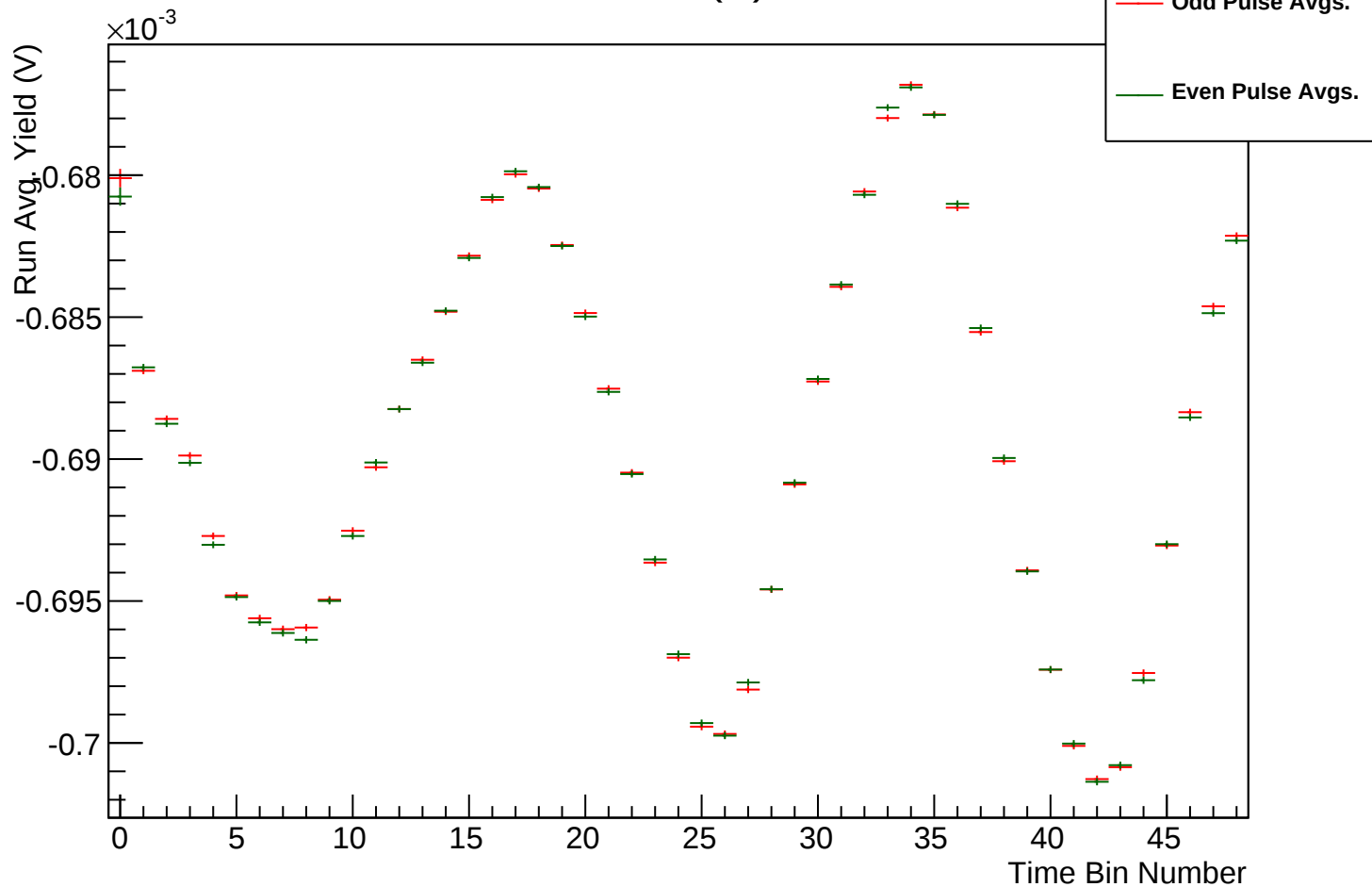
r17784-w16-Yield(V)-OddPulses



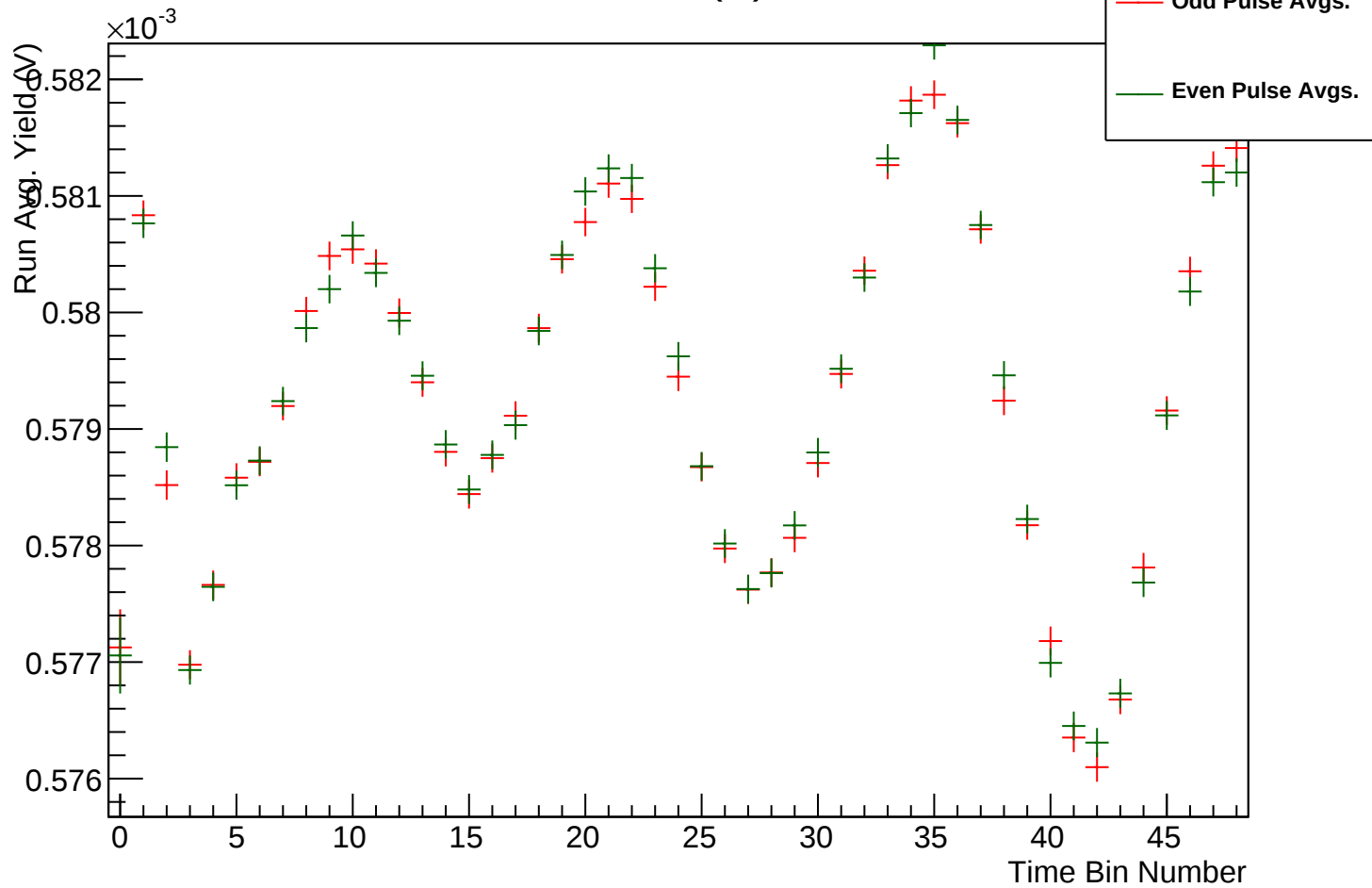
r17784-w17-Yield(V)-OddPulses



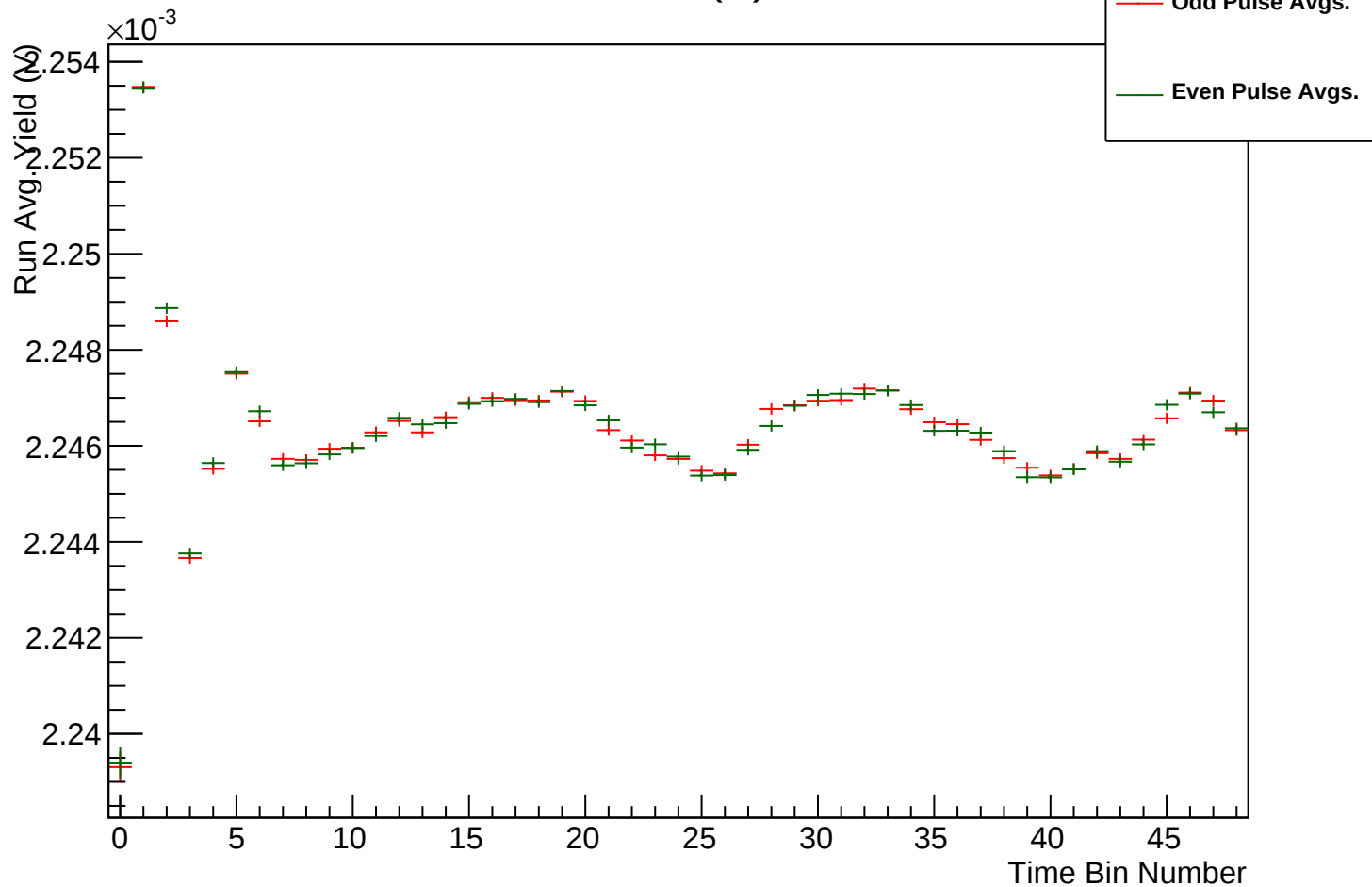
r17784-w18-Yield(V)-OddPulses



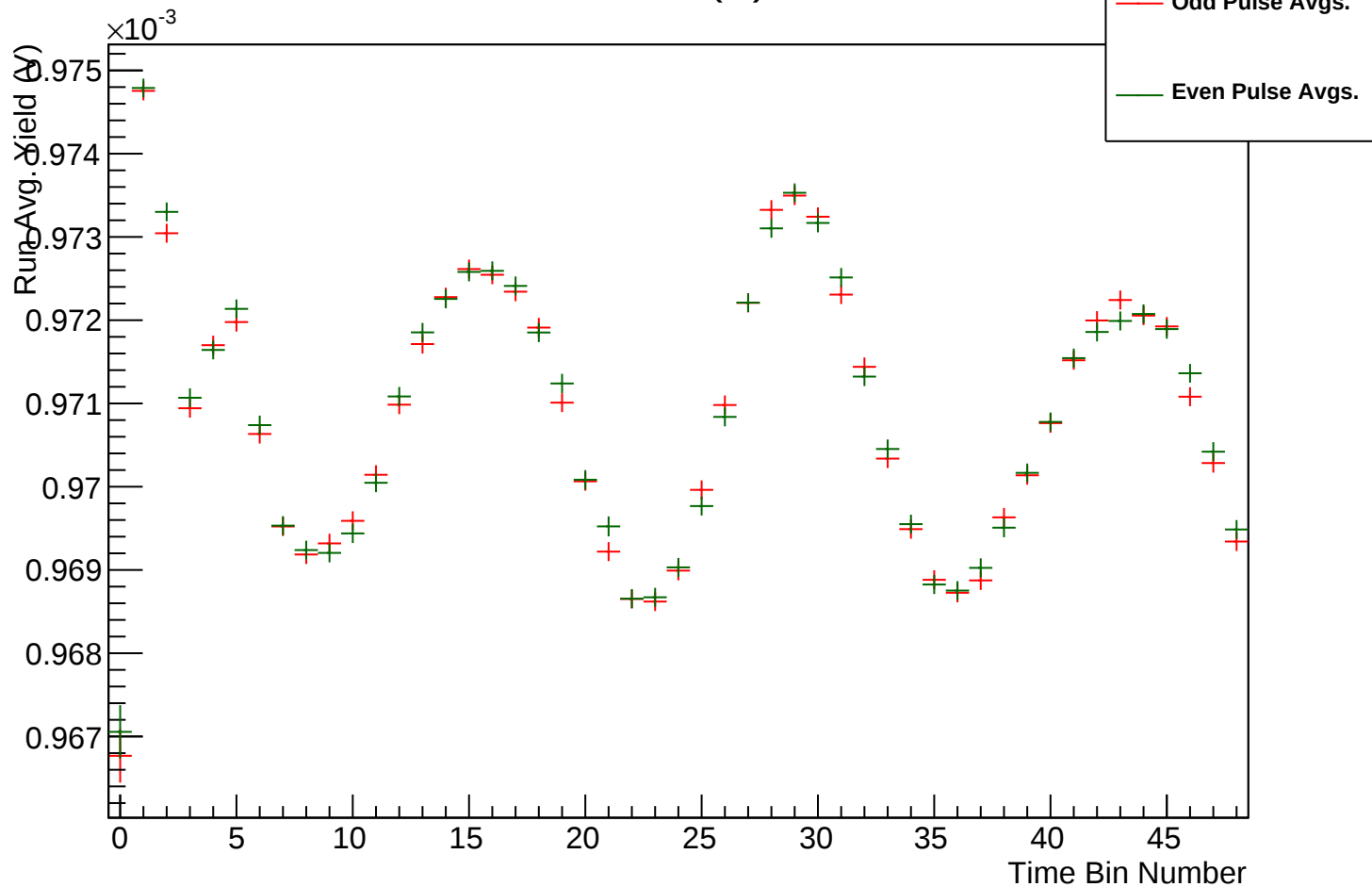
r17784-w19-Yield(V)-OddPulses



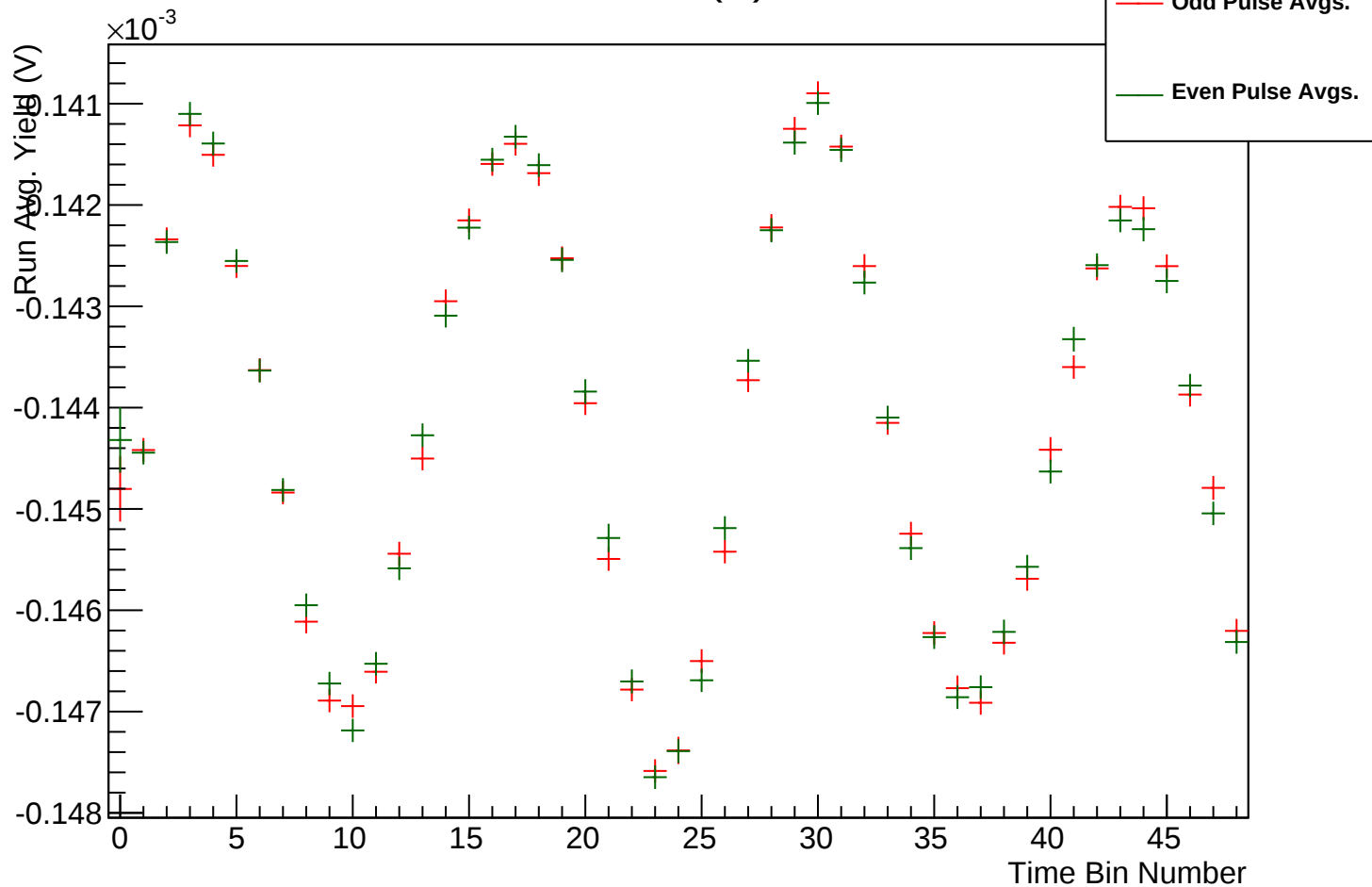
r17784-w20-Yield(V)-OddPulses



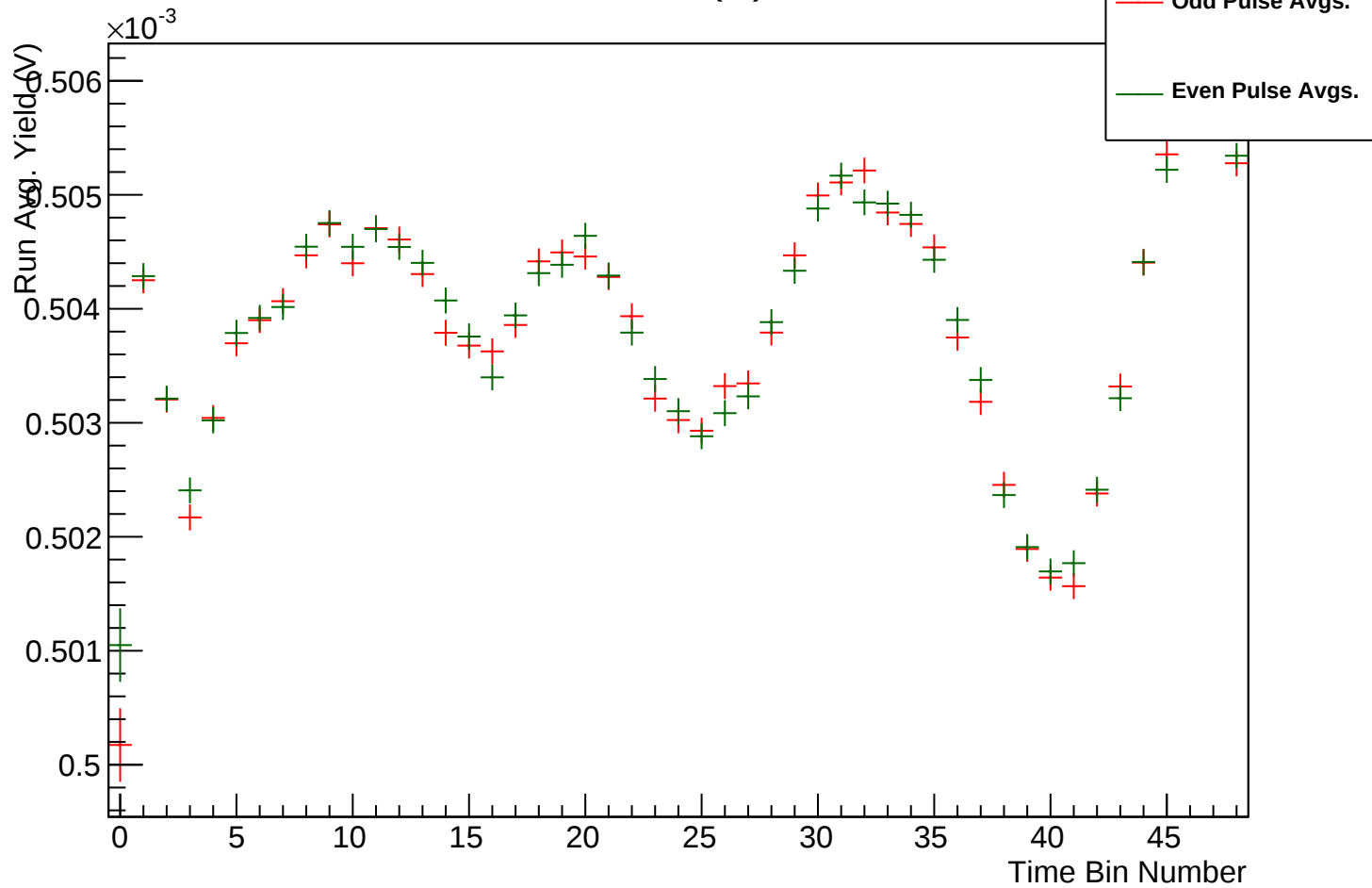
r17784-w21-Yield(V)-OddPulses



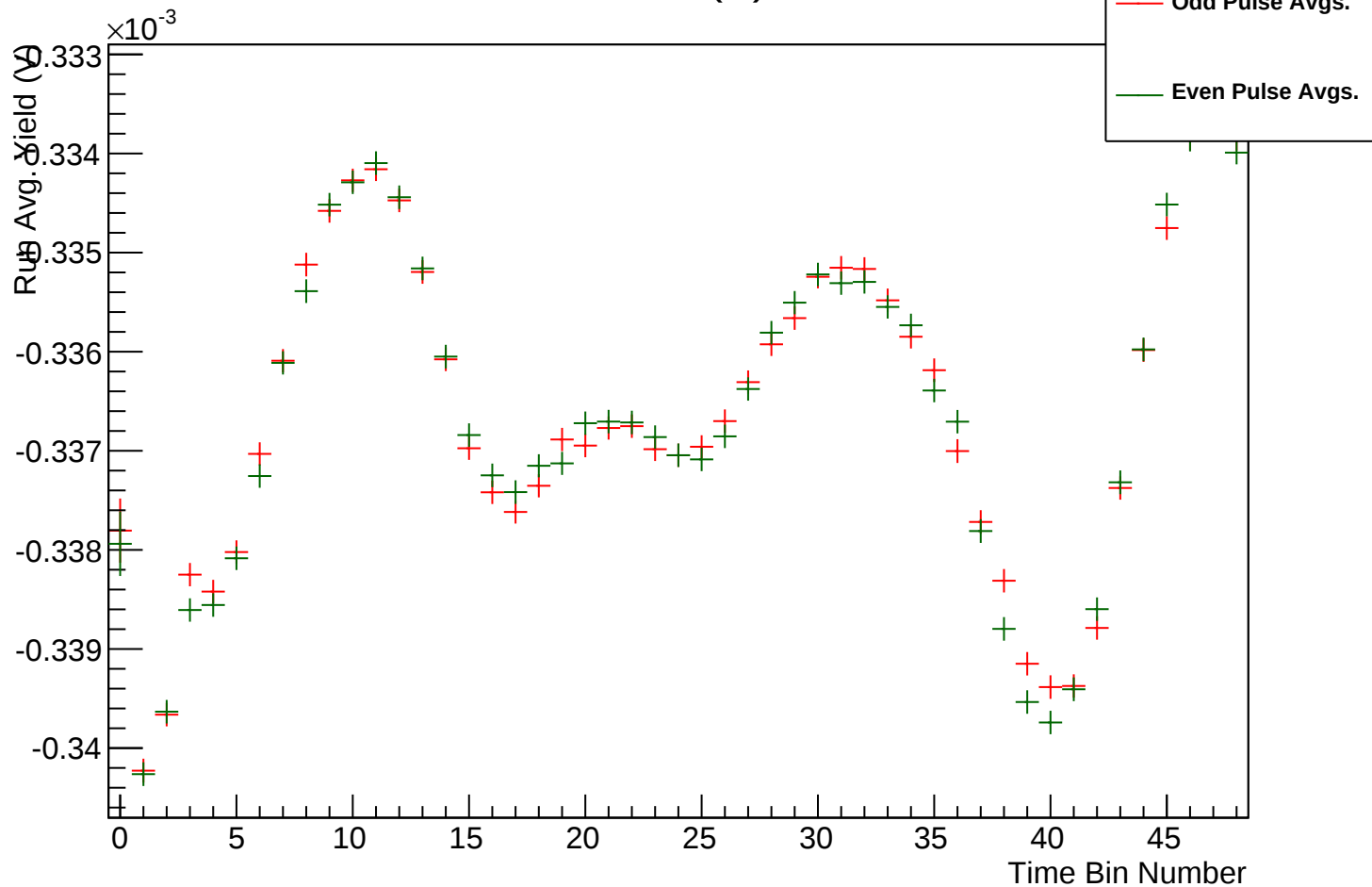
r17784-w22-Yield(V)-OddPulses



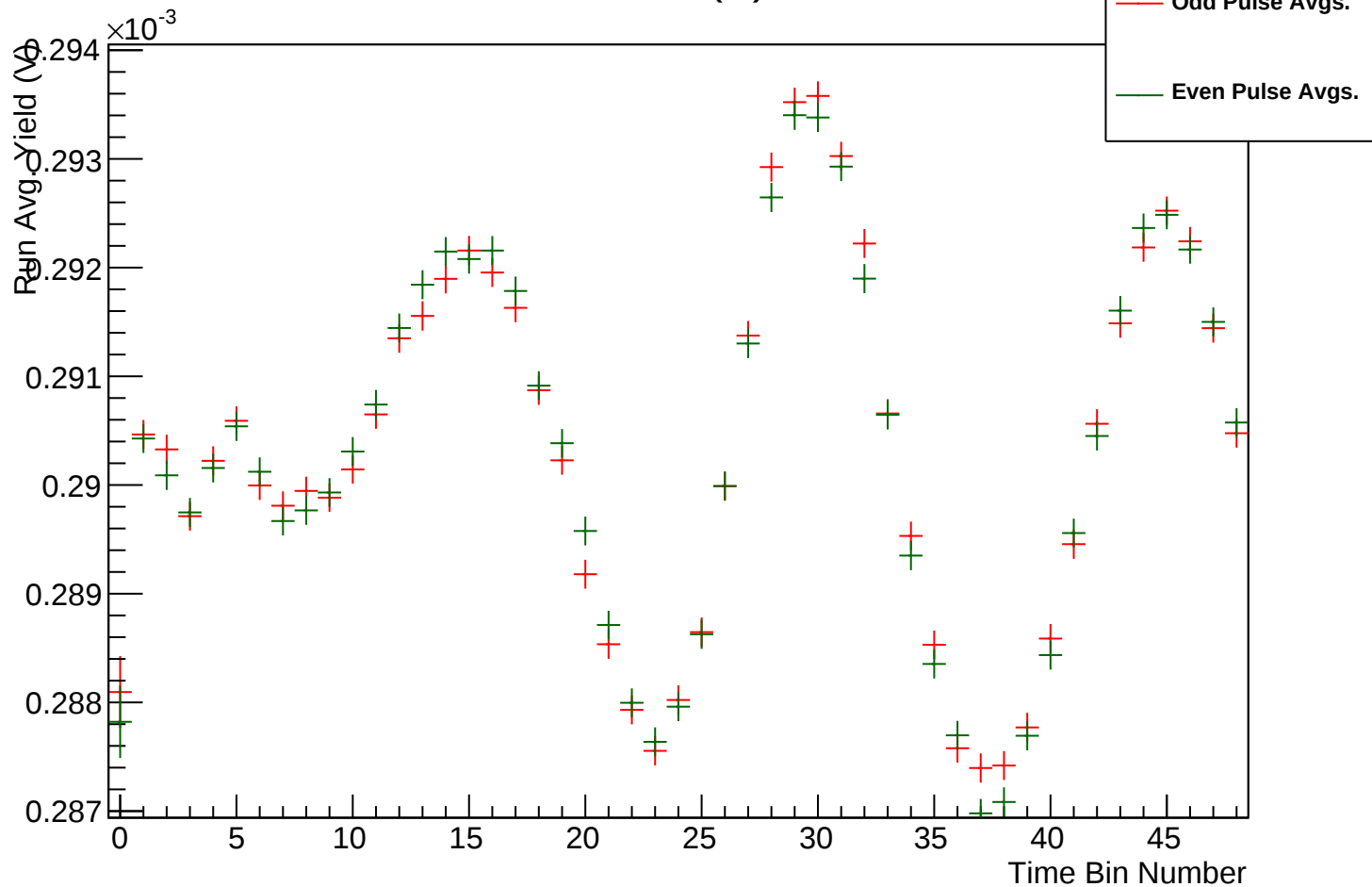
r17784-w23-Yield(V)-OddPulses



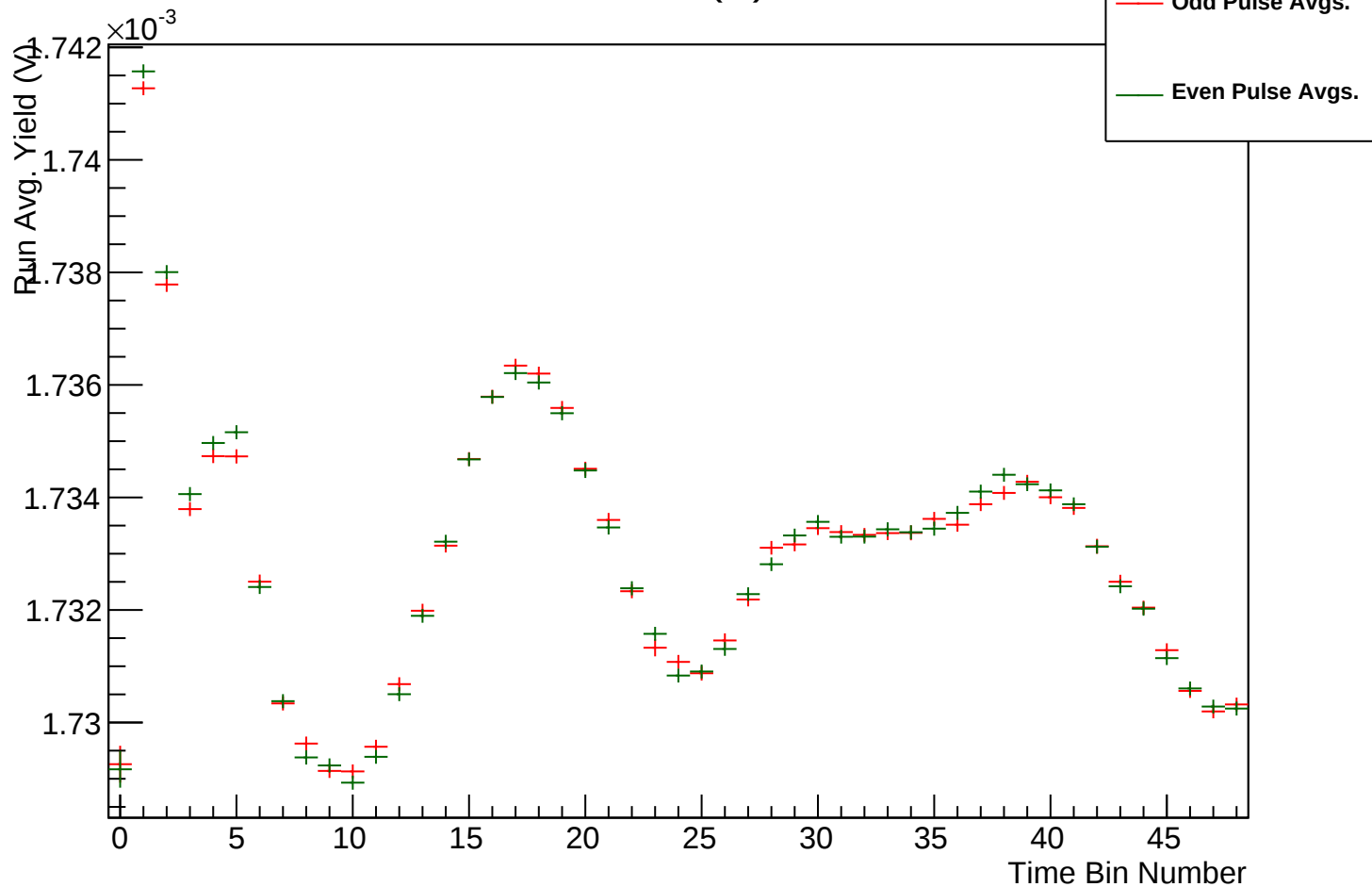
r17784-w24-Yield(V)-OddPulses



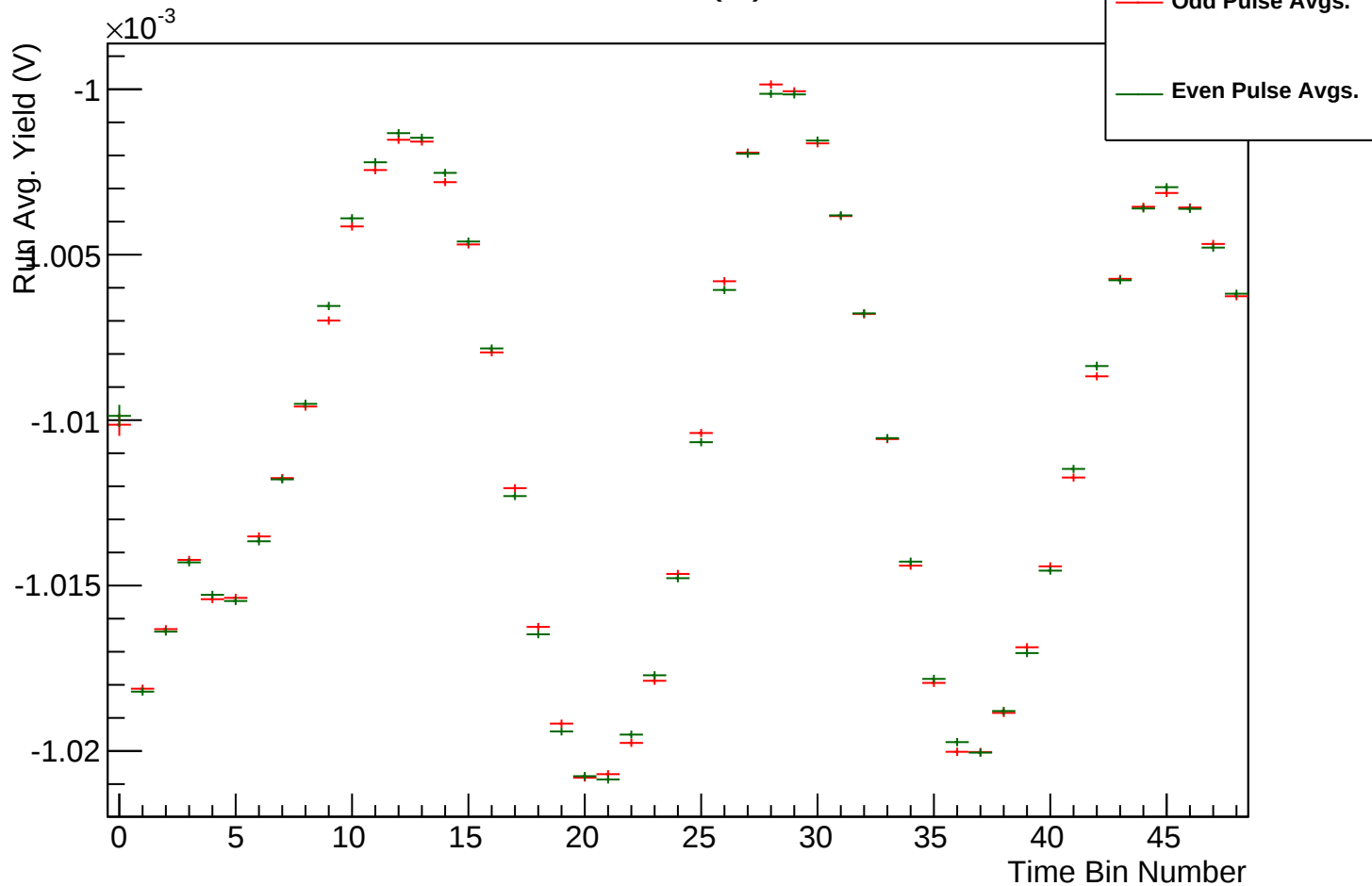
r17784-w25-Yield(V)-OddPulses



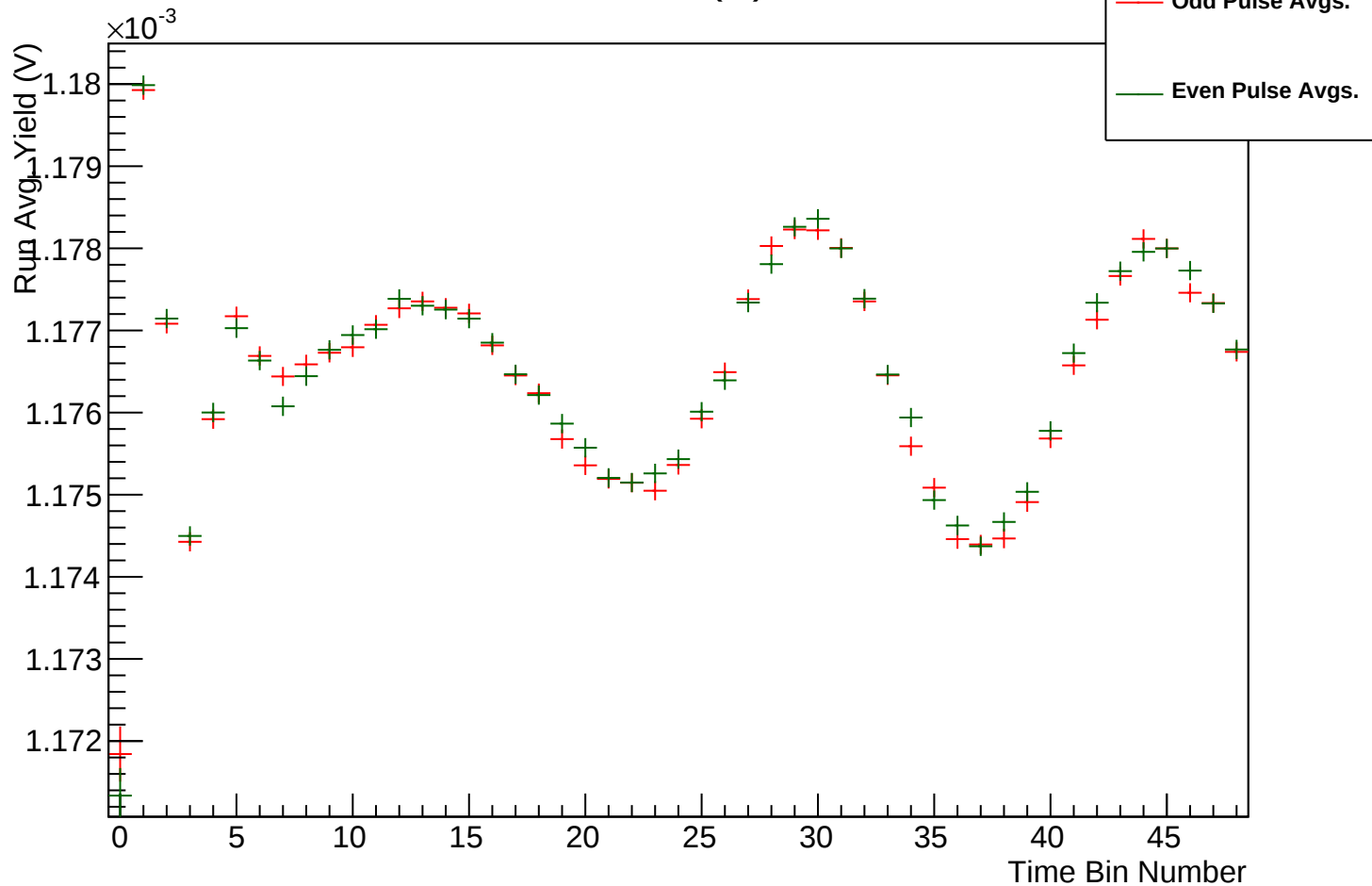
r17784-w26-Yield(V)-OddPulses



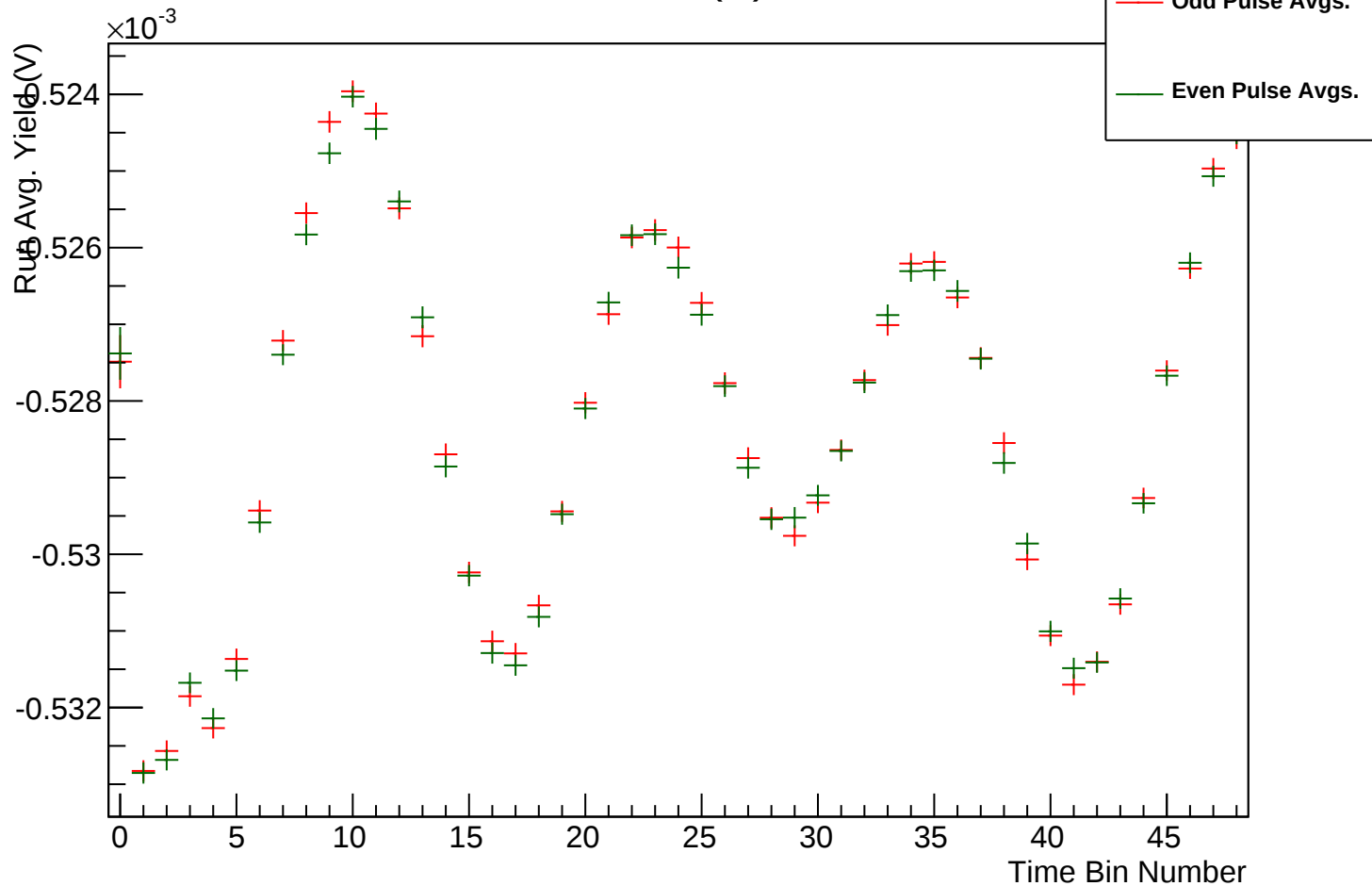
r17784-w27-Yield(V)-OddPulses



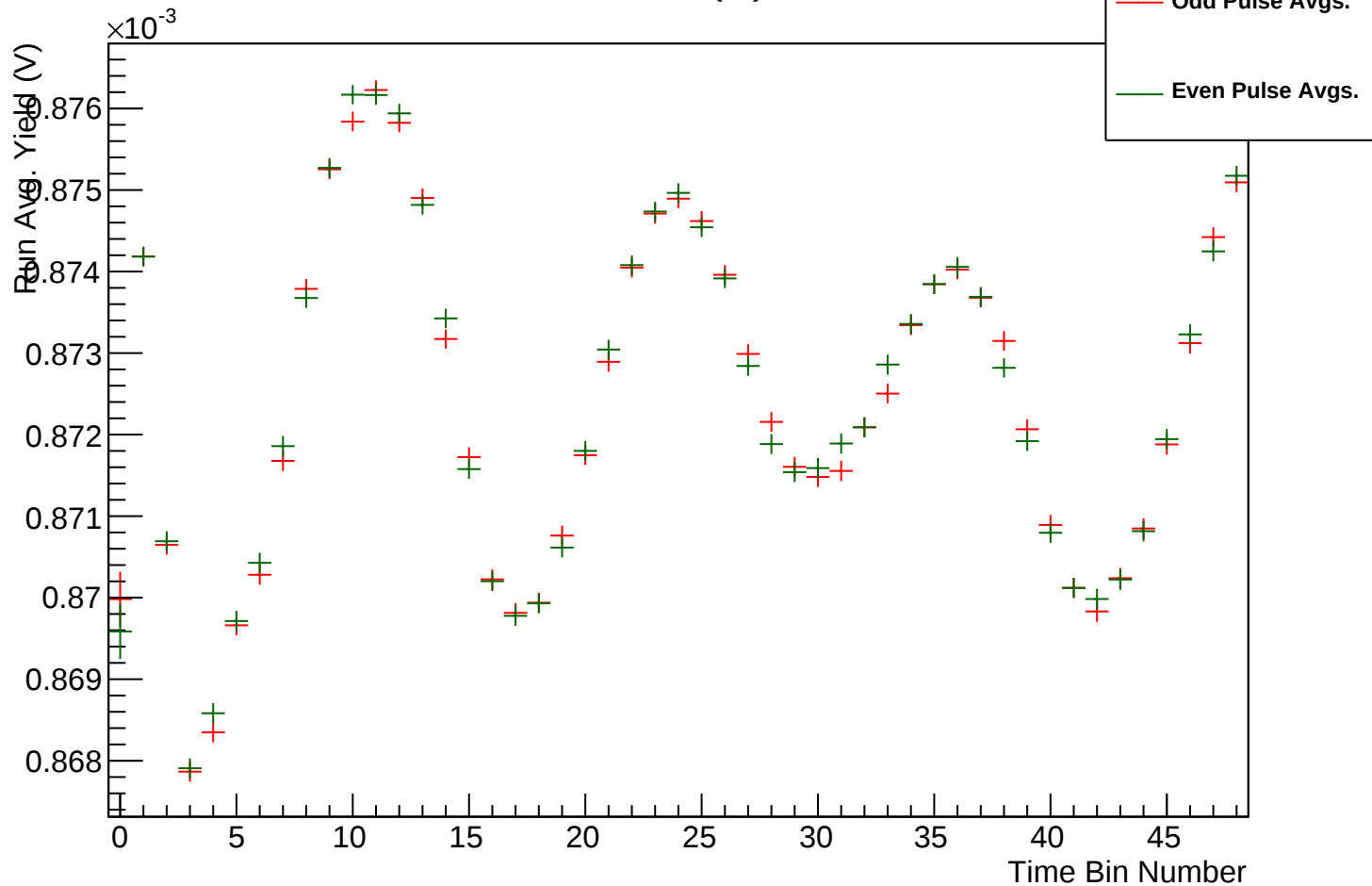
r17784-w28-Yield(V)-OddPulses



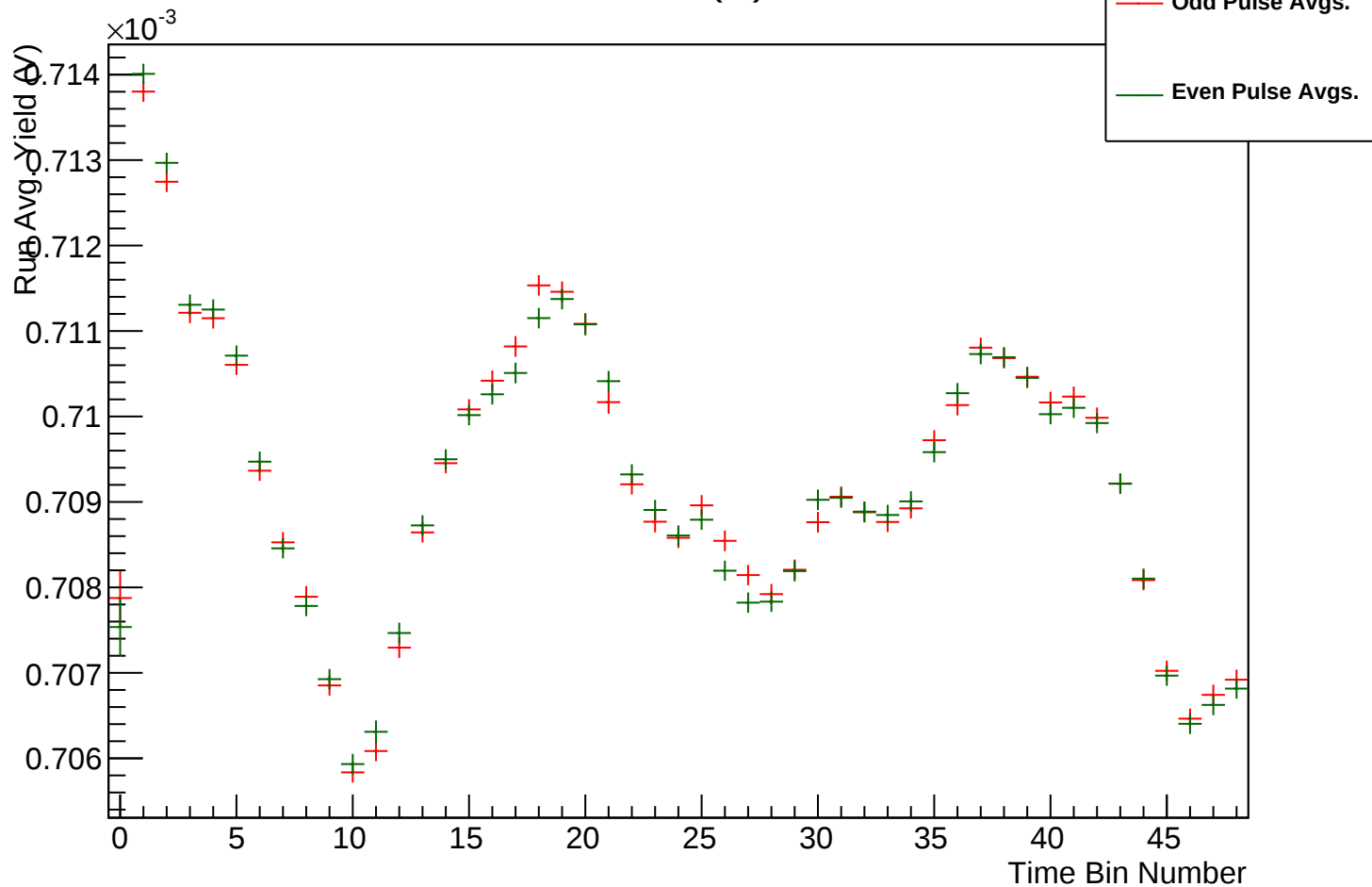
r17784-w29-Yield(V)-OddPulses



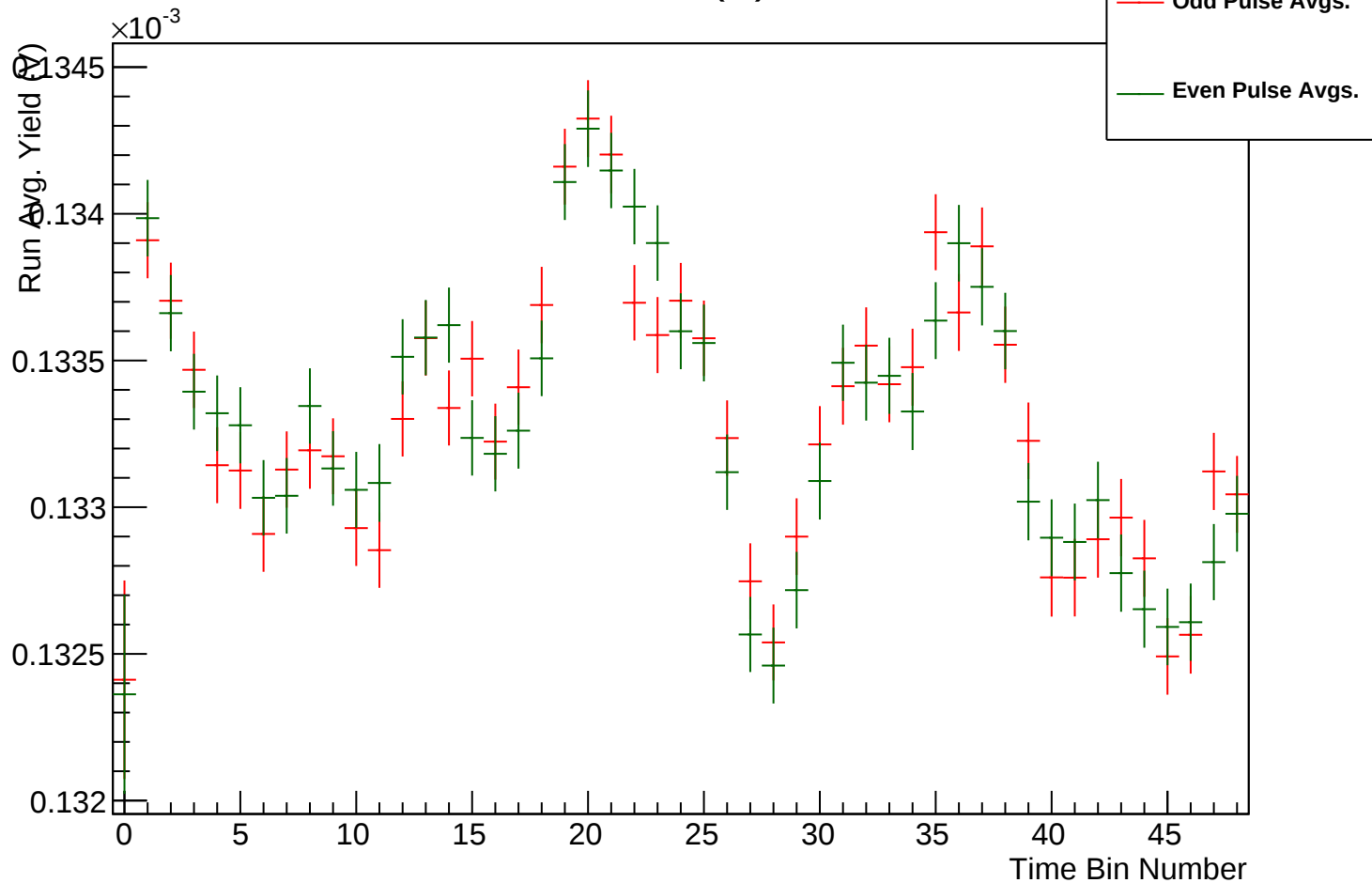
r17784-w30-Yield(V)-OddPulses



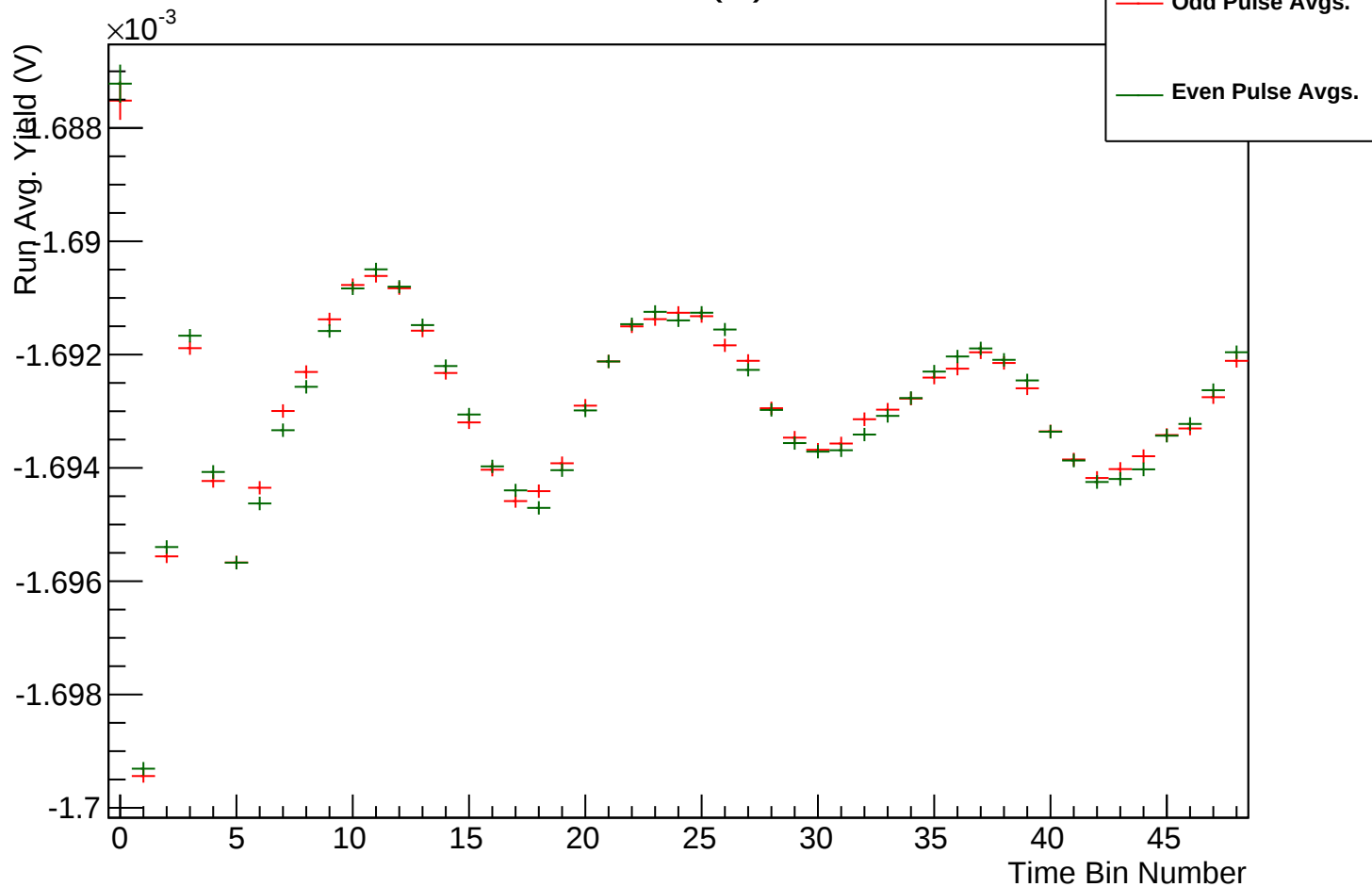
r17784-w31-Yield(V)-OddPulses



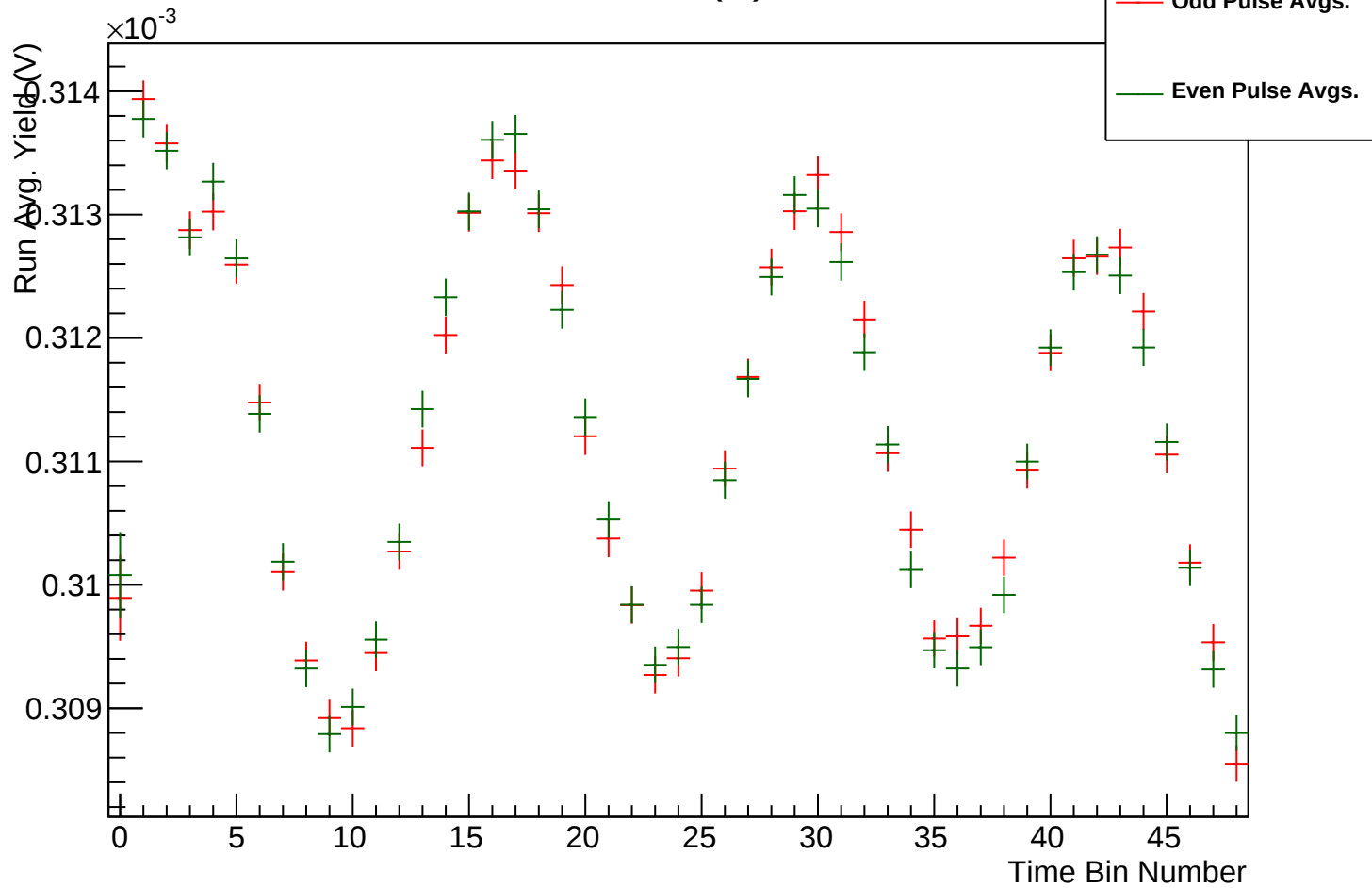
r17784-w32-Yield(V)-OddPulses



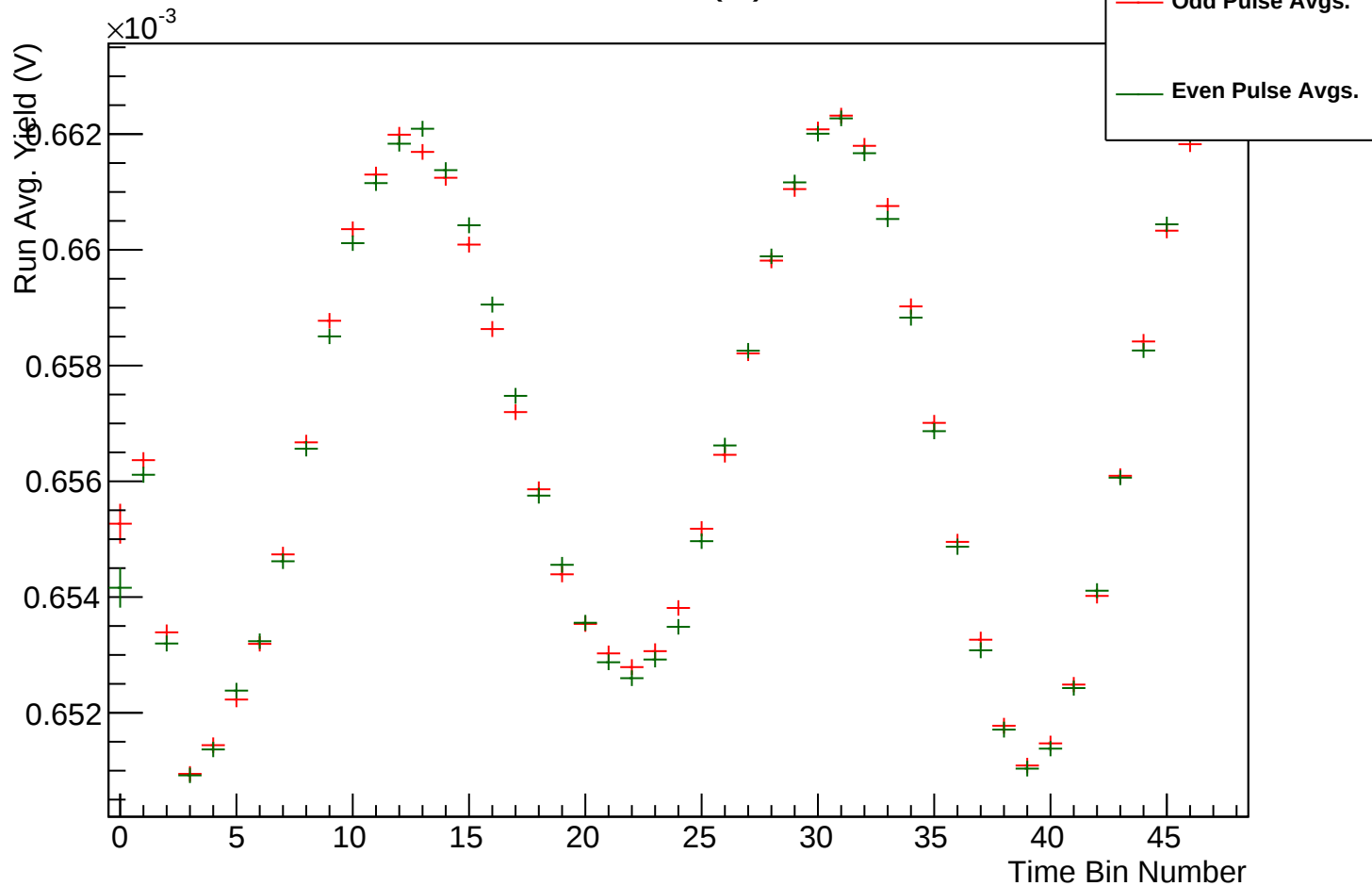
r17784-w33-Yield(V)-OddPulses



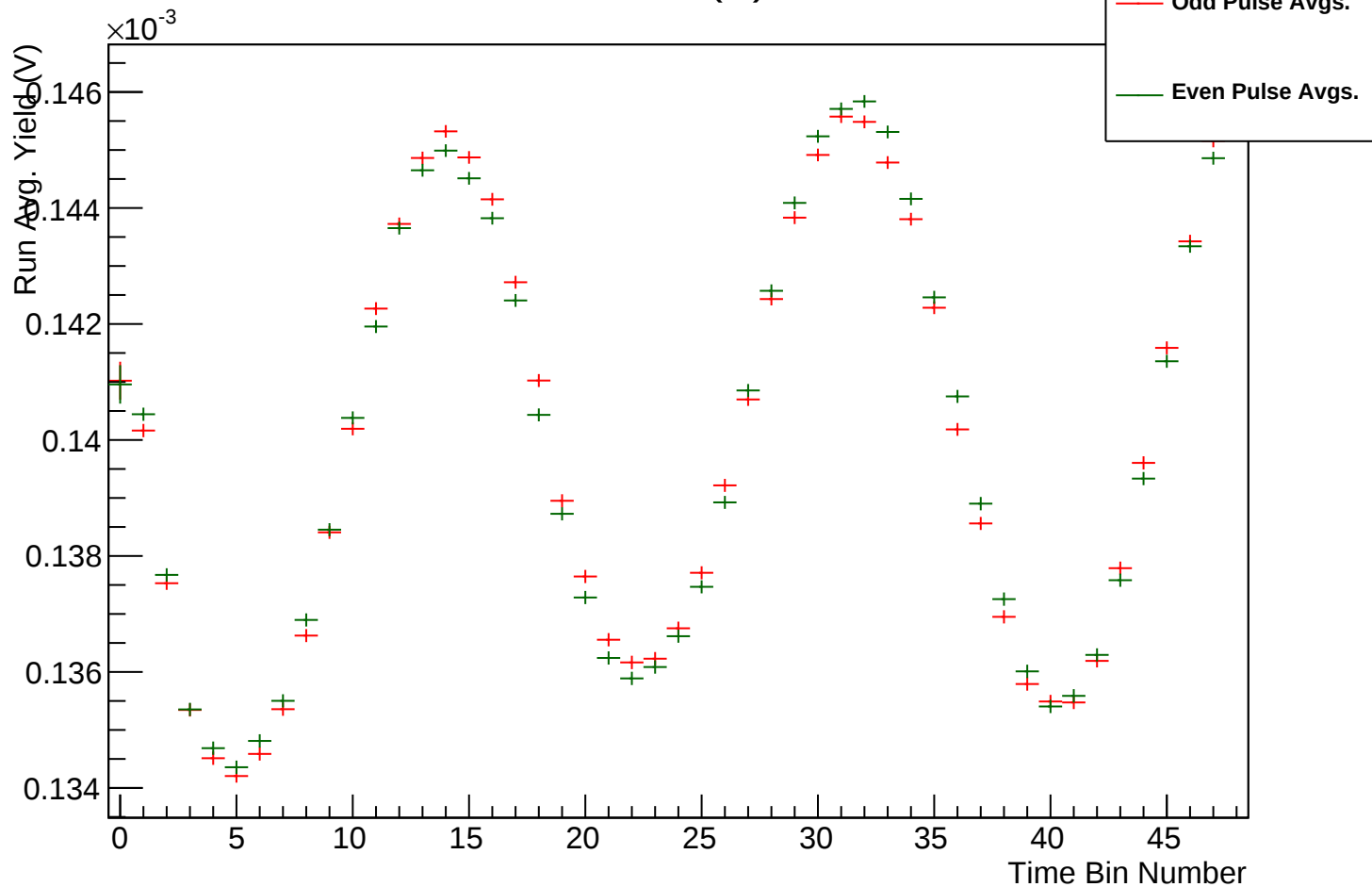
r17784-w34-Yield(V)-OddPulses



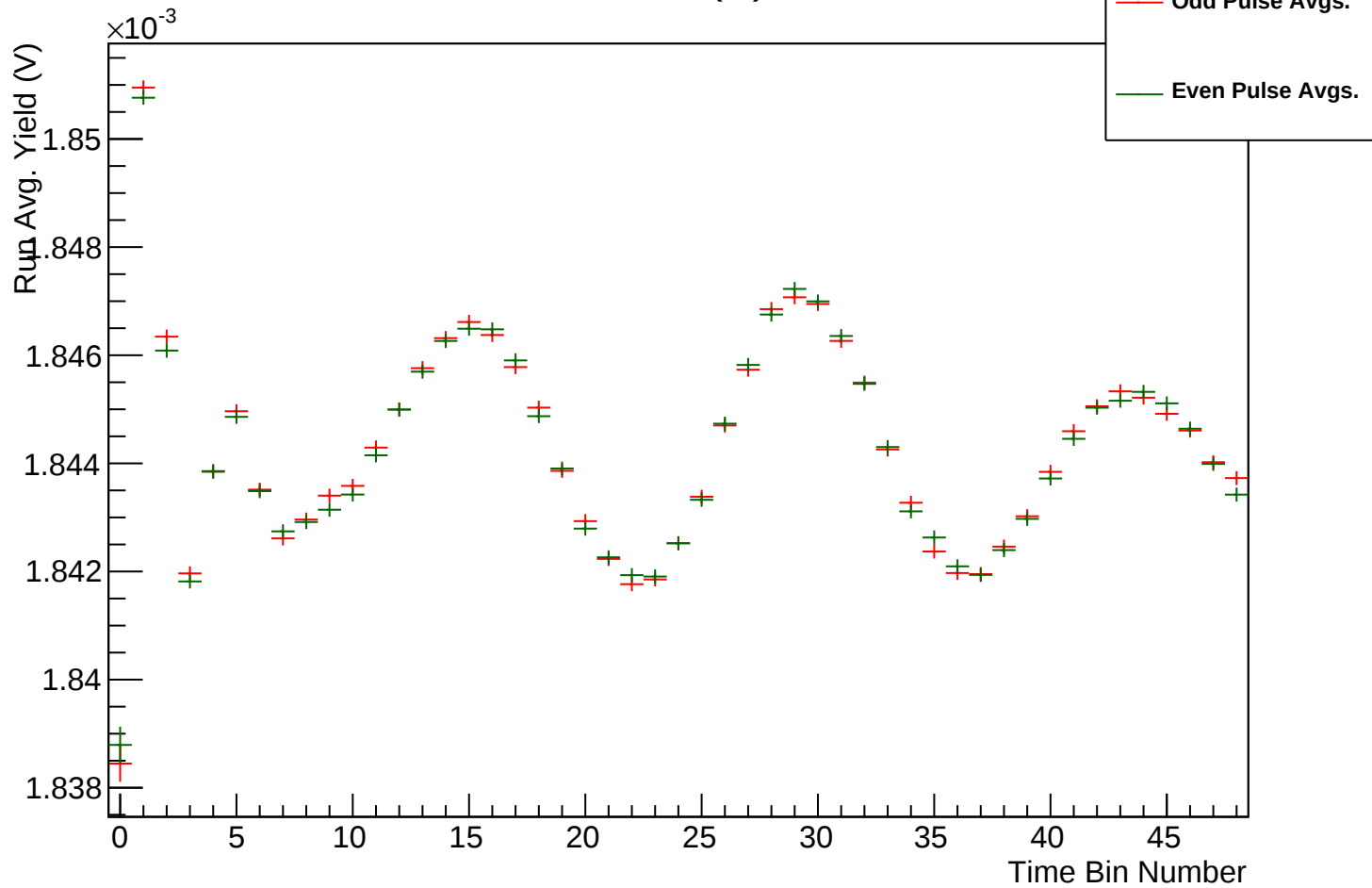
r17784-w35-Yield(V)-OddPulses



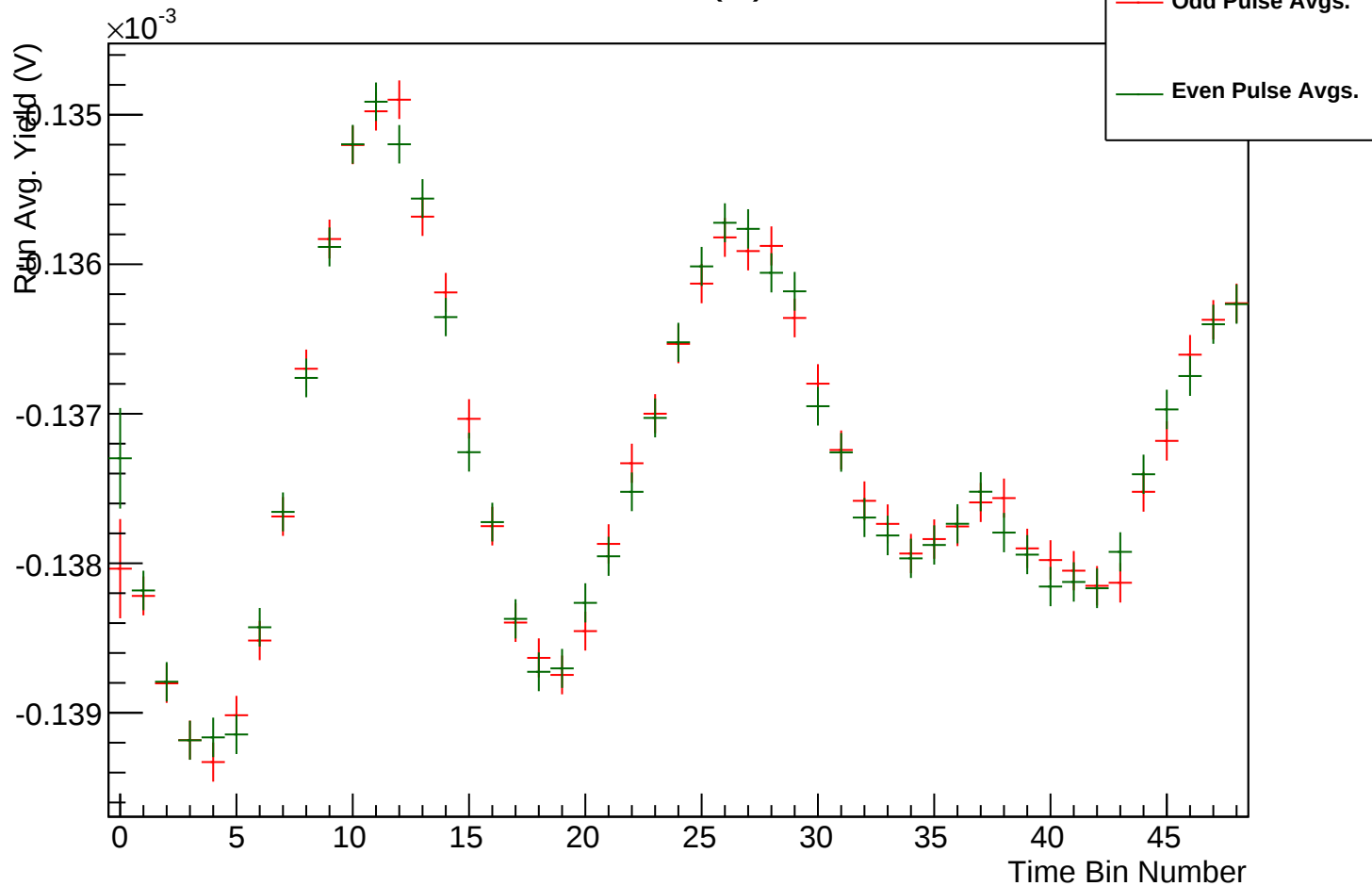
r17784-w36-Yield(V)-OddPulses



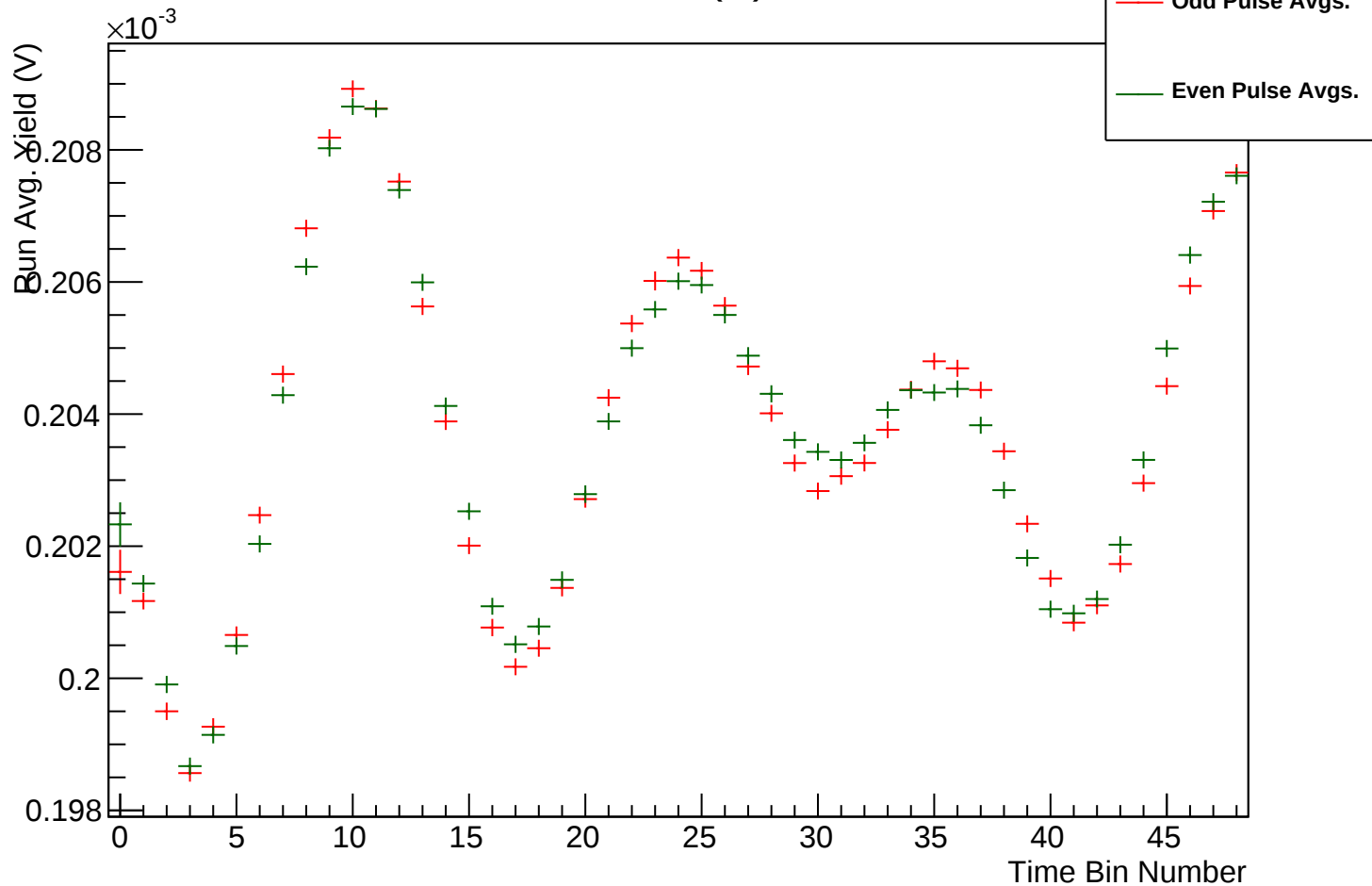
r17784-w37-Yield(V)-OddPulses



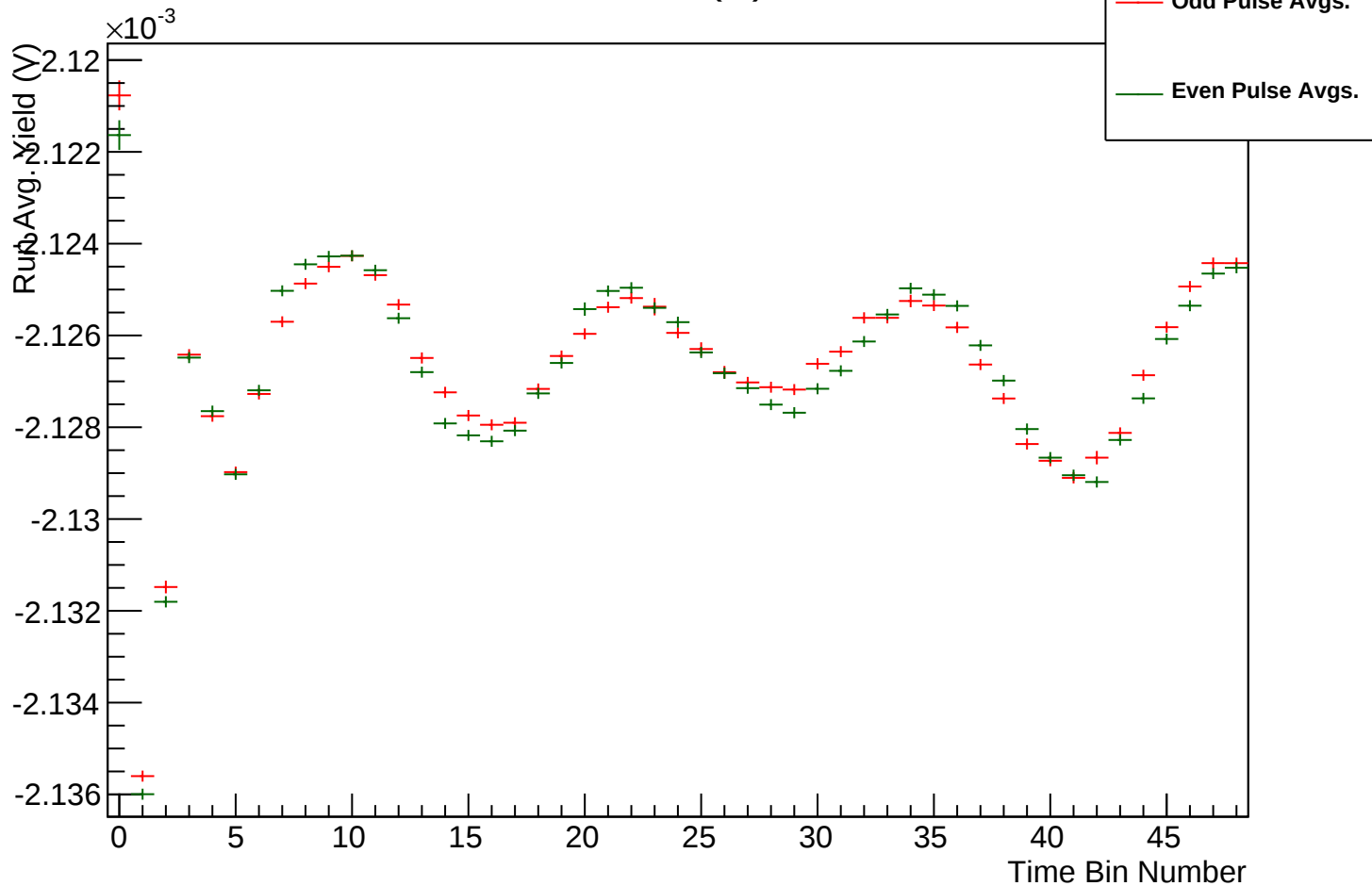
r17784-w38-Yield(V)-OddPulses



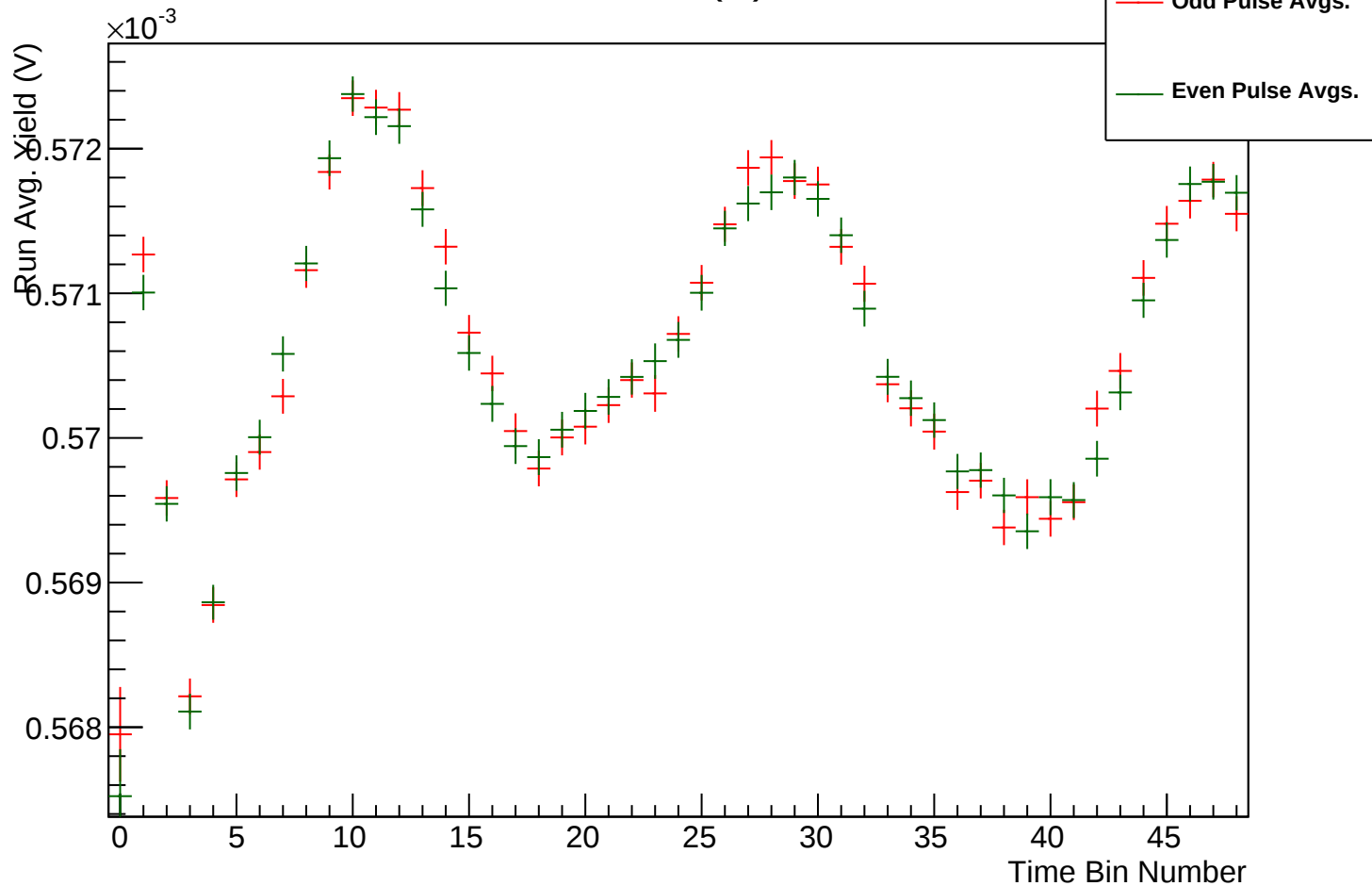
r17784-w39-Yield(V)-OddPulses



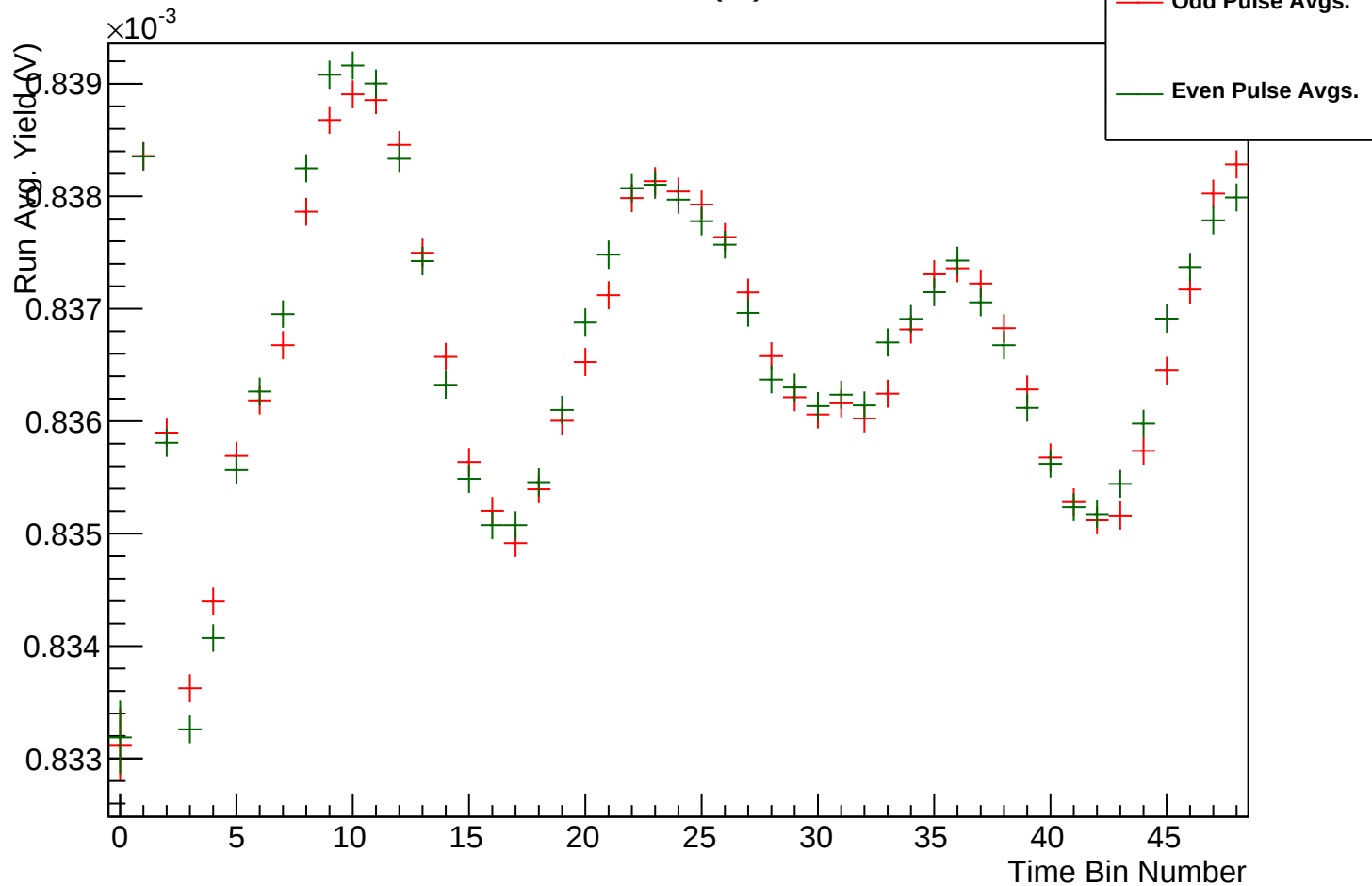
r17784-w40-Yield(V)-OddPulses



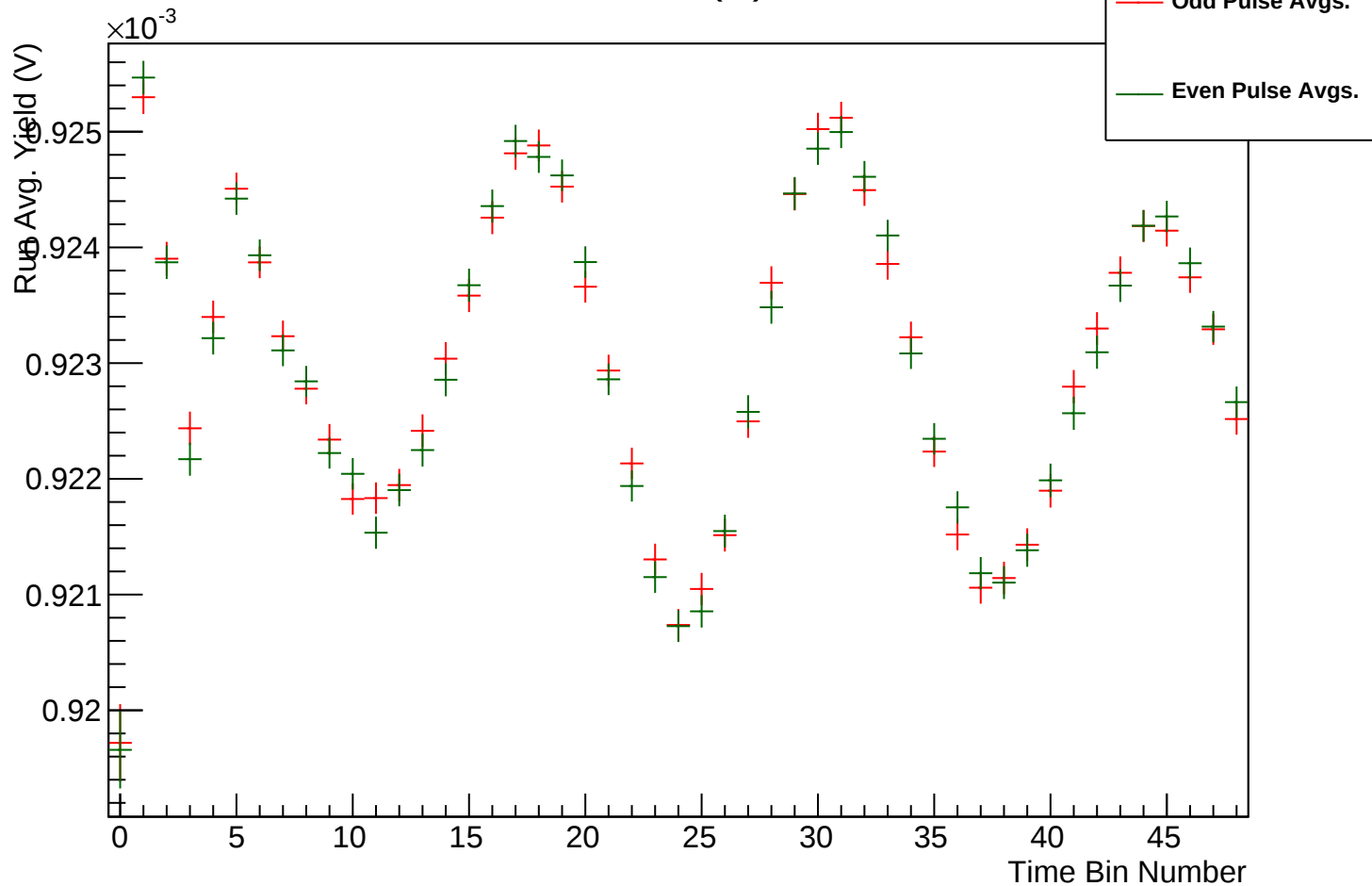
r17784-w41-Yield(V)-OddPulses



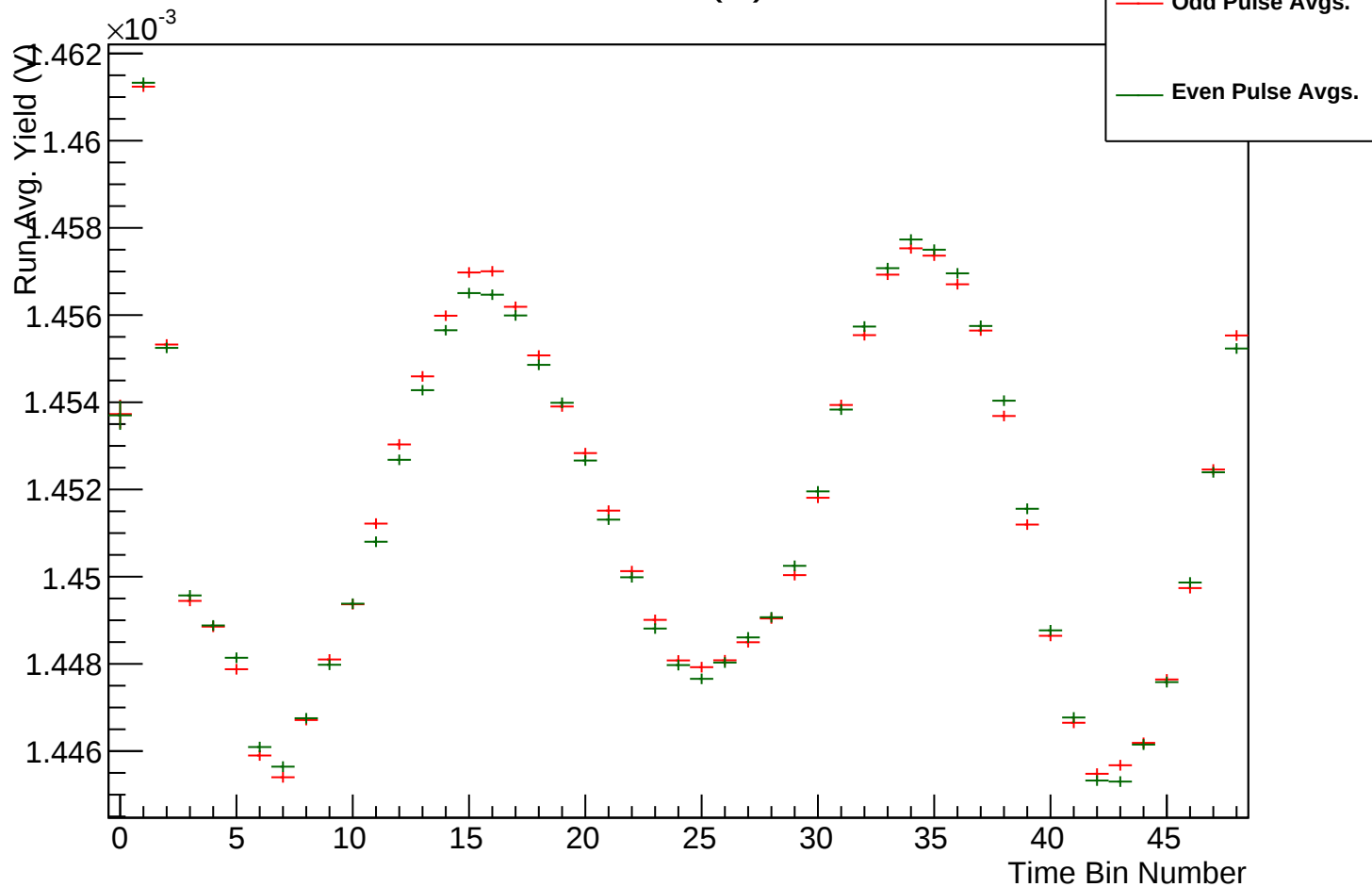
r17784-w42-Yield(V)-OddPulses



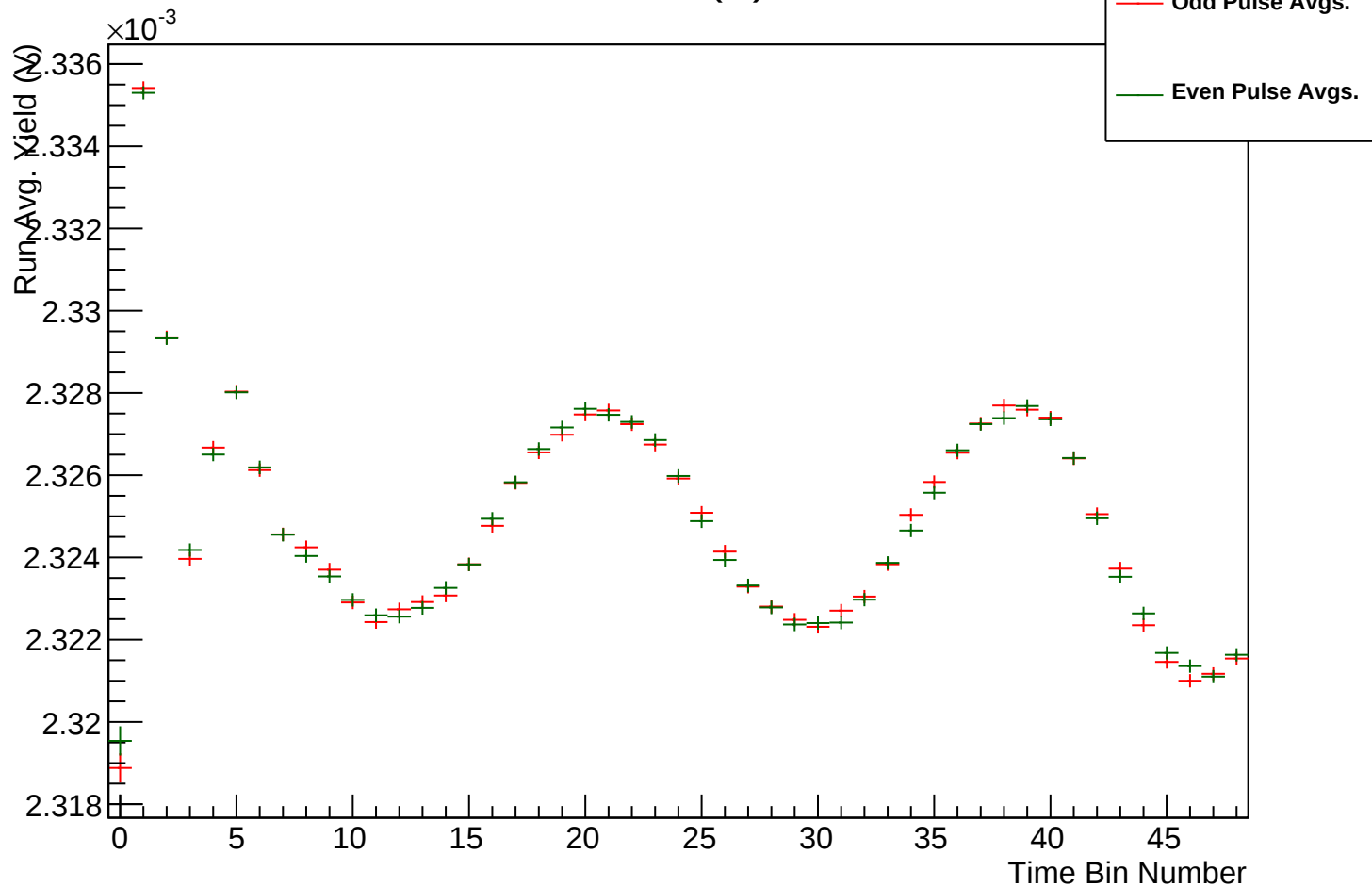
r17784-w43-Yield(V)-OddPulses



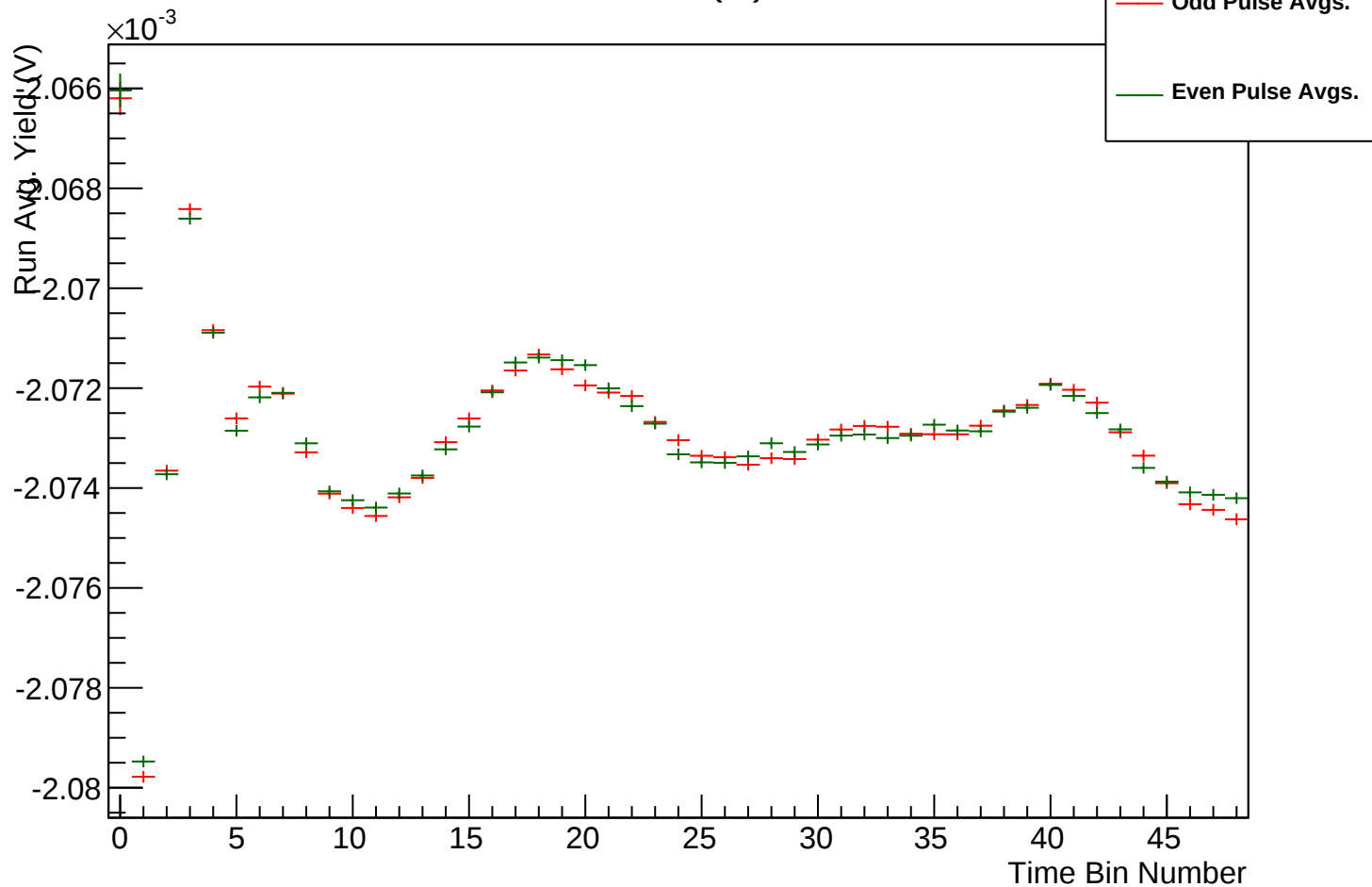
r17784-w44-Yield(V)-OddPulses



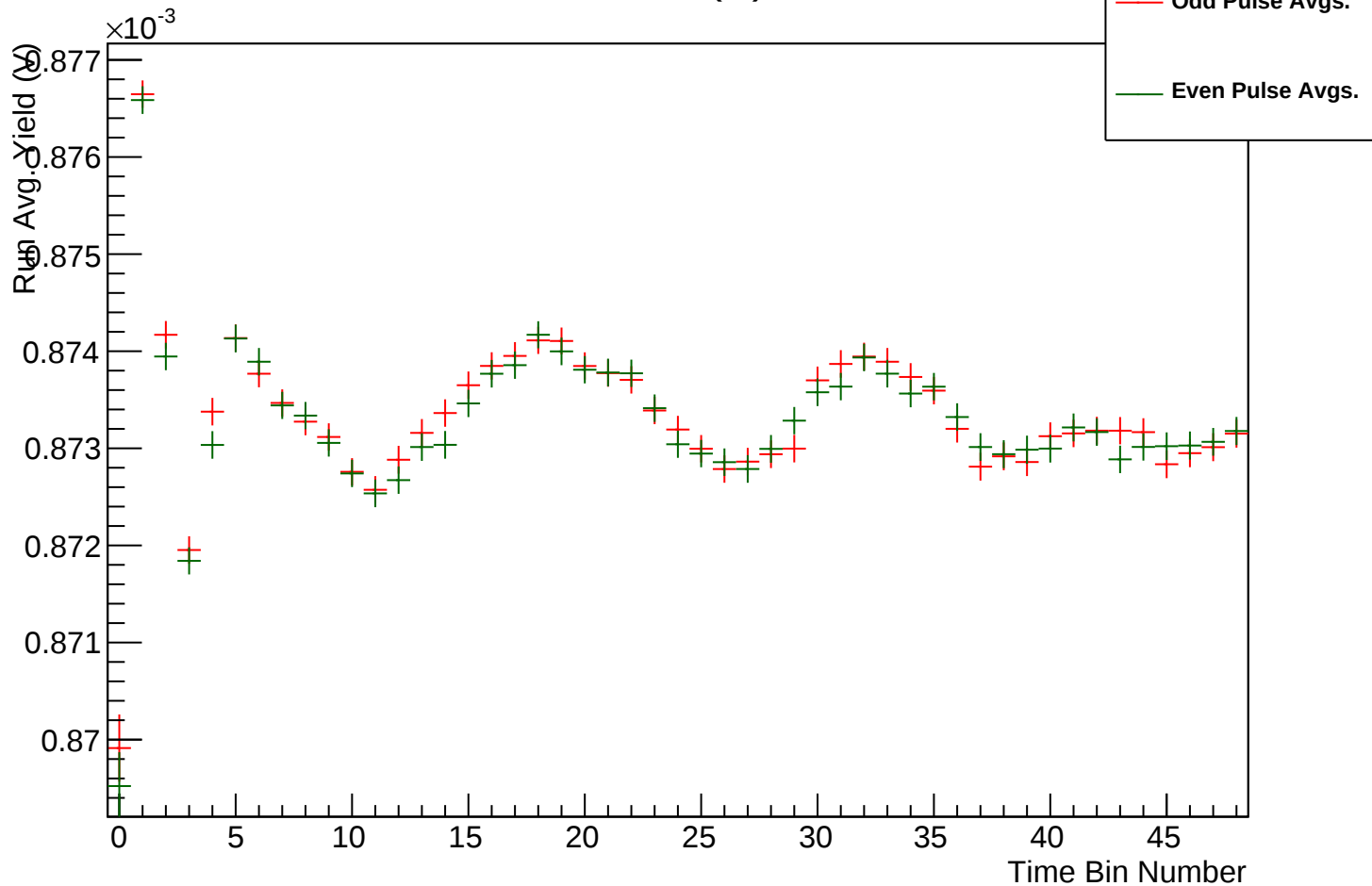
r17784-w45-Yield(V)-OddPulses



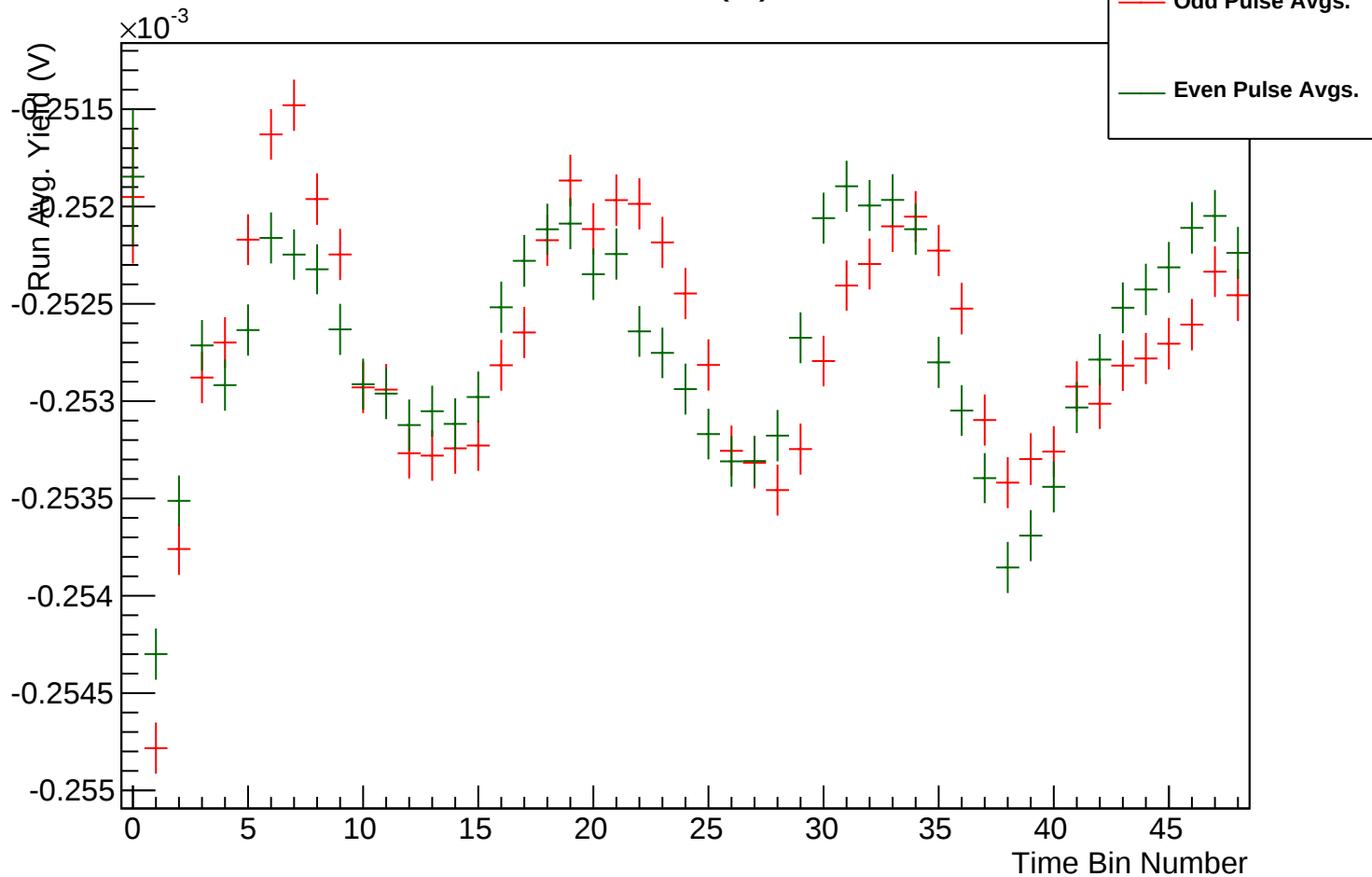
r17784-w46-Yield(V)-OddPulses



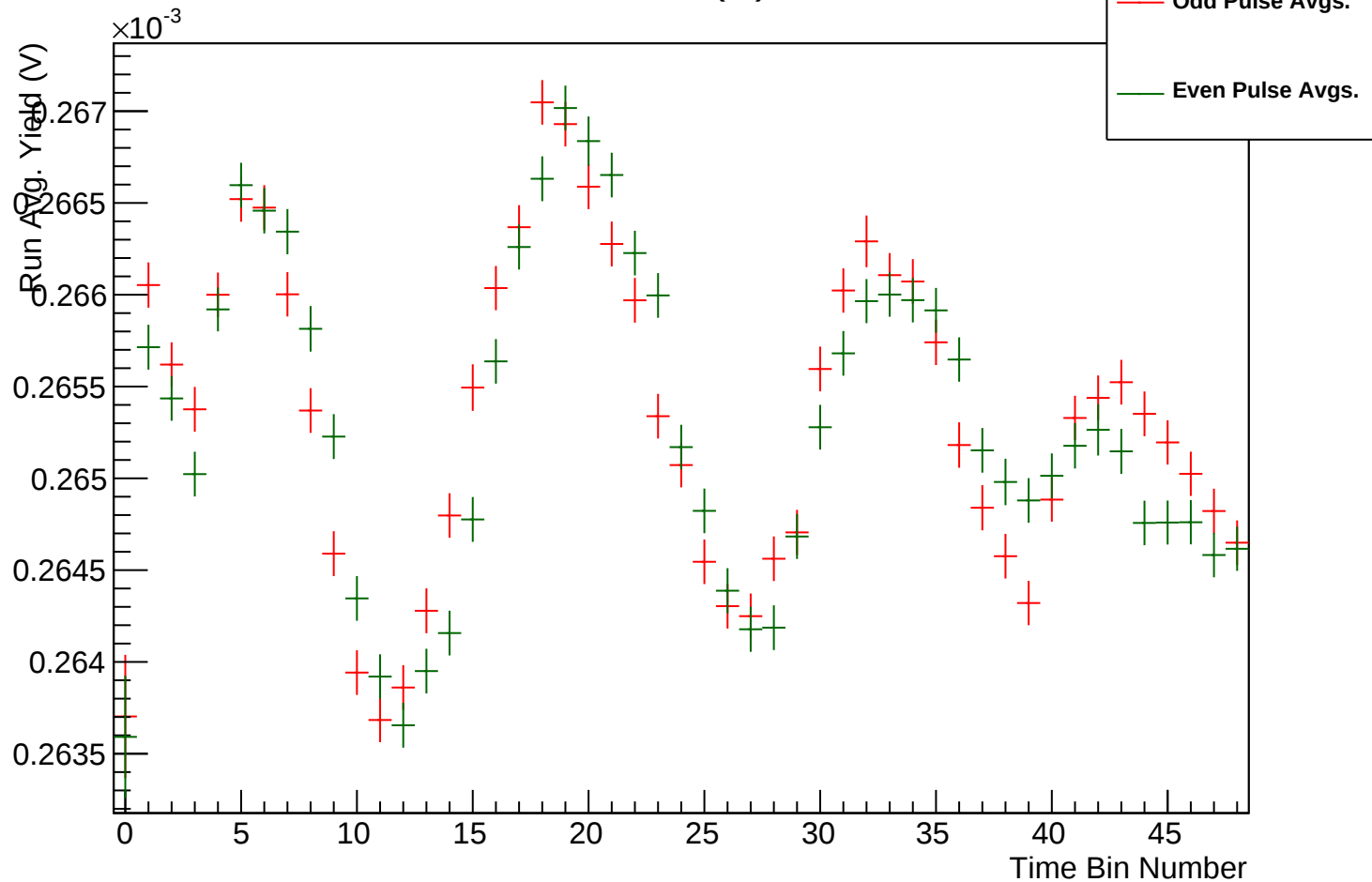
r17784-w47-Yield(V)-OddPulses



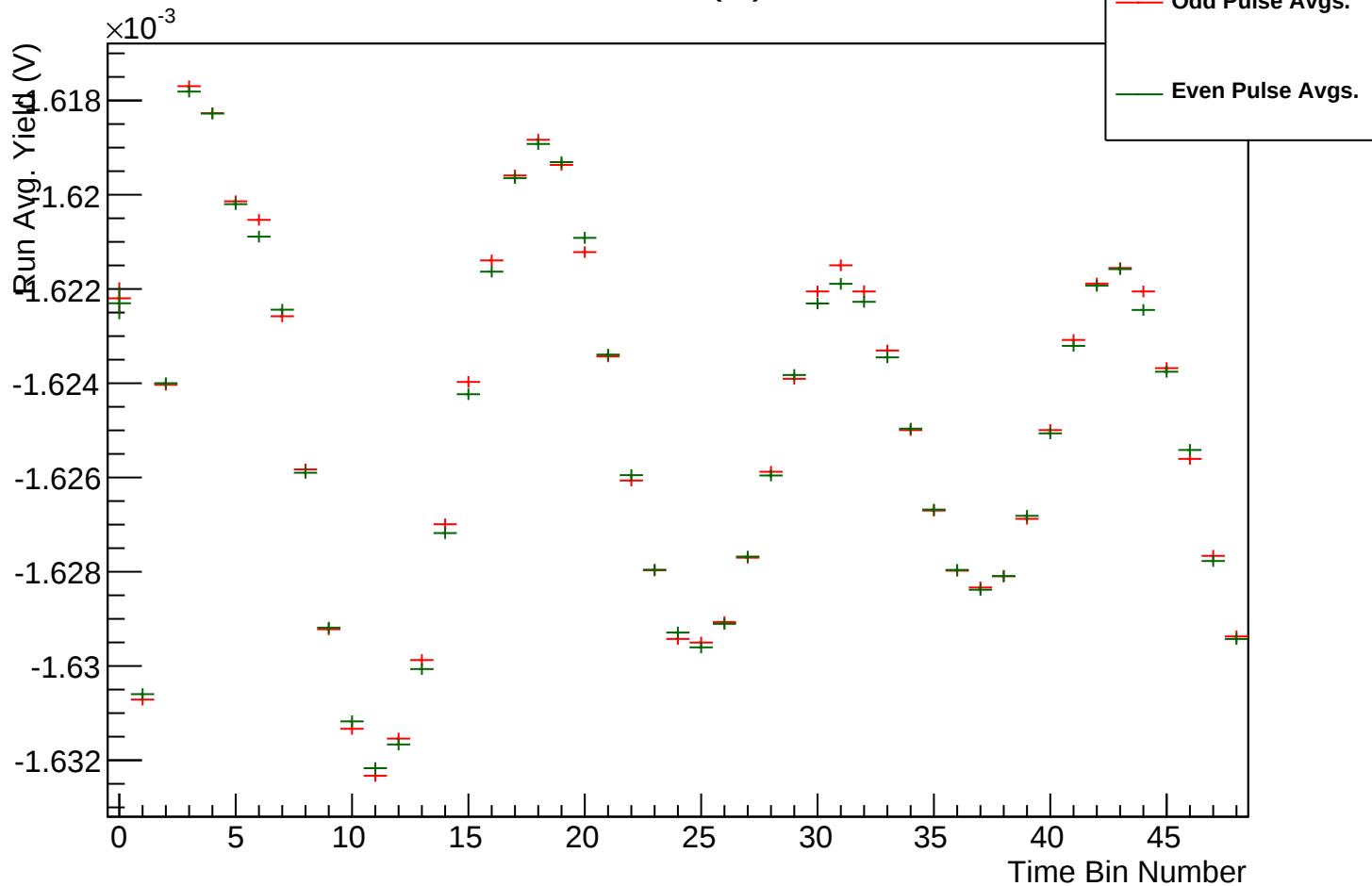
r17784-w48-Yield(V)-OddPulses



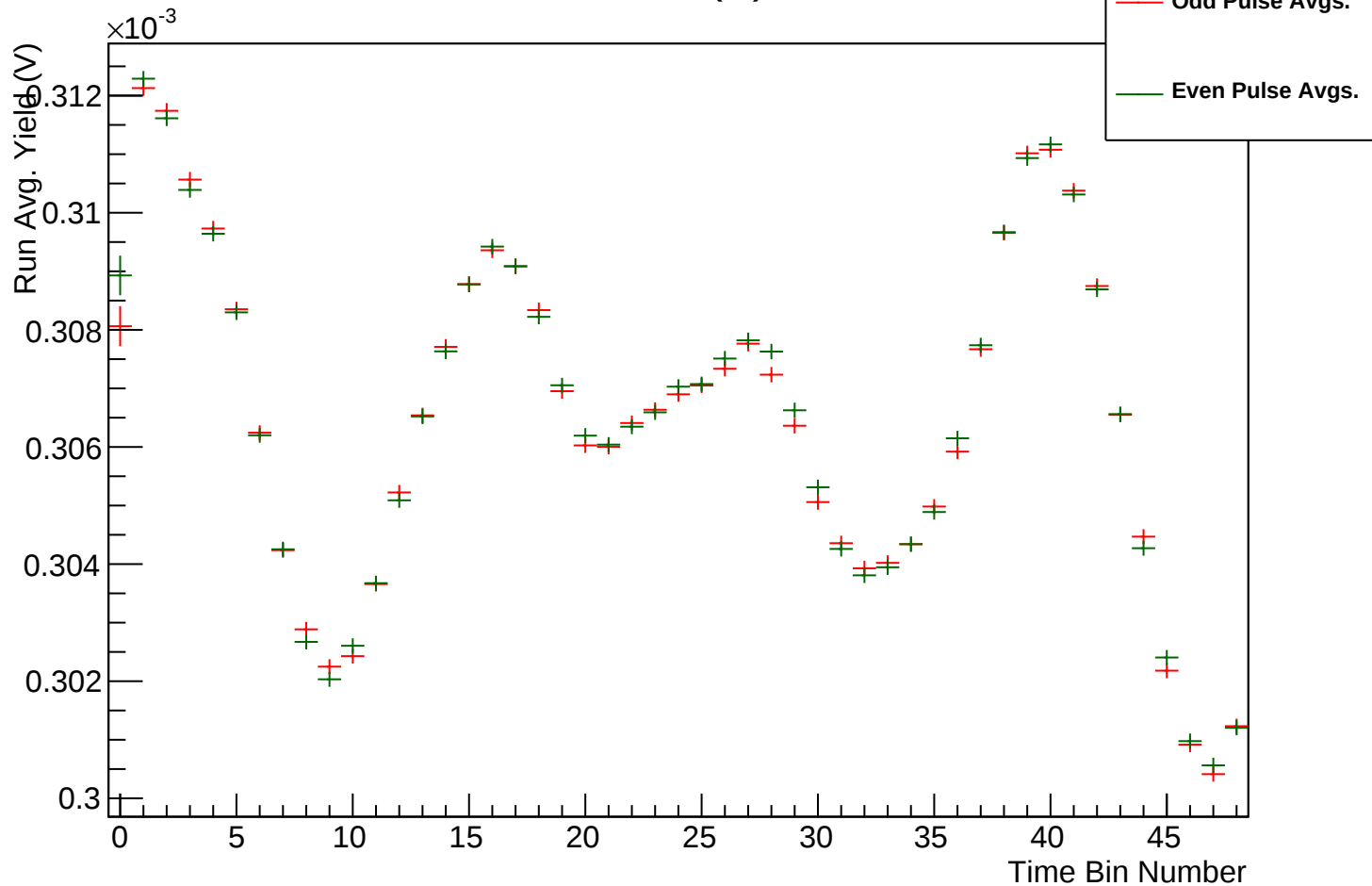
r17784-w49-Yield(V)-OddPulses



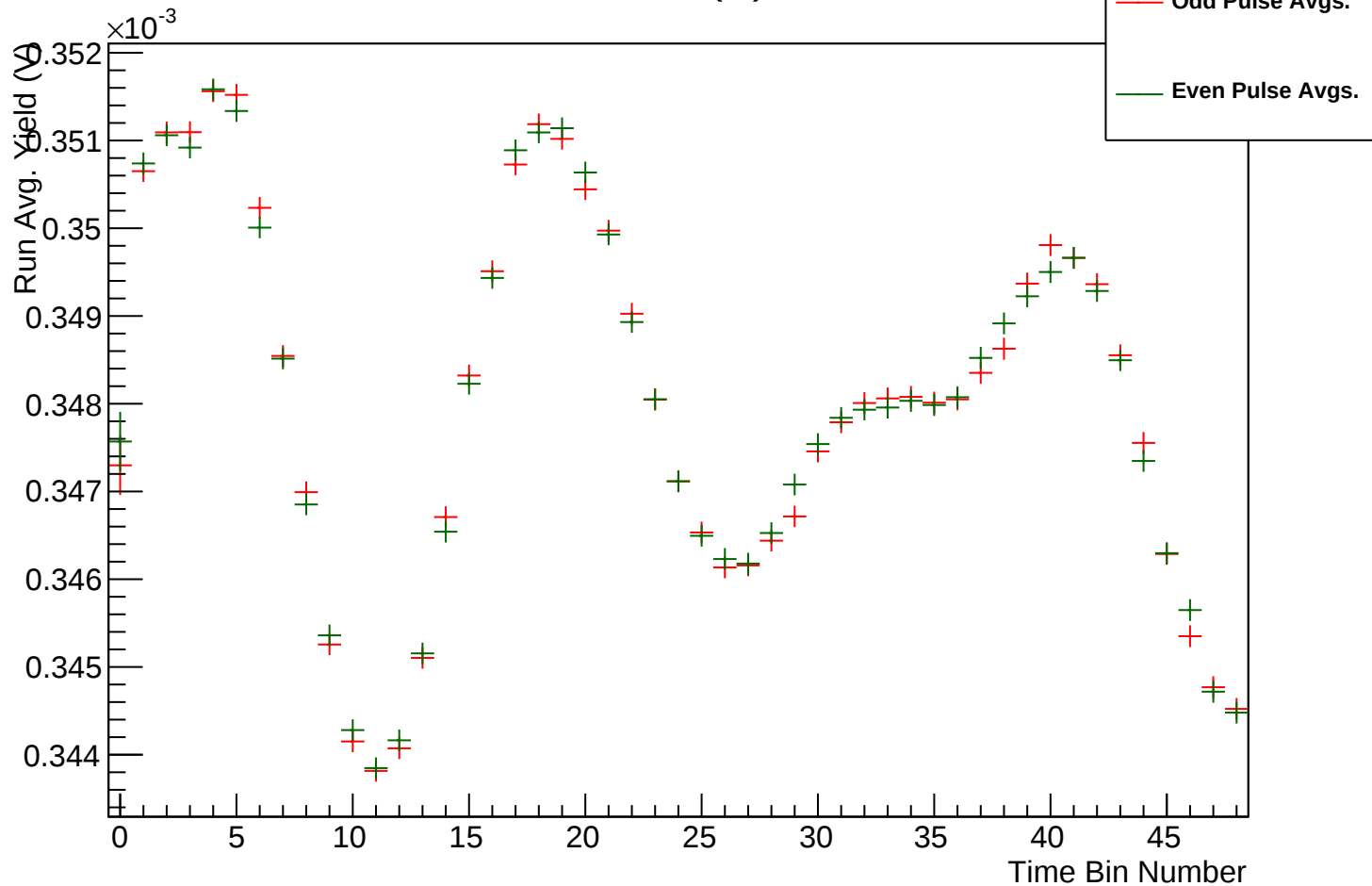
r17784-w50-Yield(V)-OddPulses



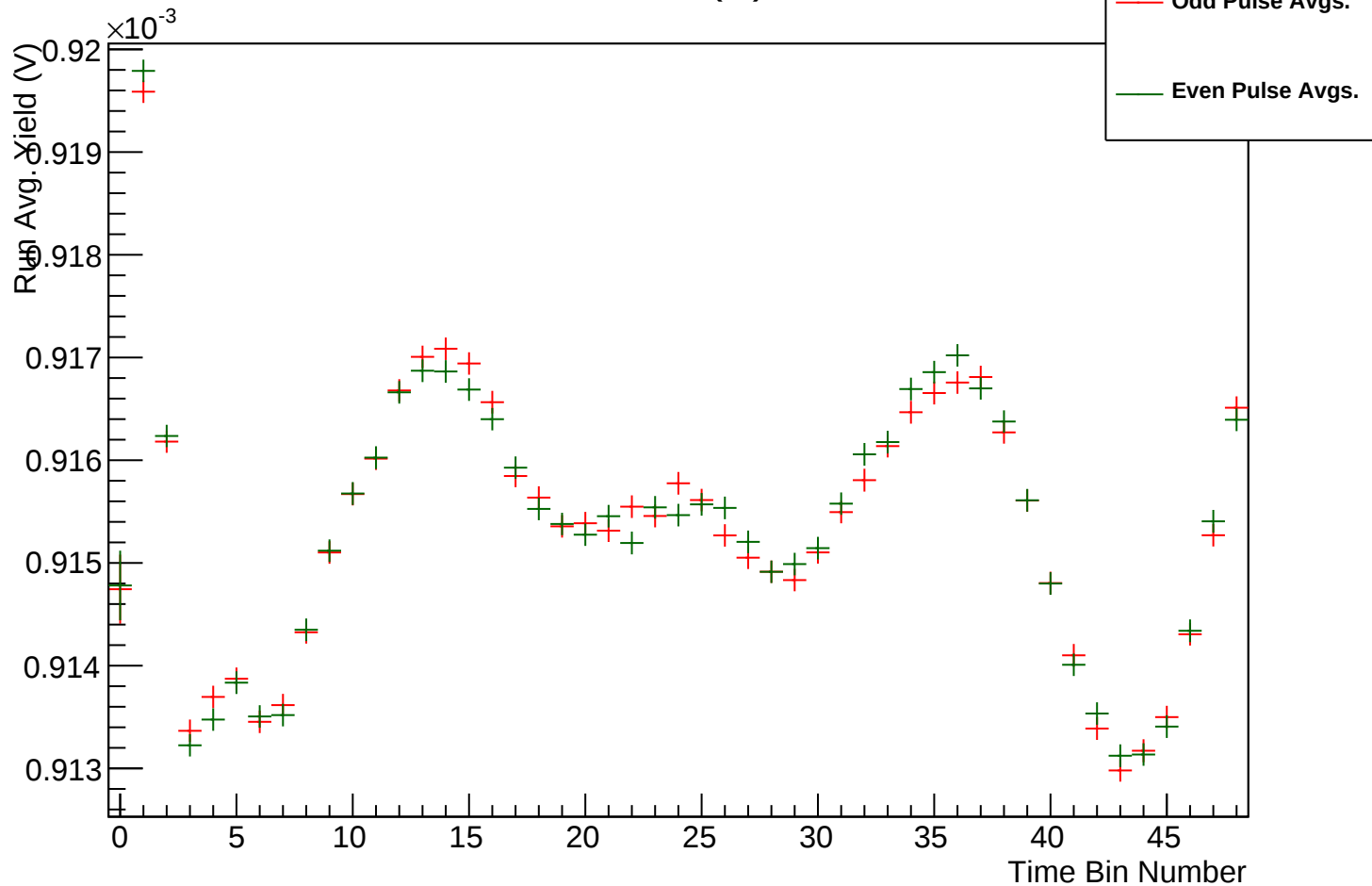
r17784-w51-Yield(V)-OddPulses



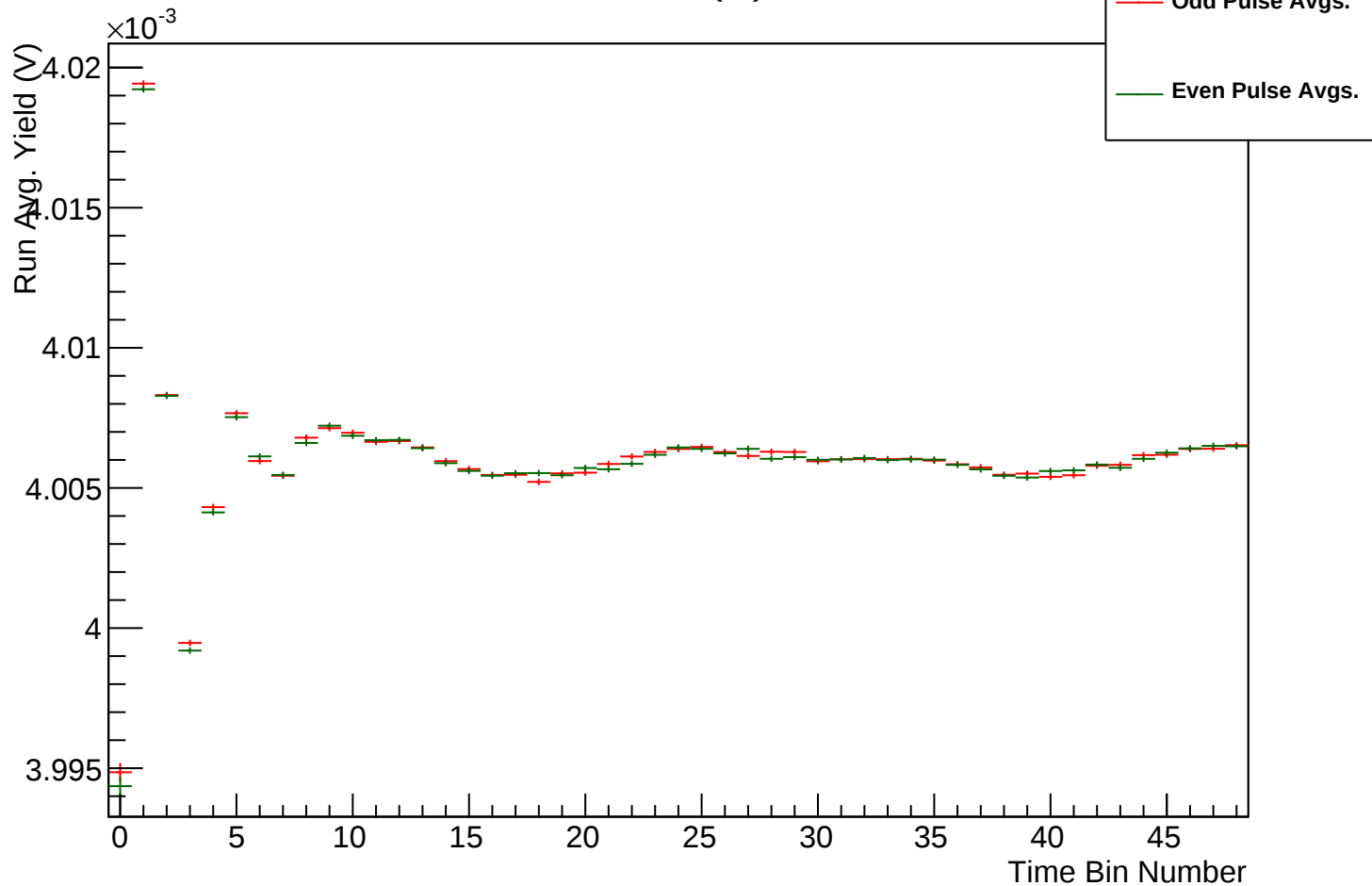
r17784-w52-Yield(V)-OddPulses



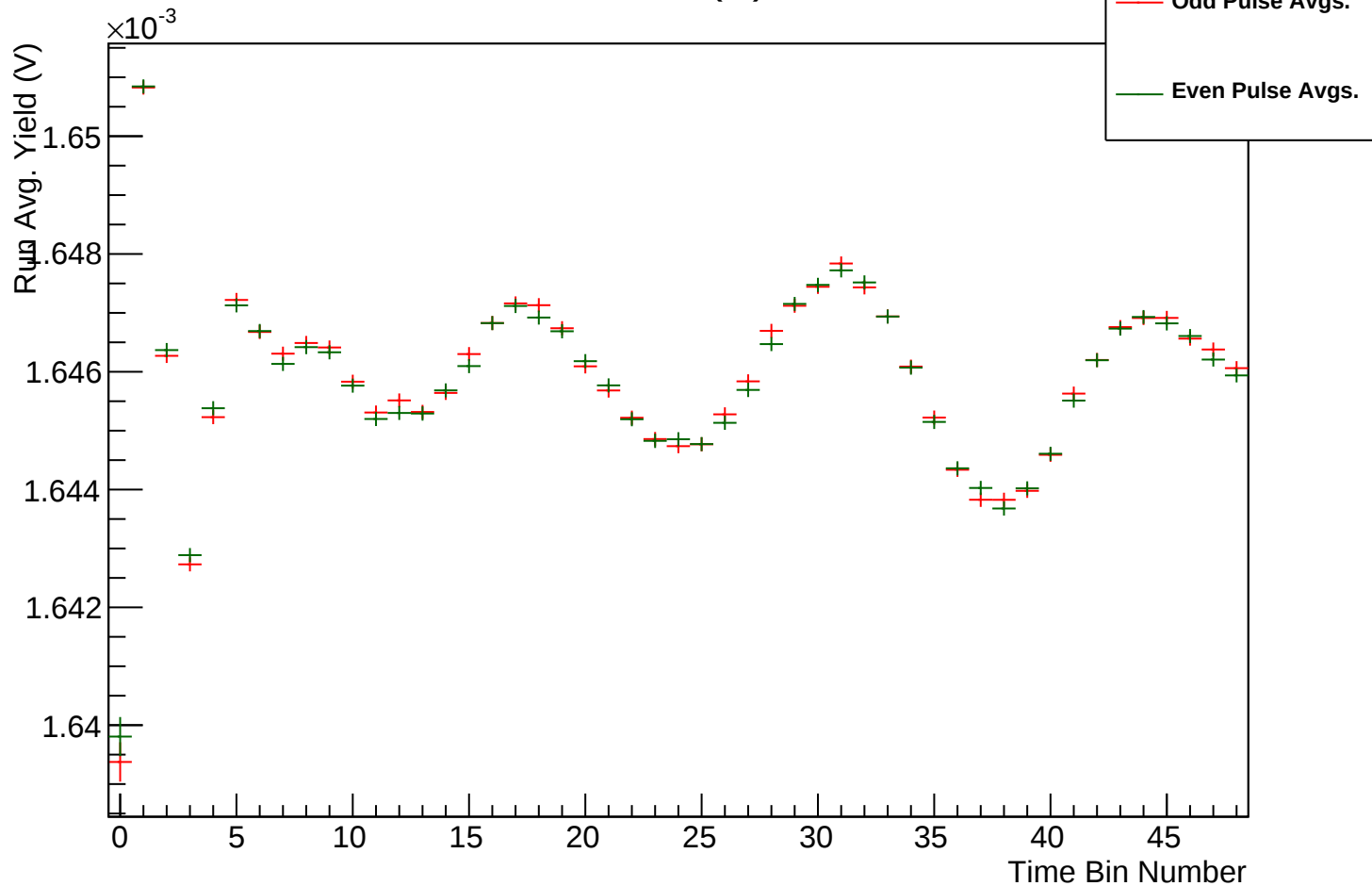
r17784-w53-Yield(V)-OddPulses



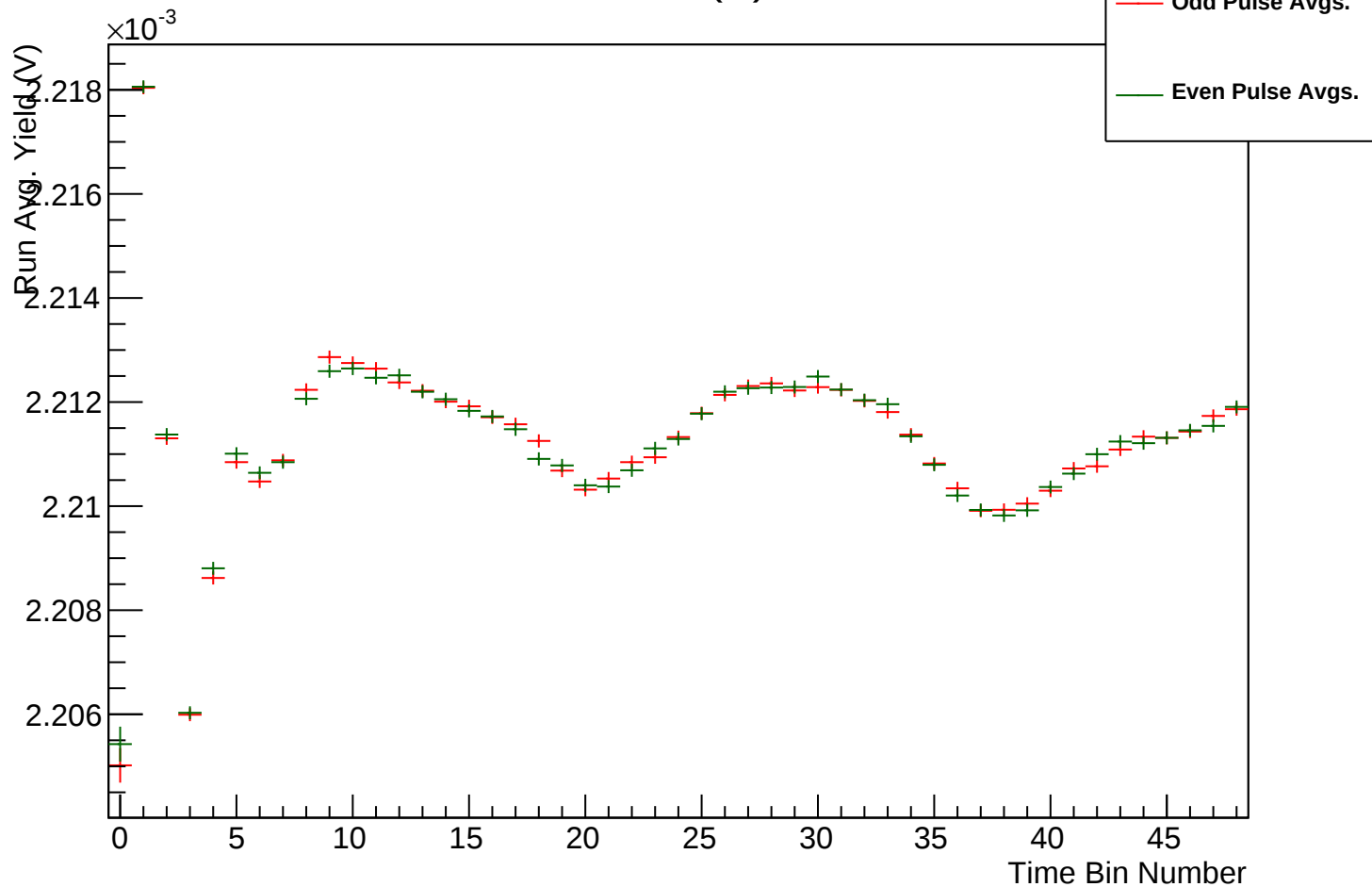
r17784-w54-Yield(V)-OddPulses



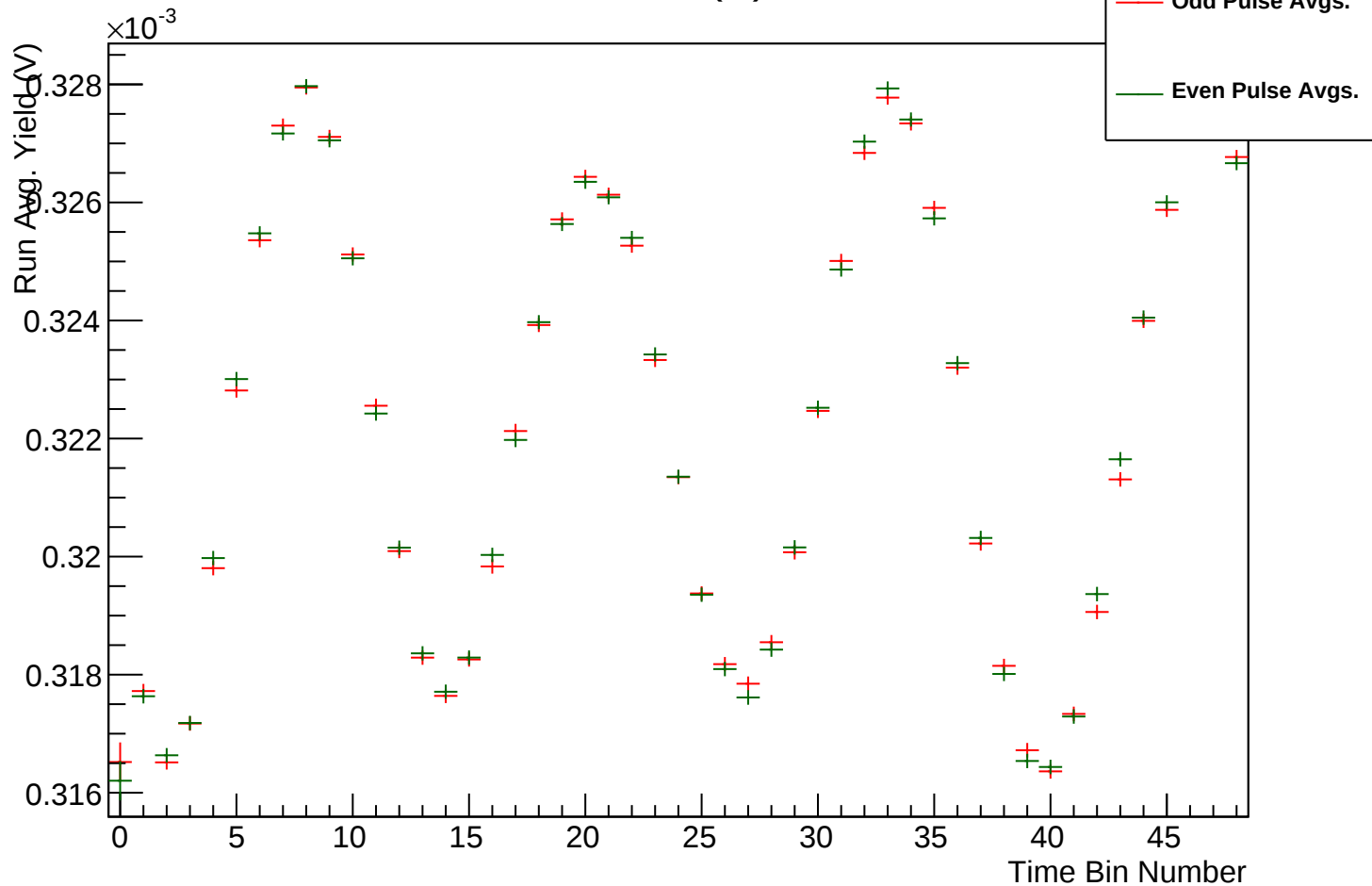
r17784-w55-Yield(V)-OddPulses



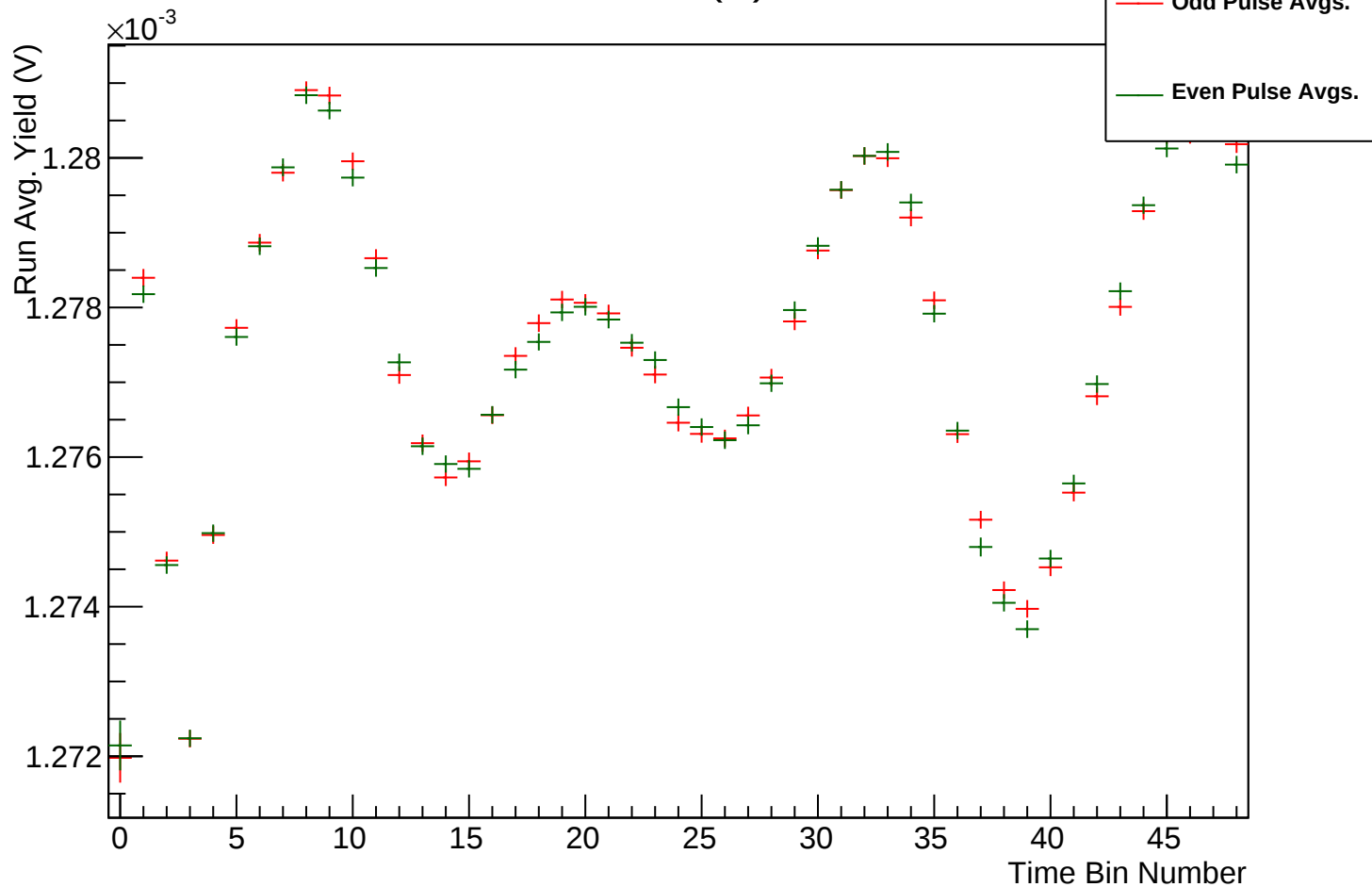
r17784-w56-Yield(V)-OddPulses



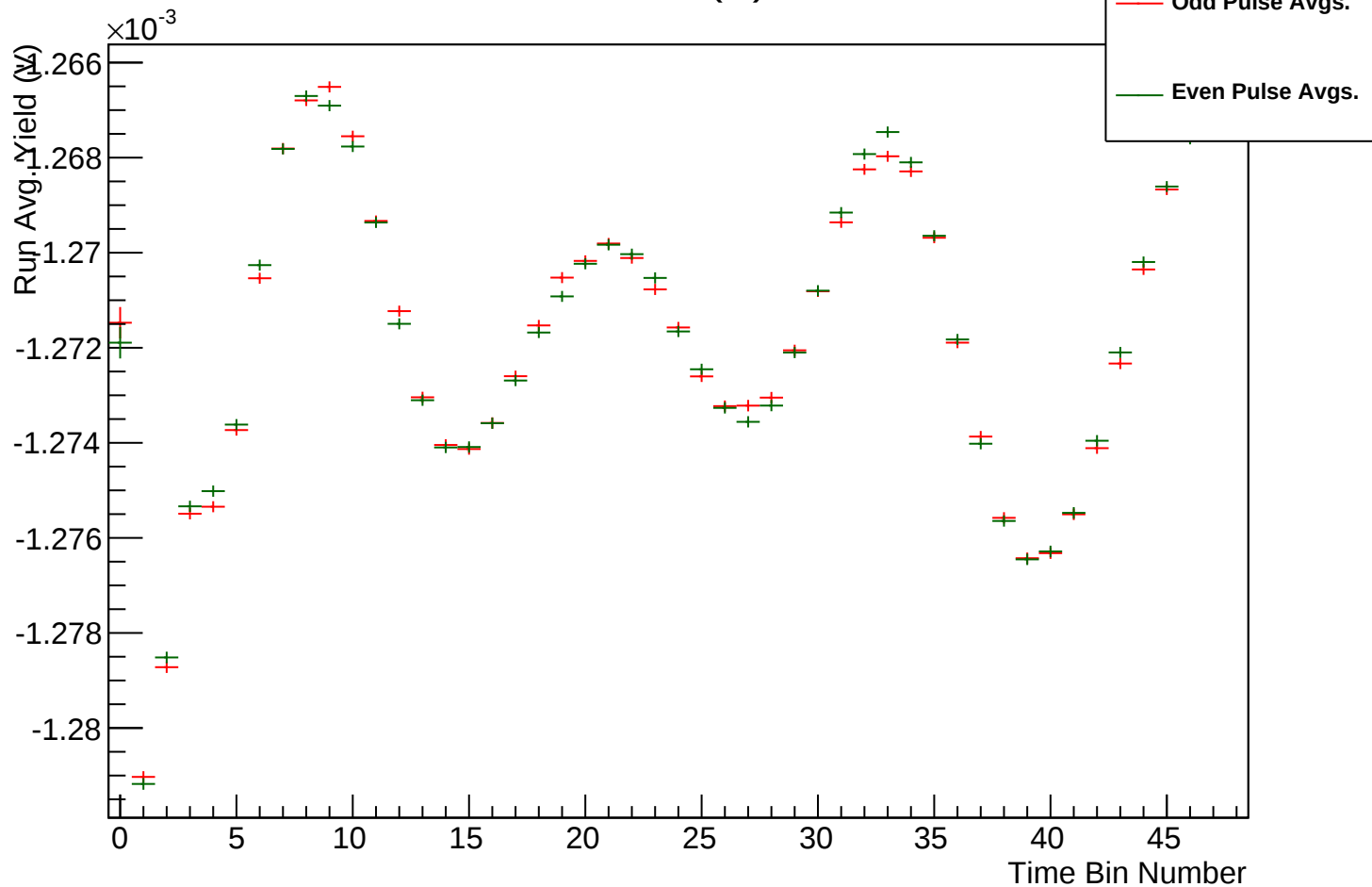
r17784-w57-Yield(V)-OddPulses



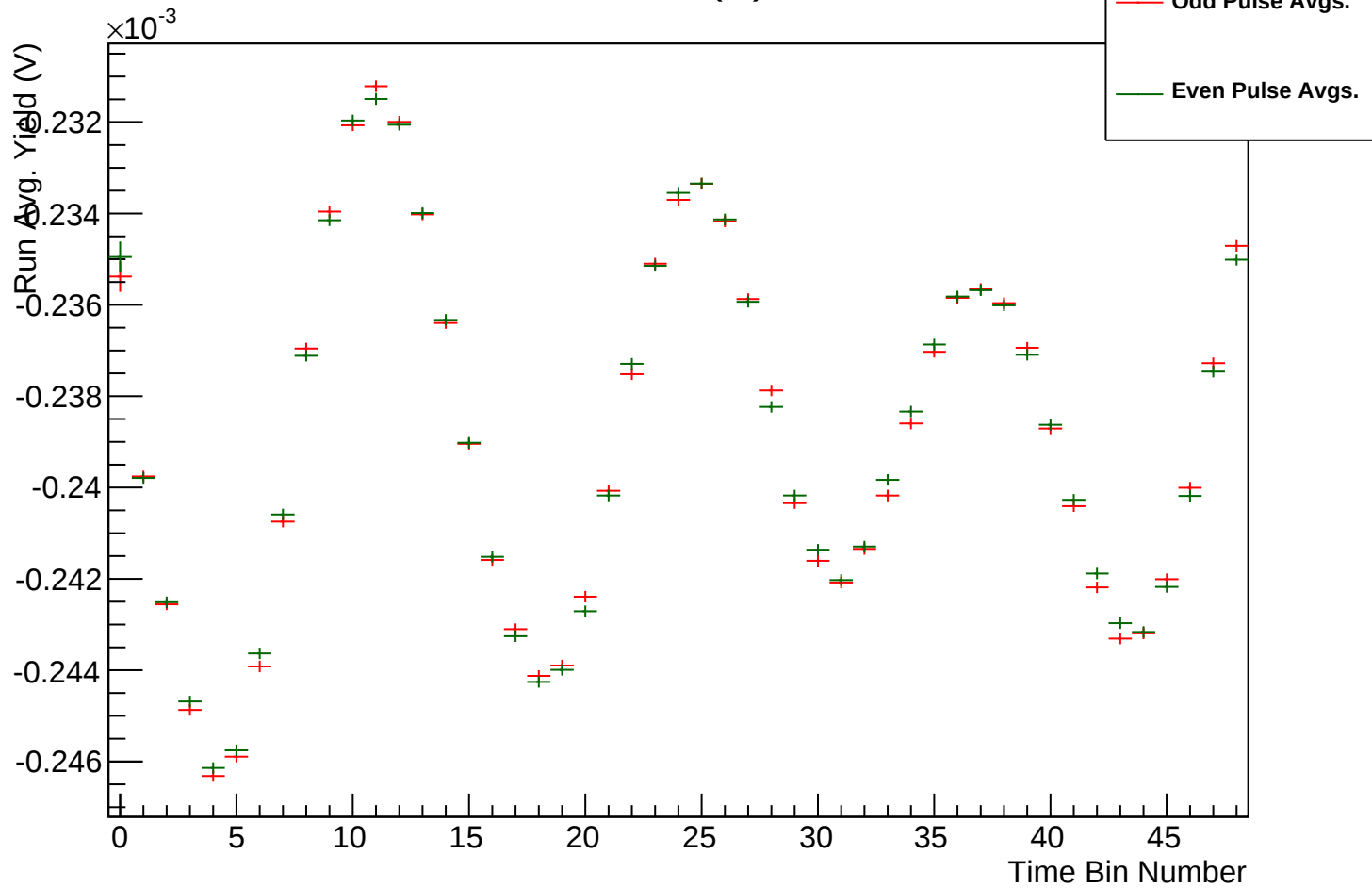
r17784-w58-Yield(V)-OddPulses



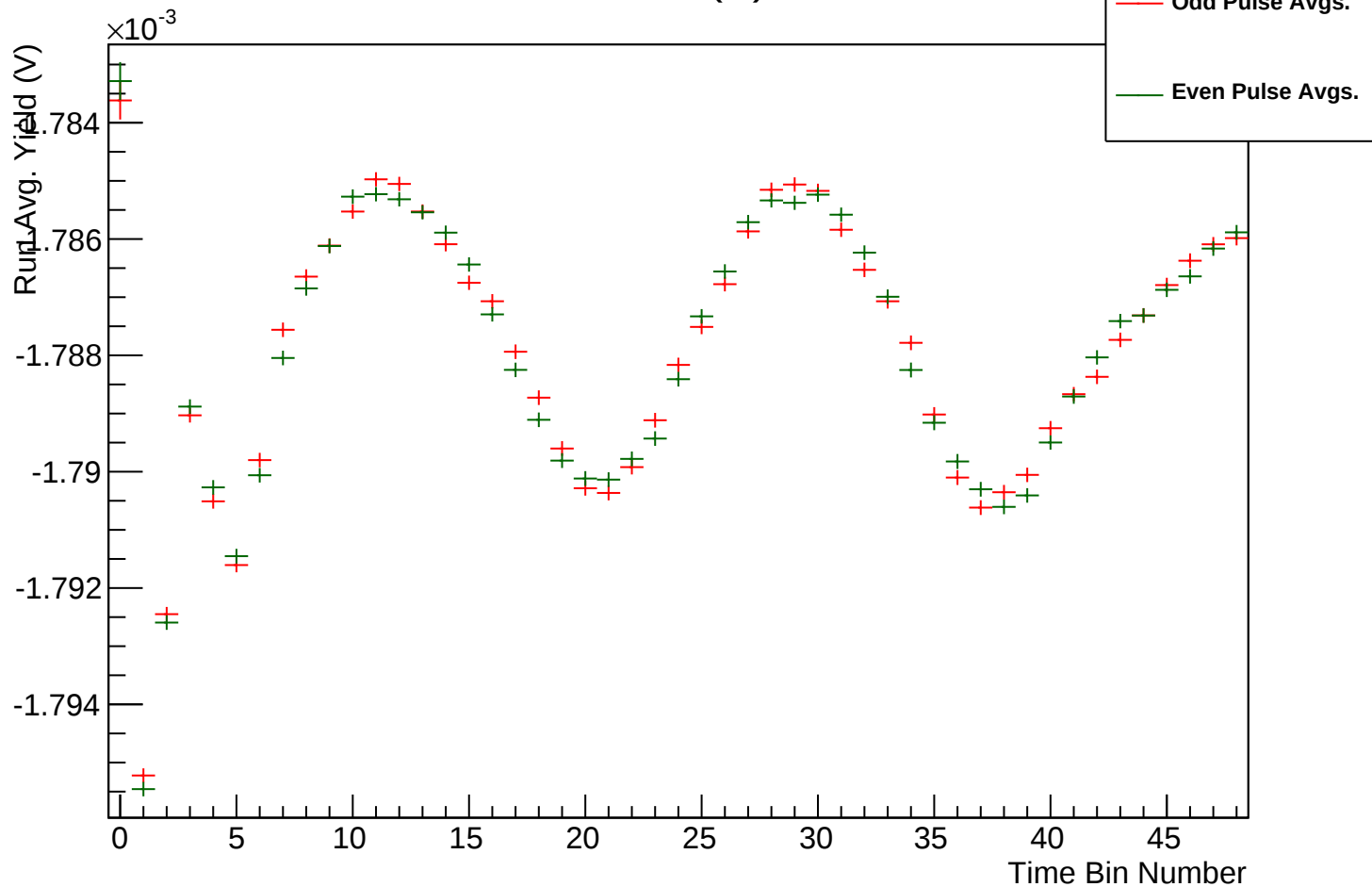
r17784-w59-Yield(V)-OddPulses



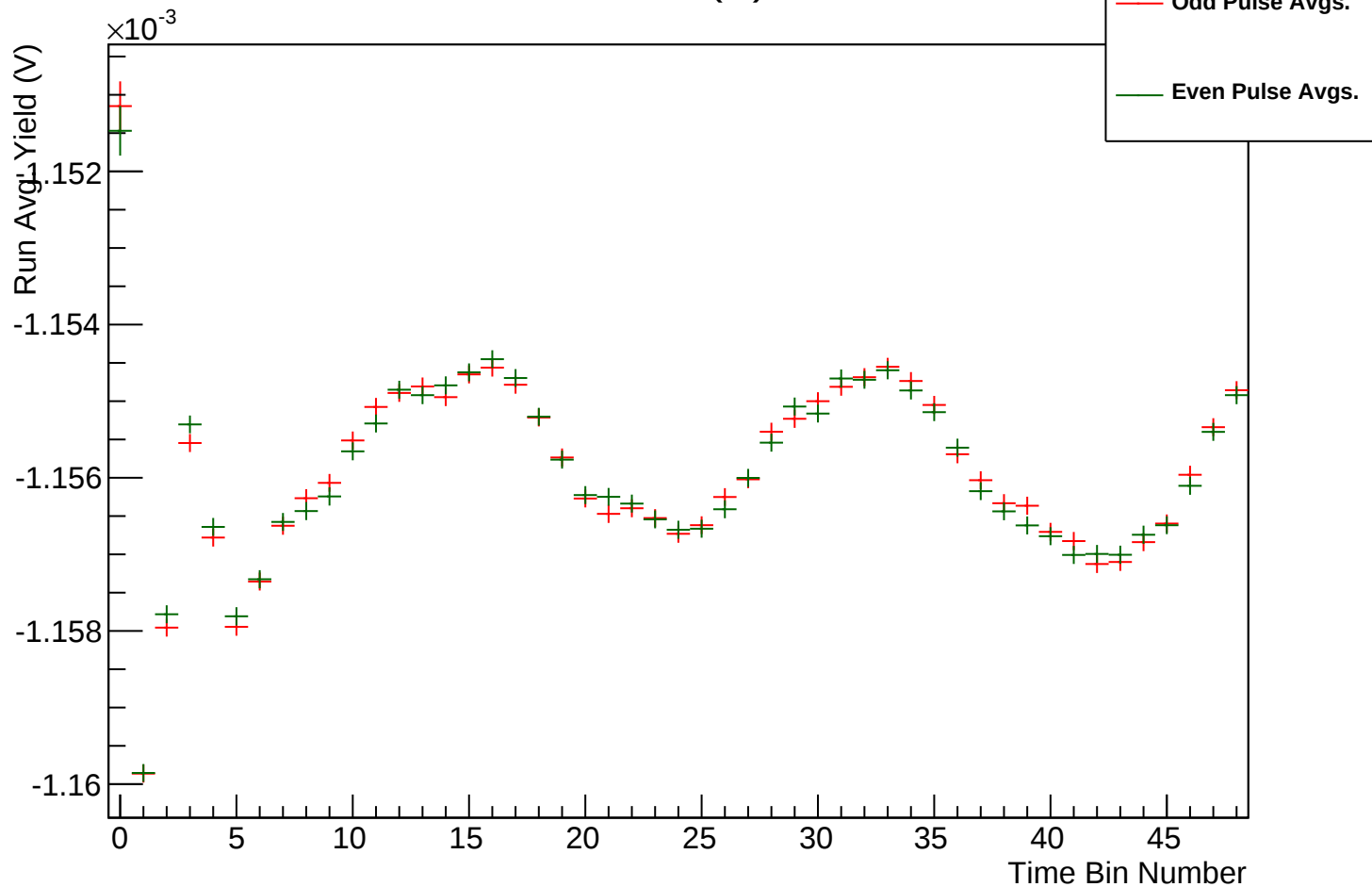
r17784-w60-Yield(V)-OddPulses



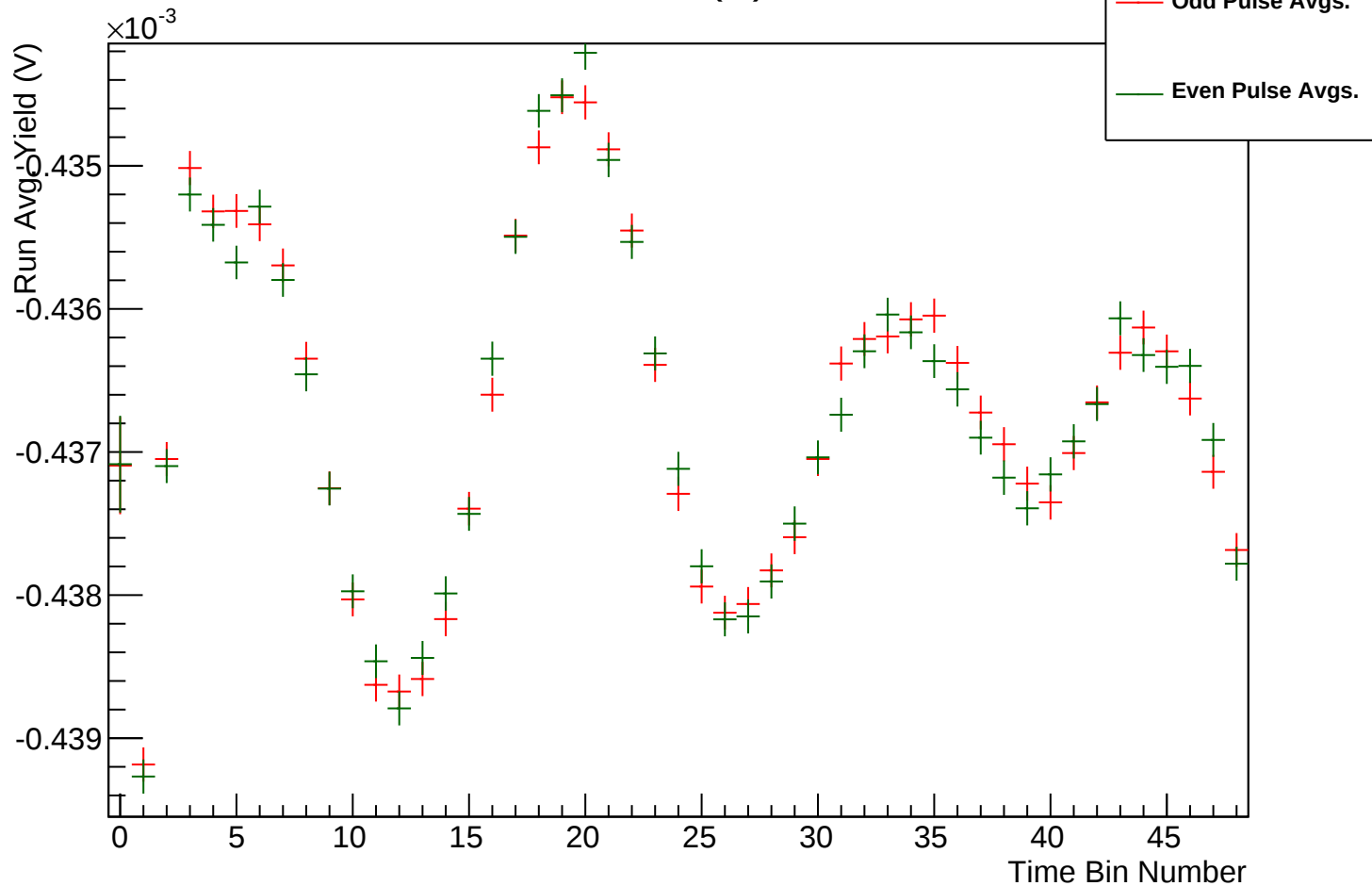
r17784-w61-Yield(V)-OddPulses



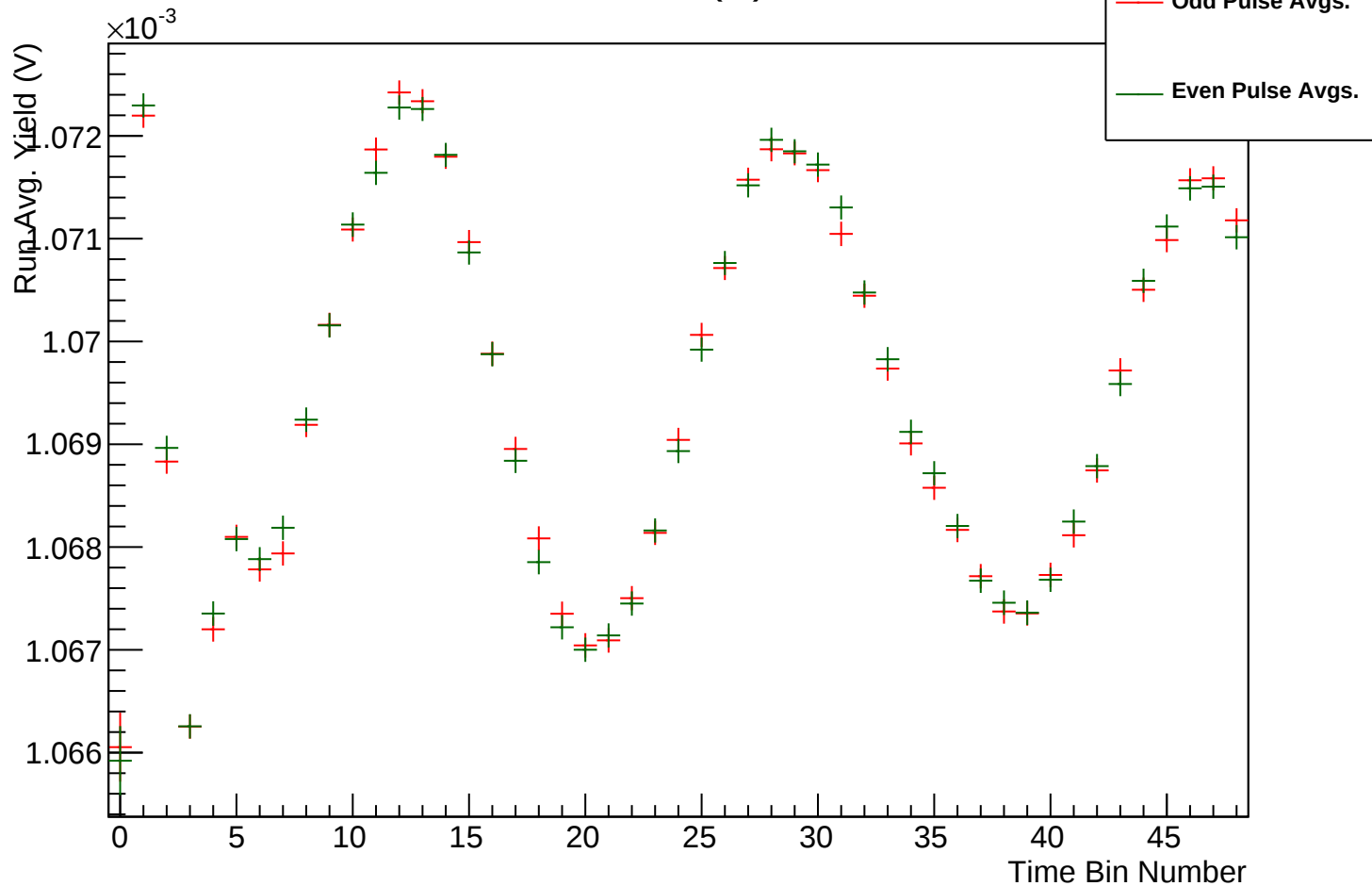
r17784-w62-Yield(V)-OddPulses



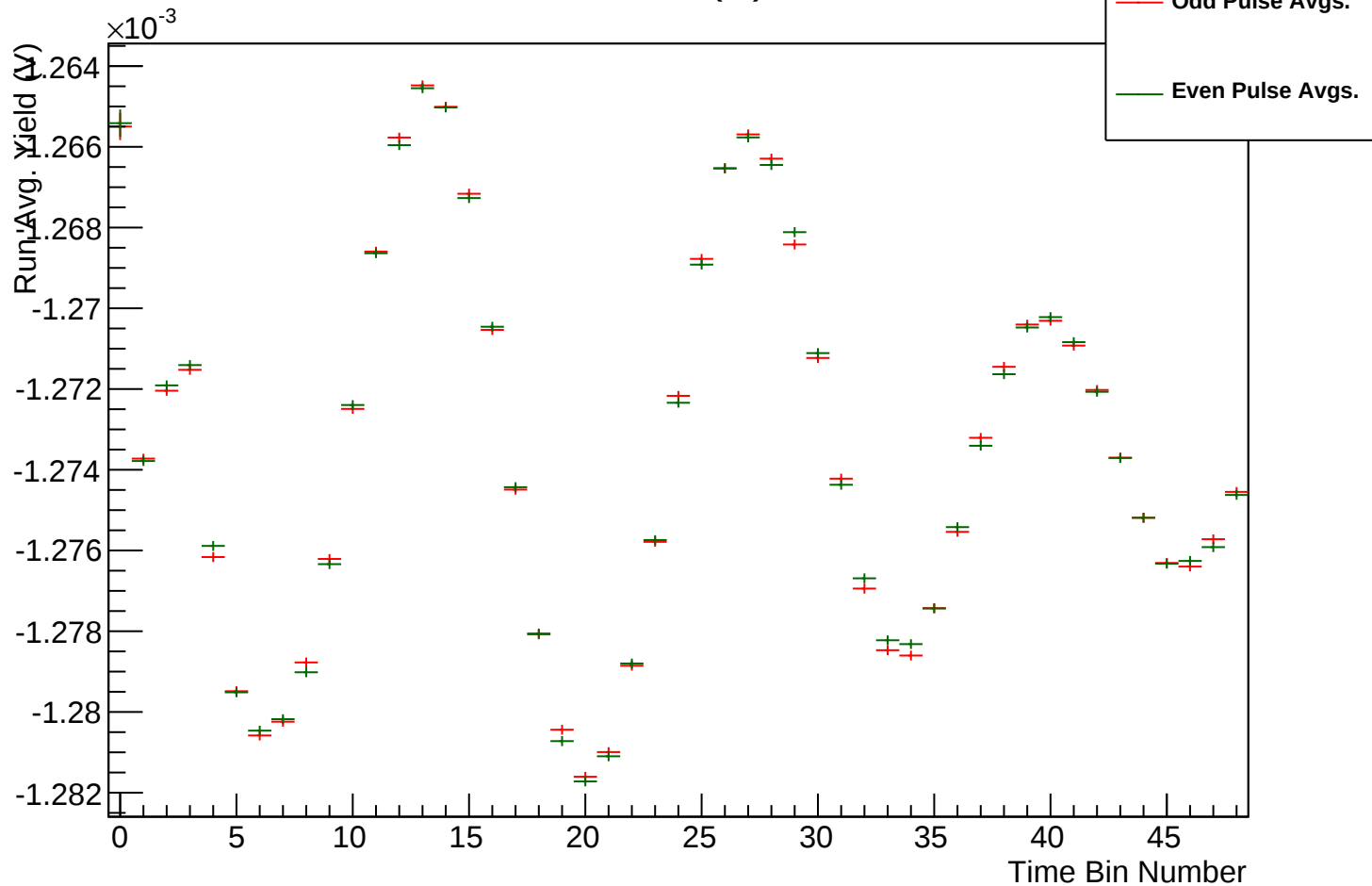
r17784-w63-Yield(V)-OddPulses



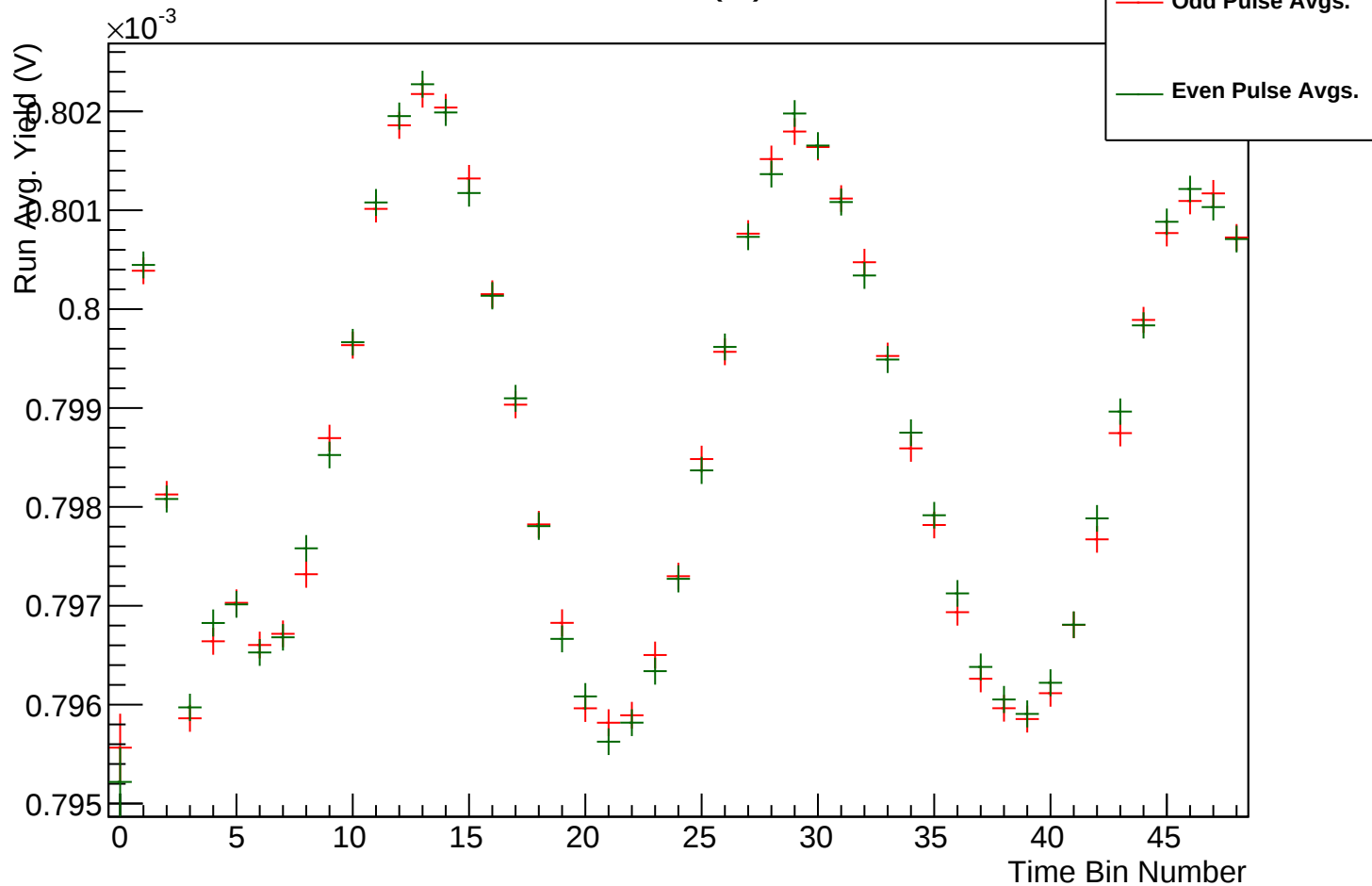
r17784-w64-Yield(V)-OddPulses



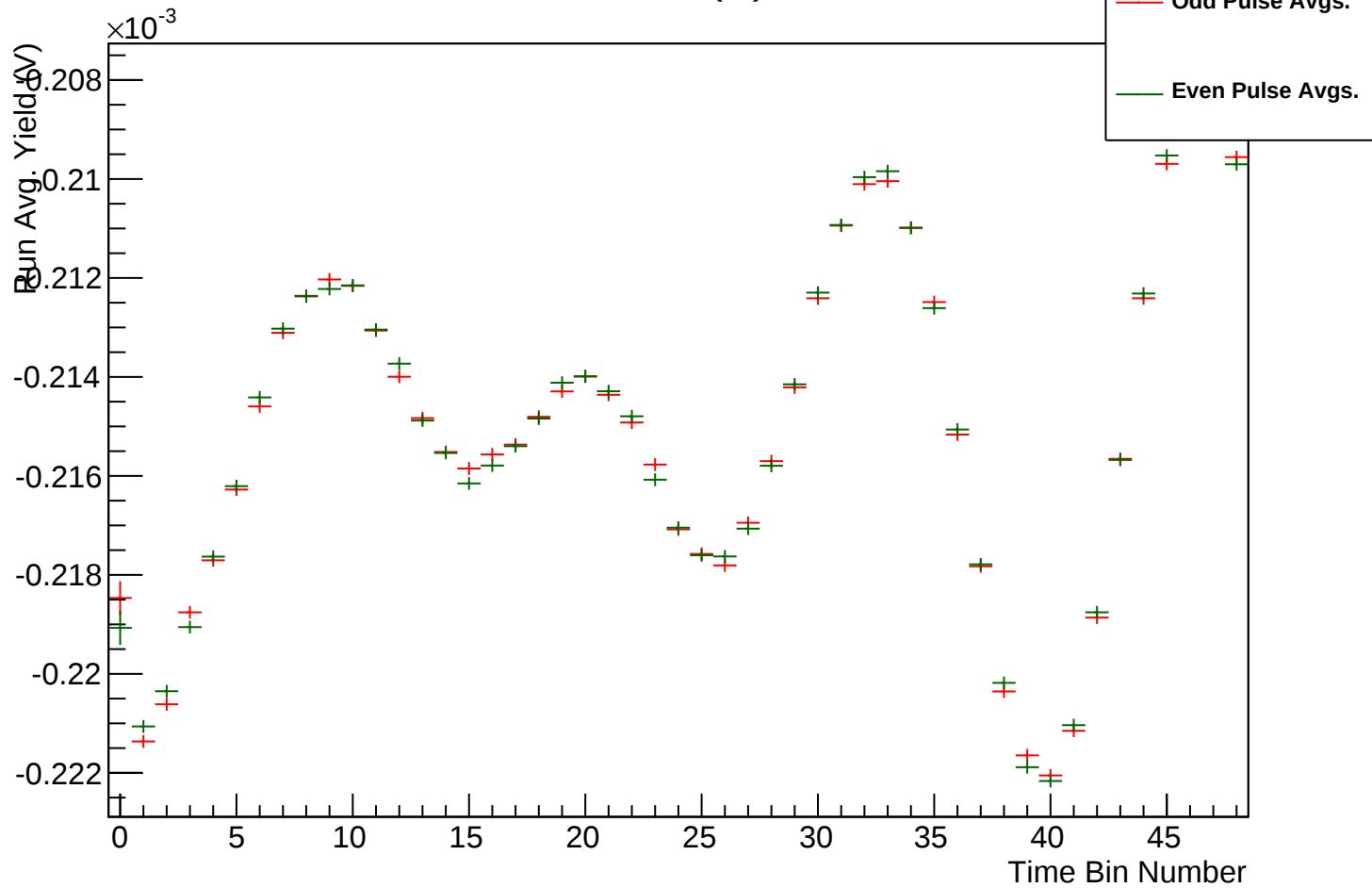
r17784-w65-Yield(V)-OddPulses



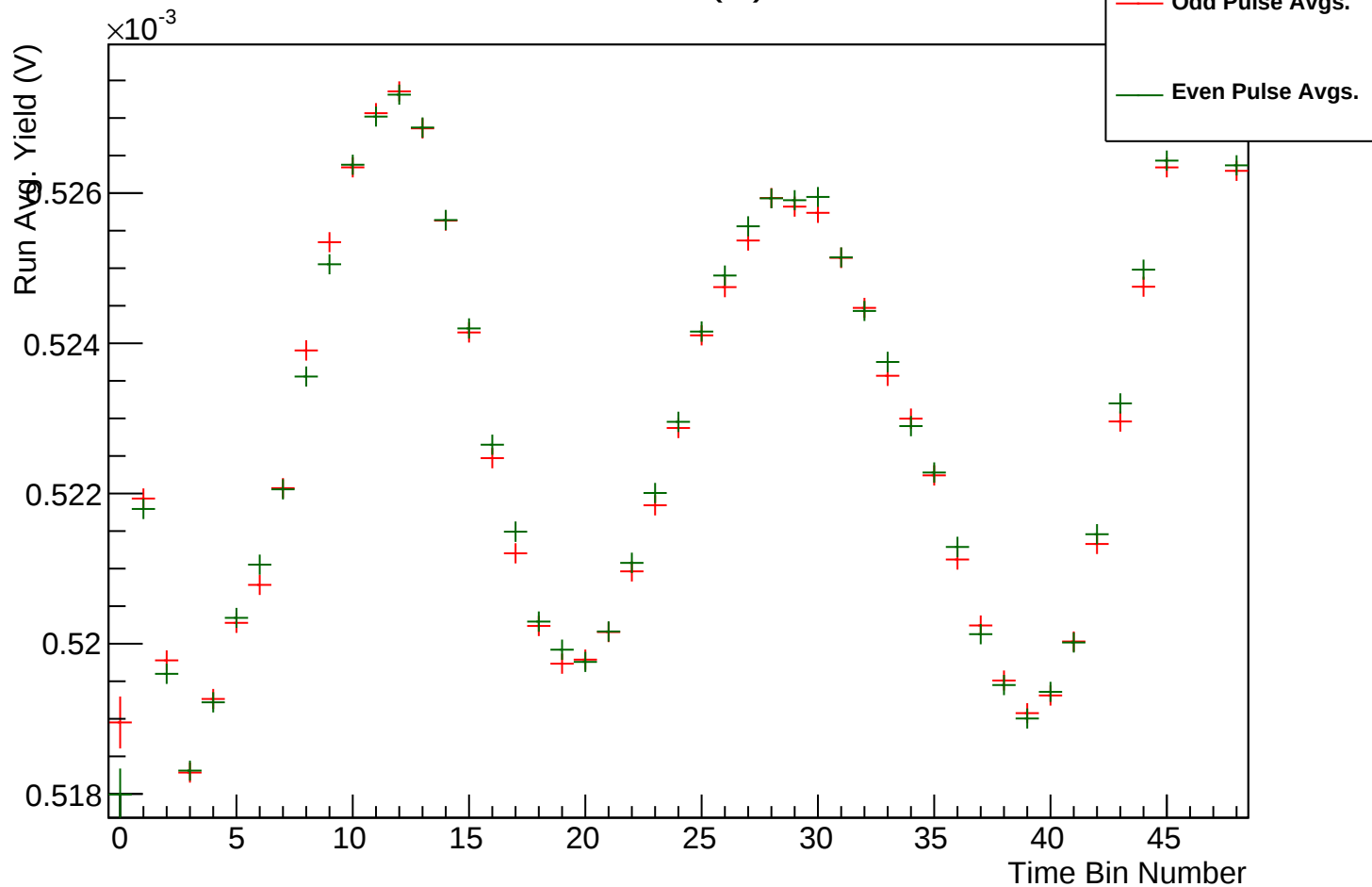
r17784-w66-Yield(V)-OddPulses



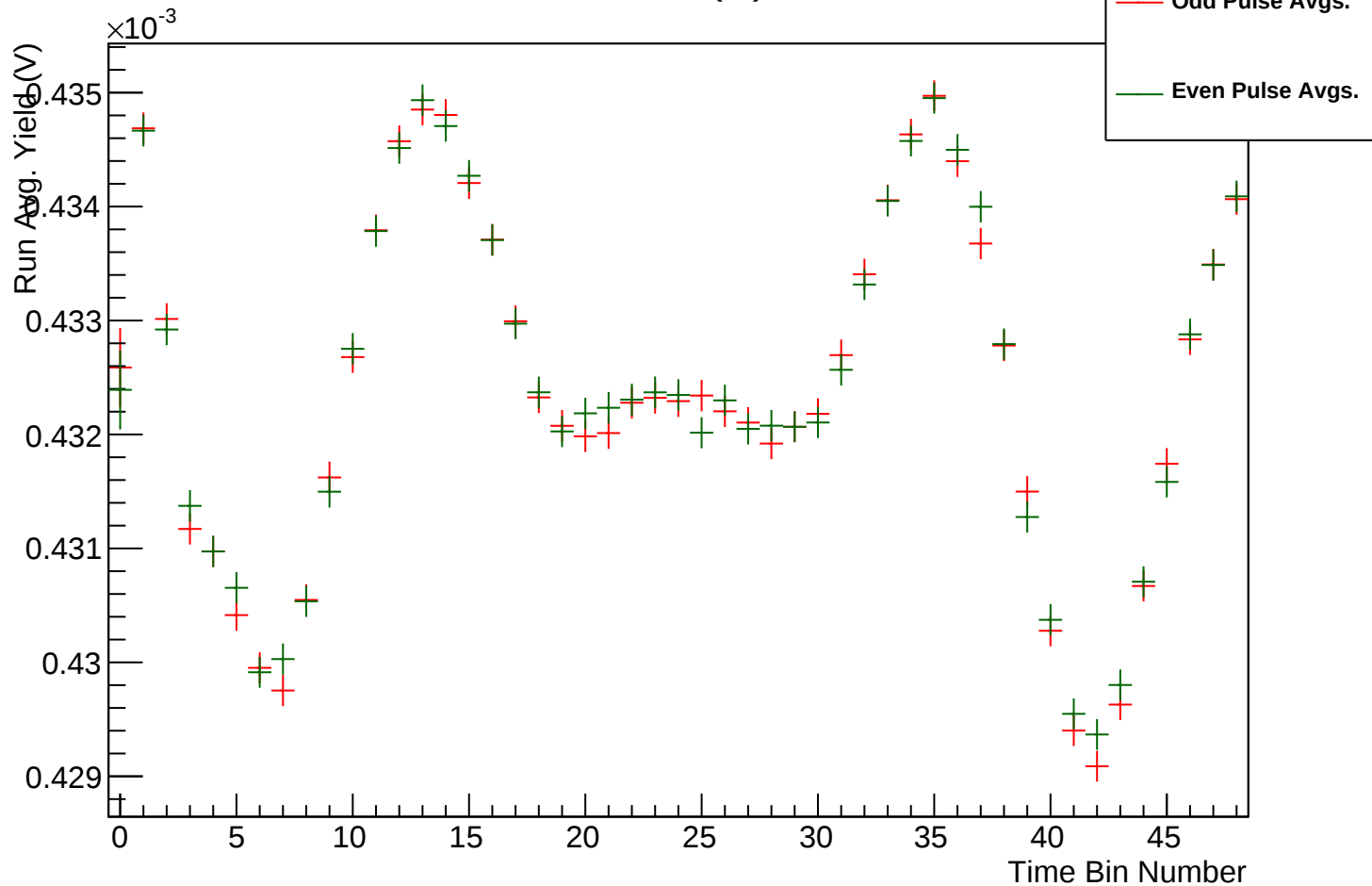
r17784-w67-Yield(V)-OddPulses



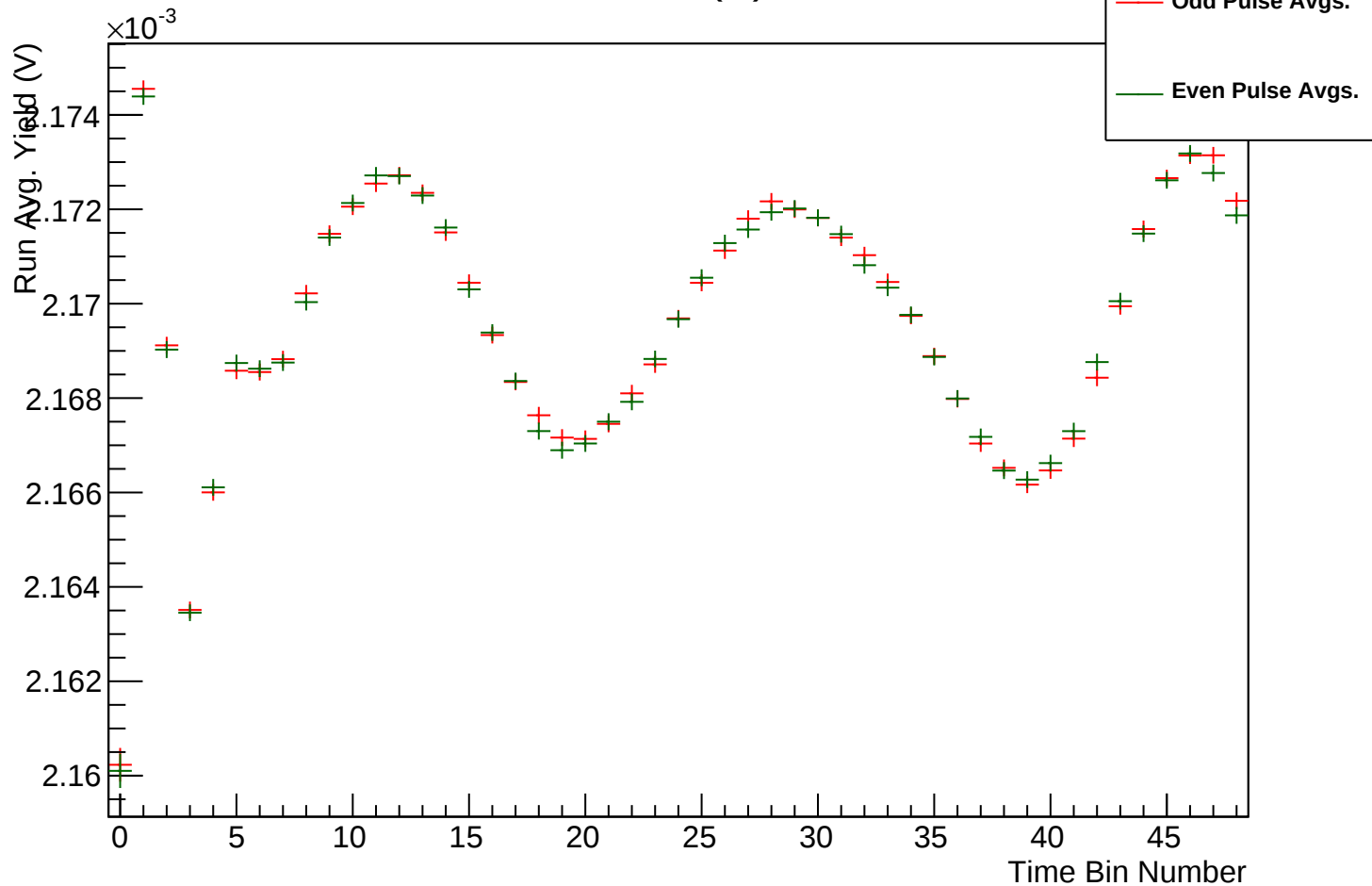
r17784-w68-Yield(V)-OddPulses



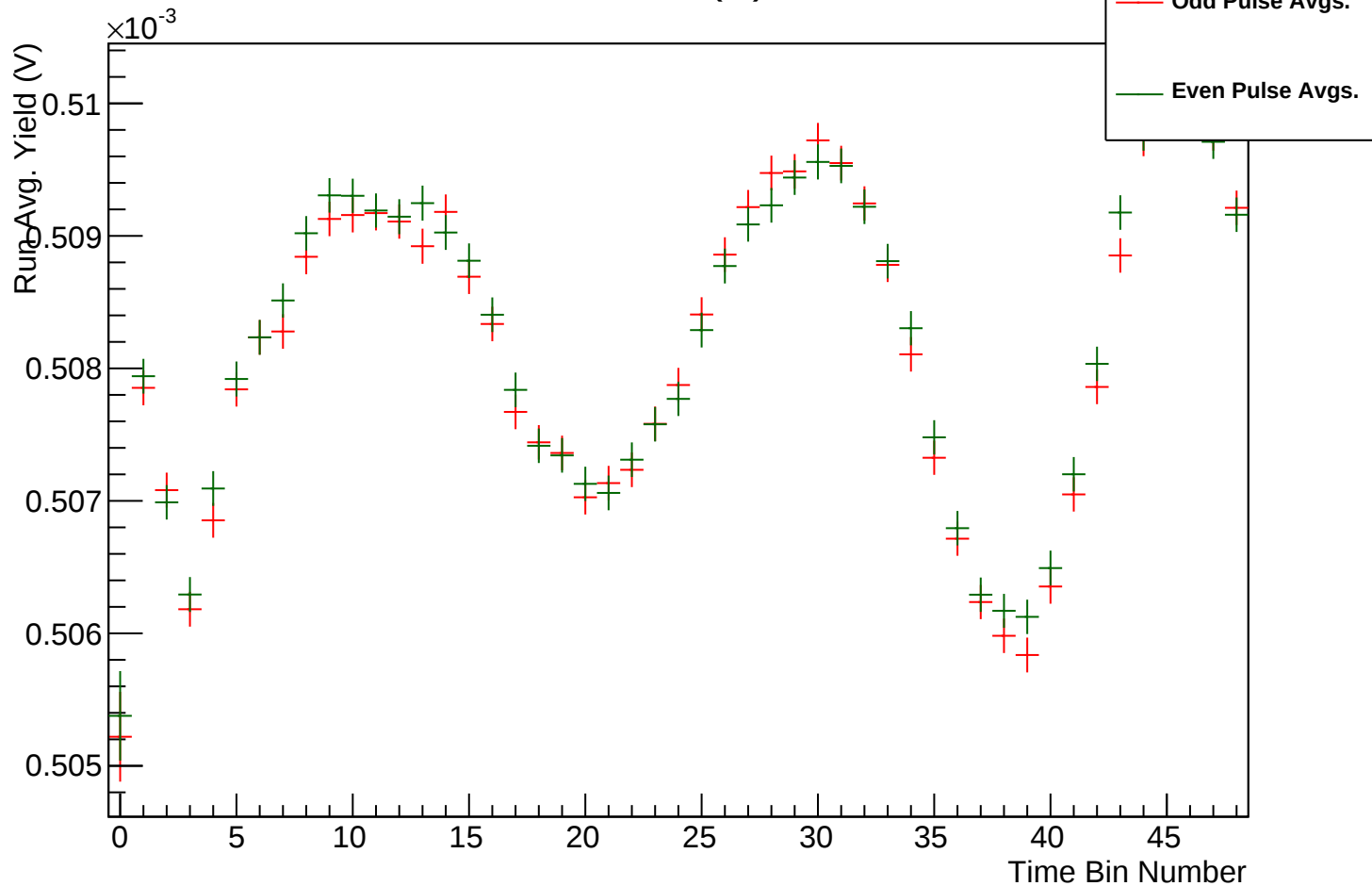
r17784-w69-Yield(V)-OddPulses



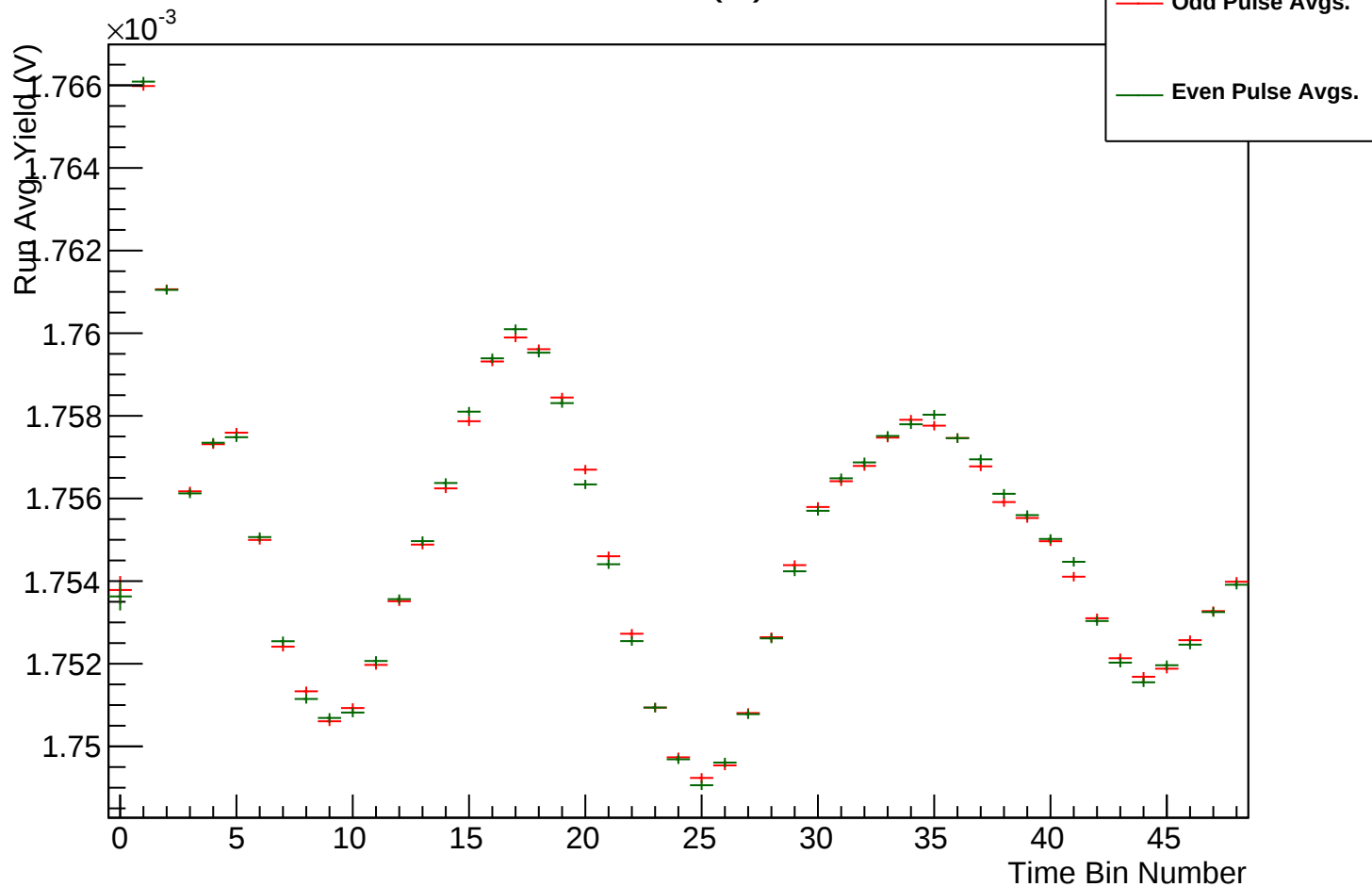
r17784-w70-Yield(V)-OddPulses



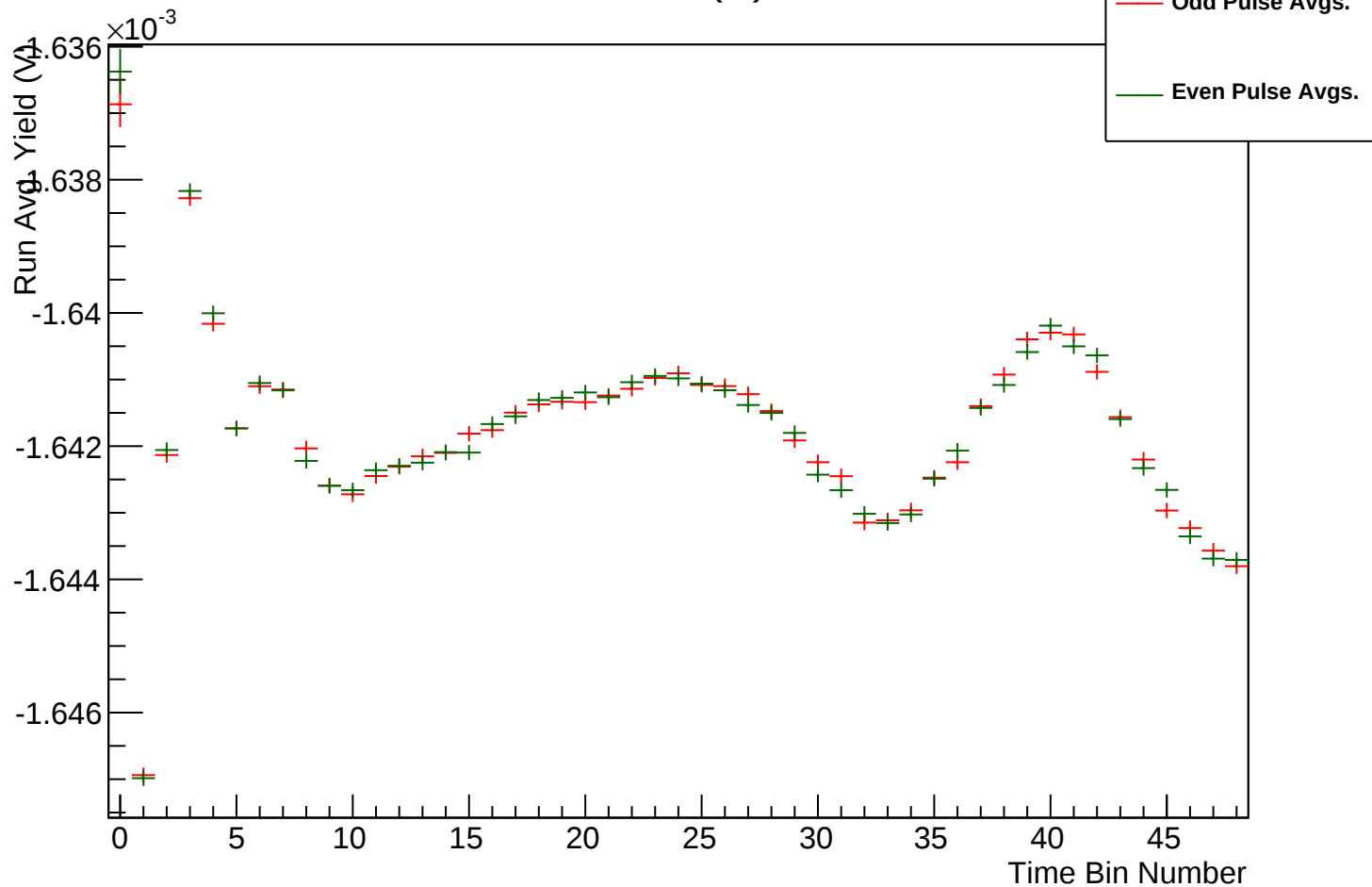
r17784-w71-Yield(V)-OddPulses



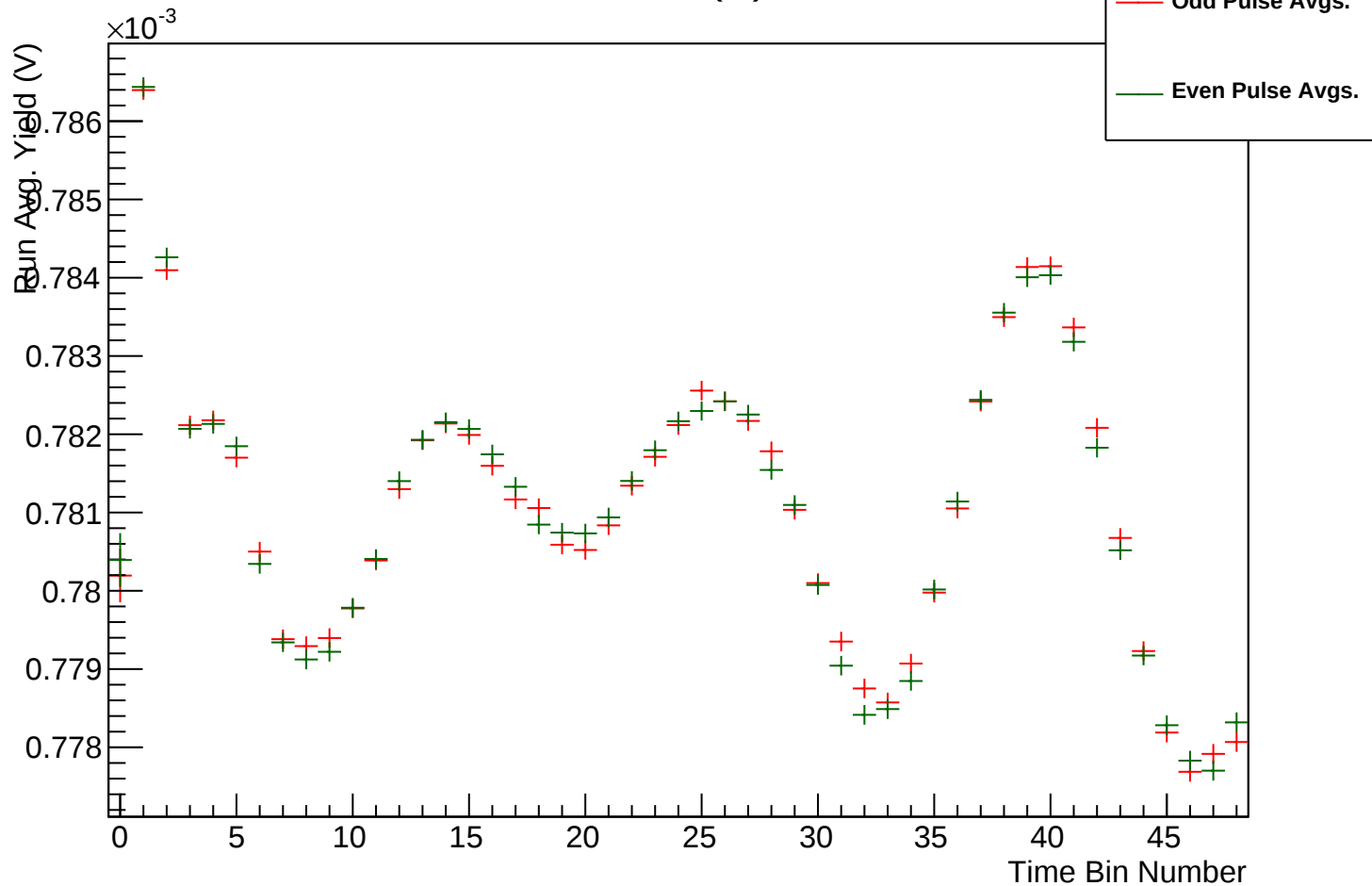
r17784-w72-Yield(V)-OddPulses



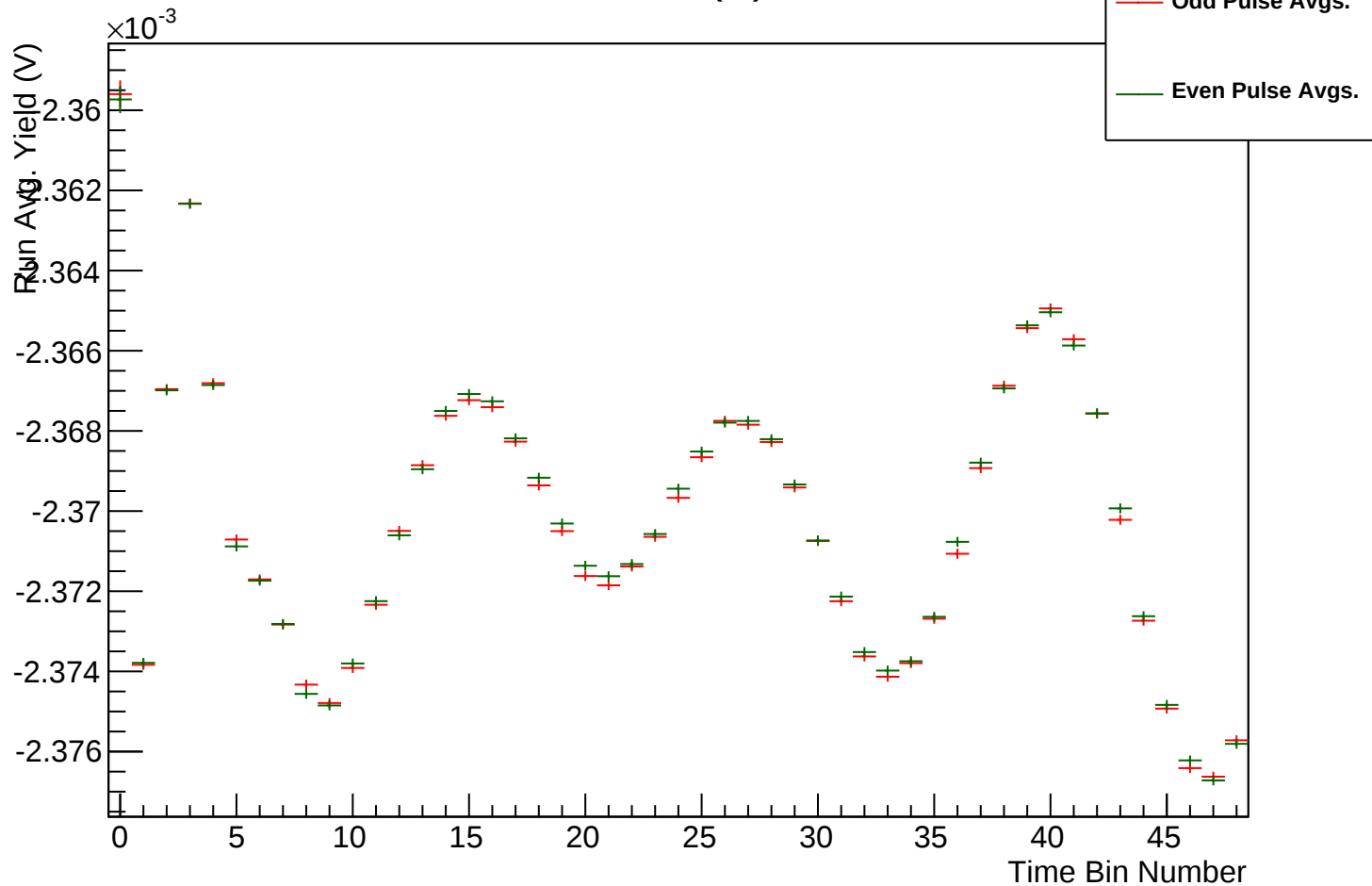
r17784-w73-Yield(V)-OddPulses



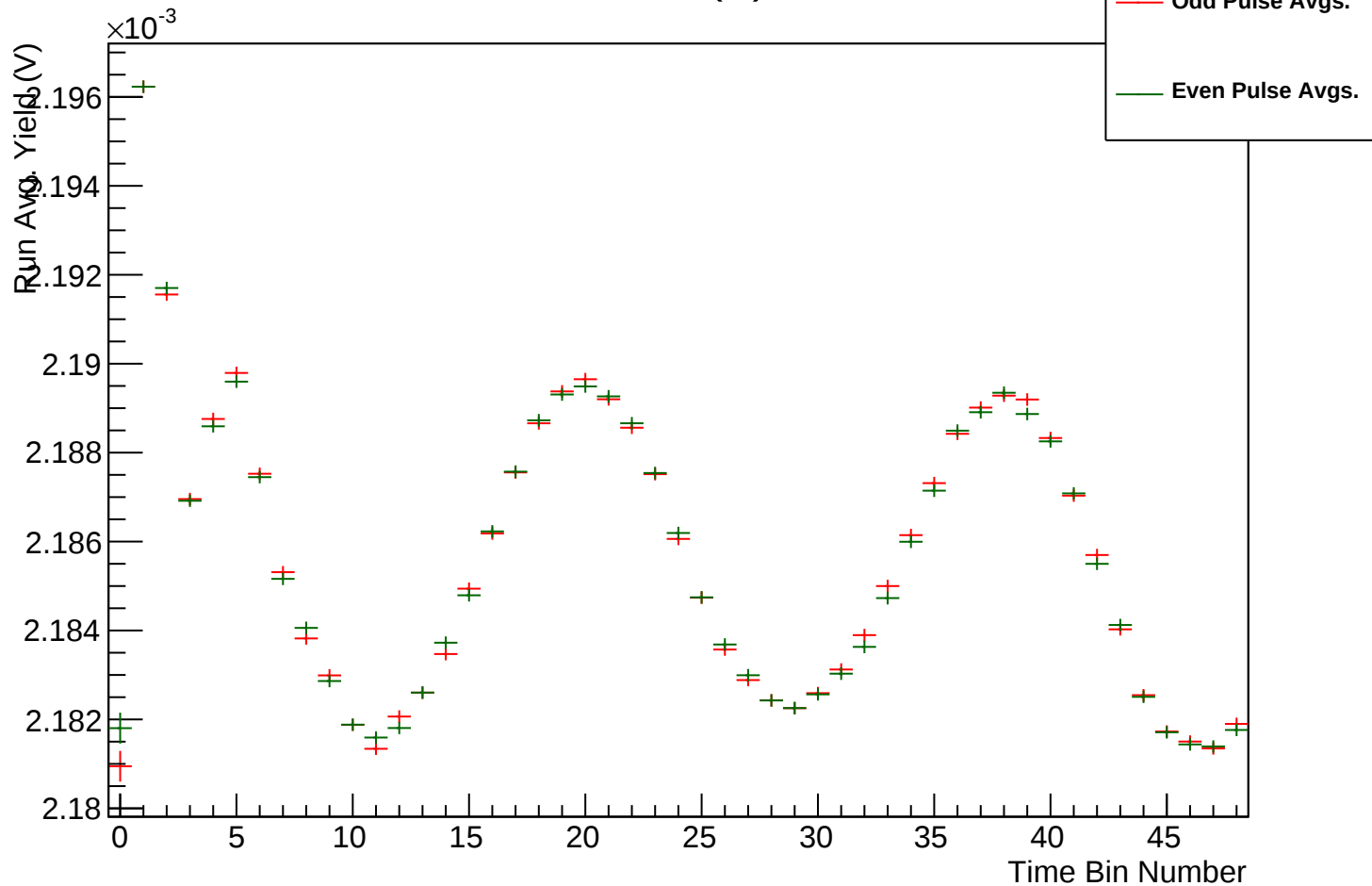
r17784-w74-Yield(V)-OddPulses



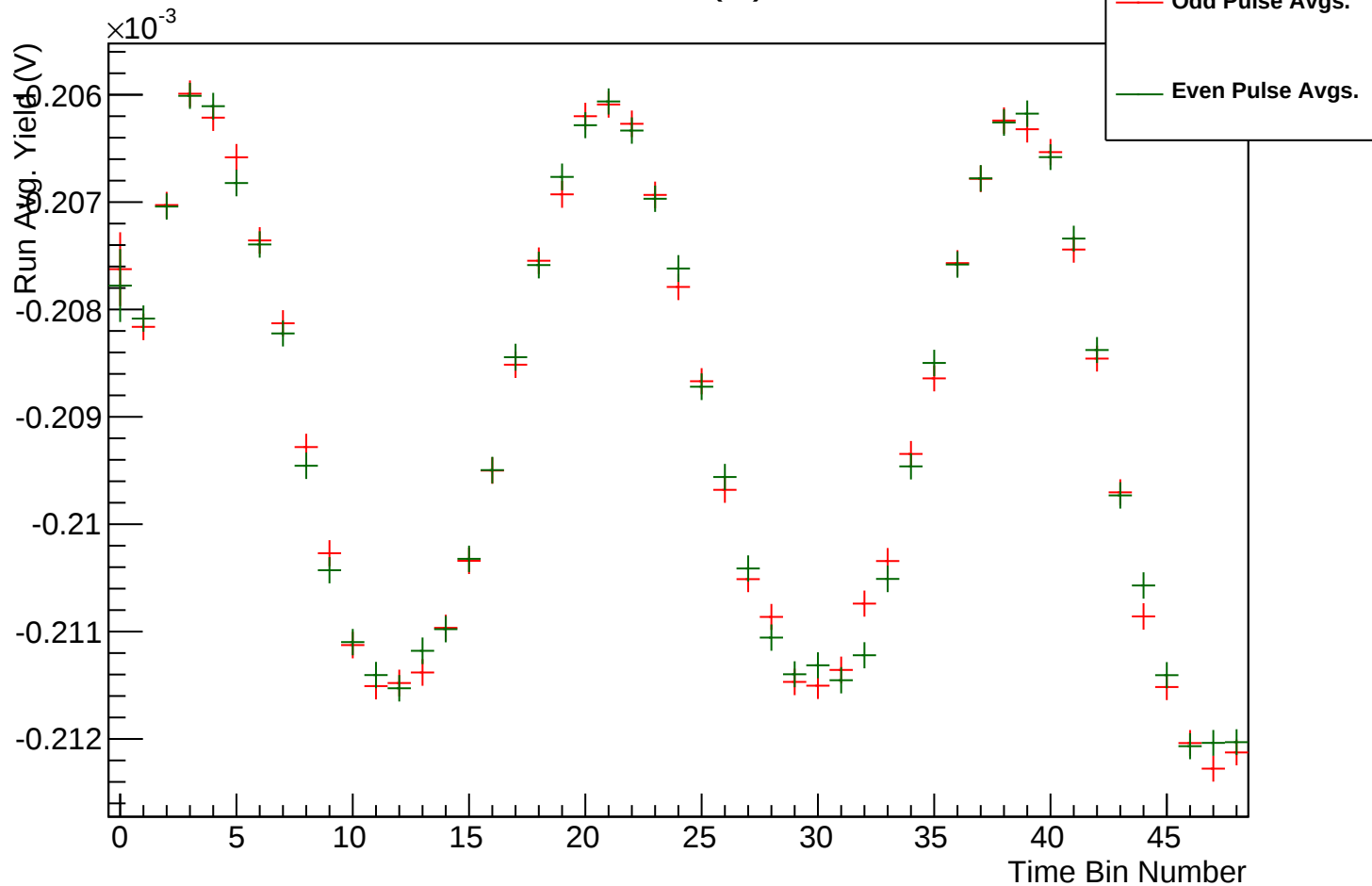
r17784-w75-Yield(V)-OddPulses



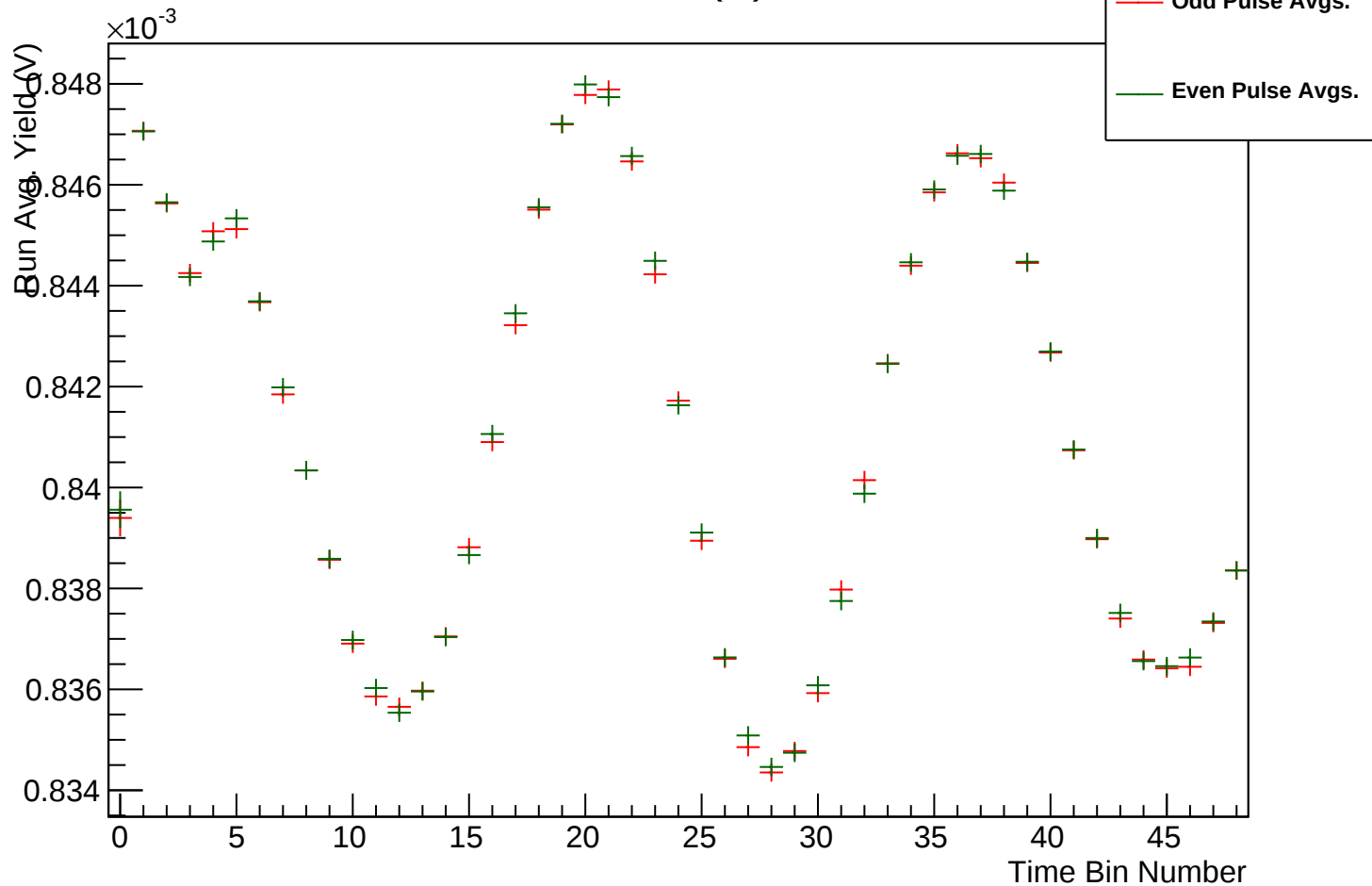
r17784-w76-Yield(V)-OddPulses



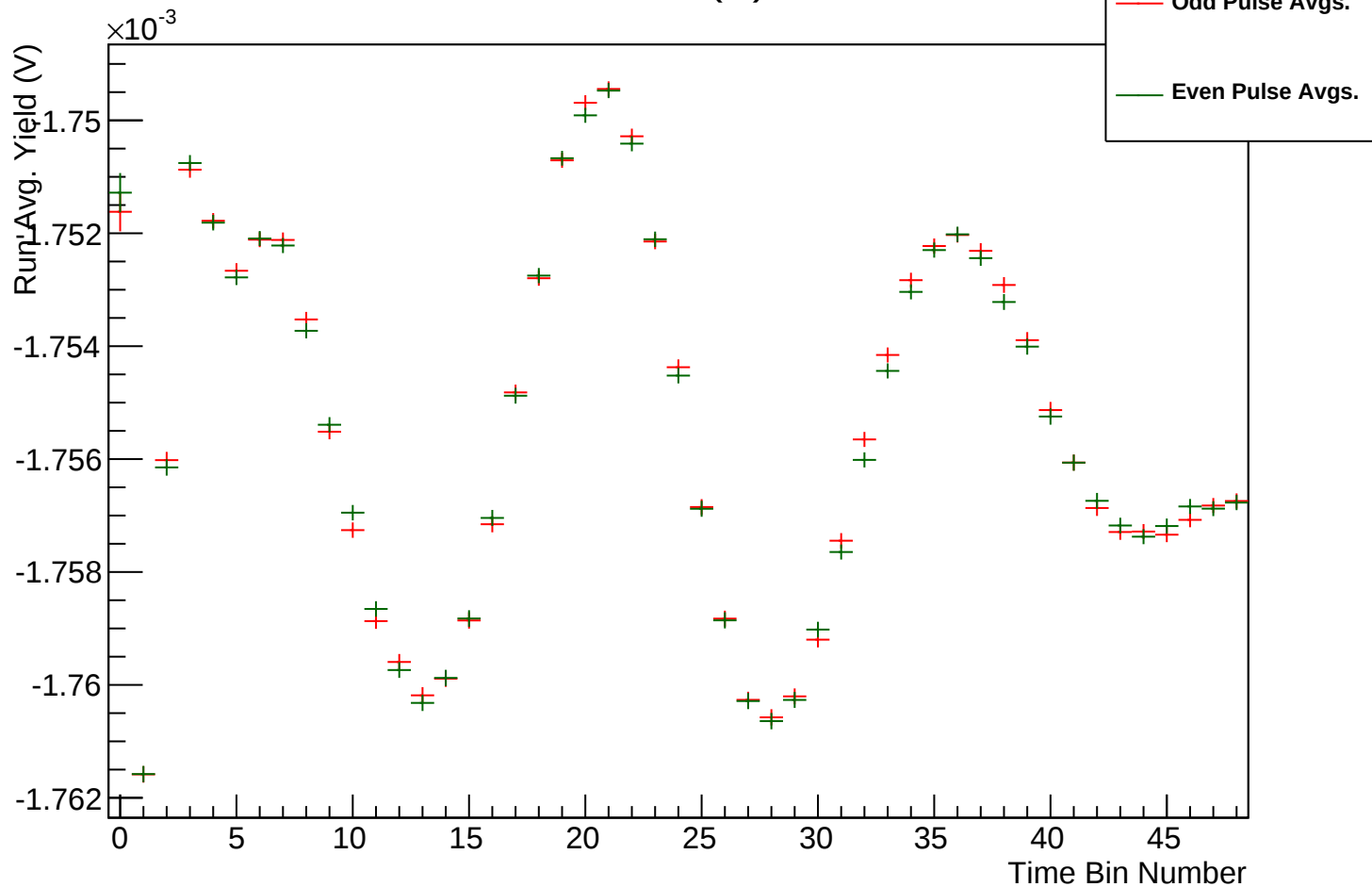
r17784-w77-Yield(V)-OddPulses



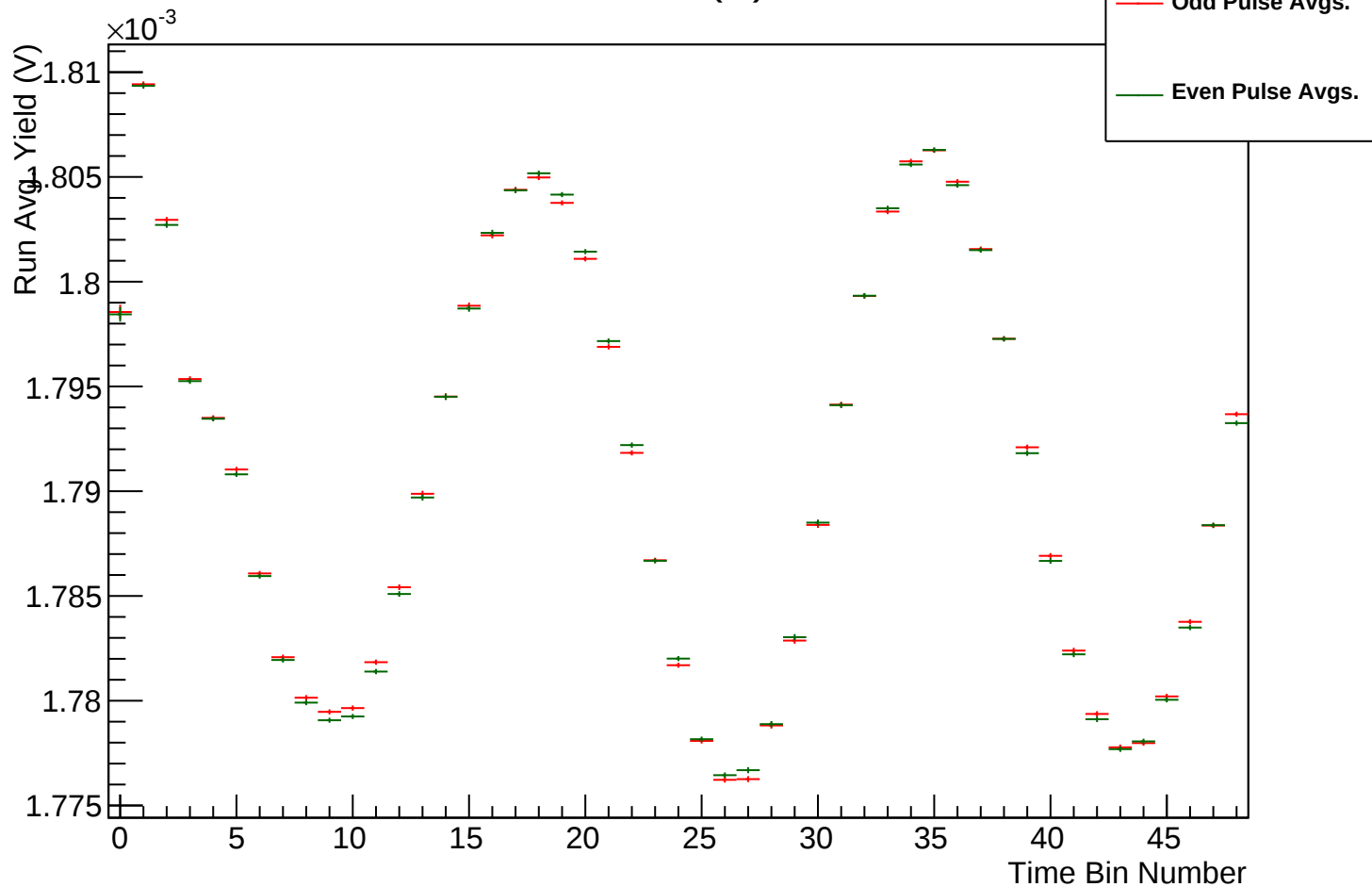
r17784-w78-Yield(V)-OddPulses



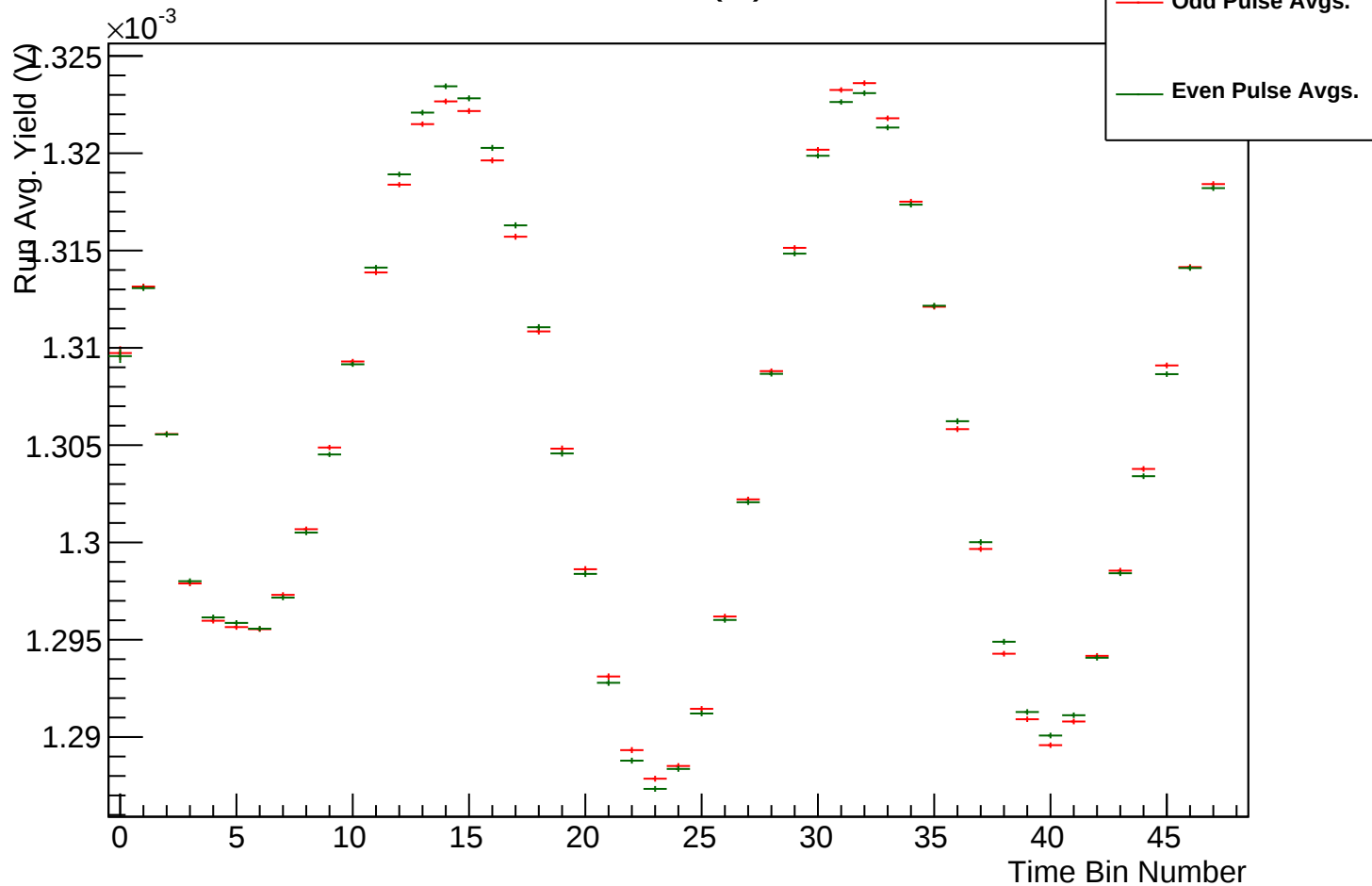
r17784-w79-Yield(V)-OddPulses



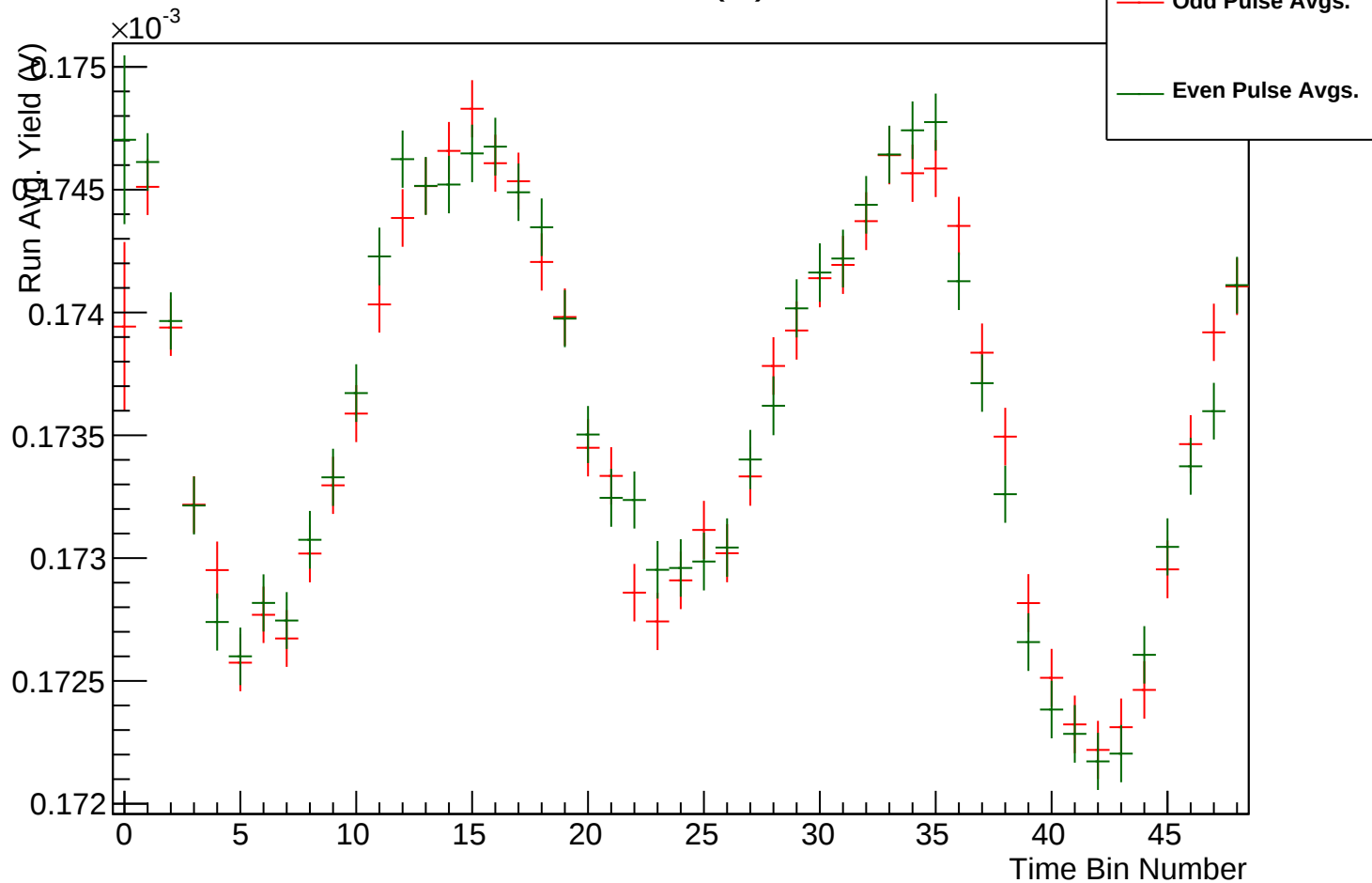
r17784-w80-Yield(V)-OddPulses



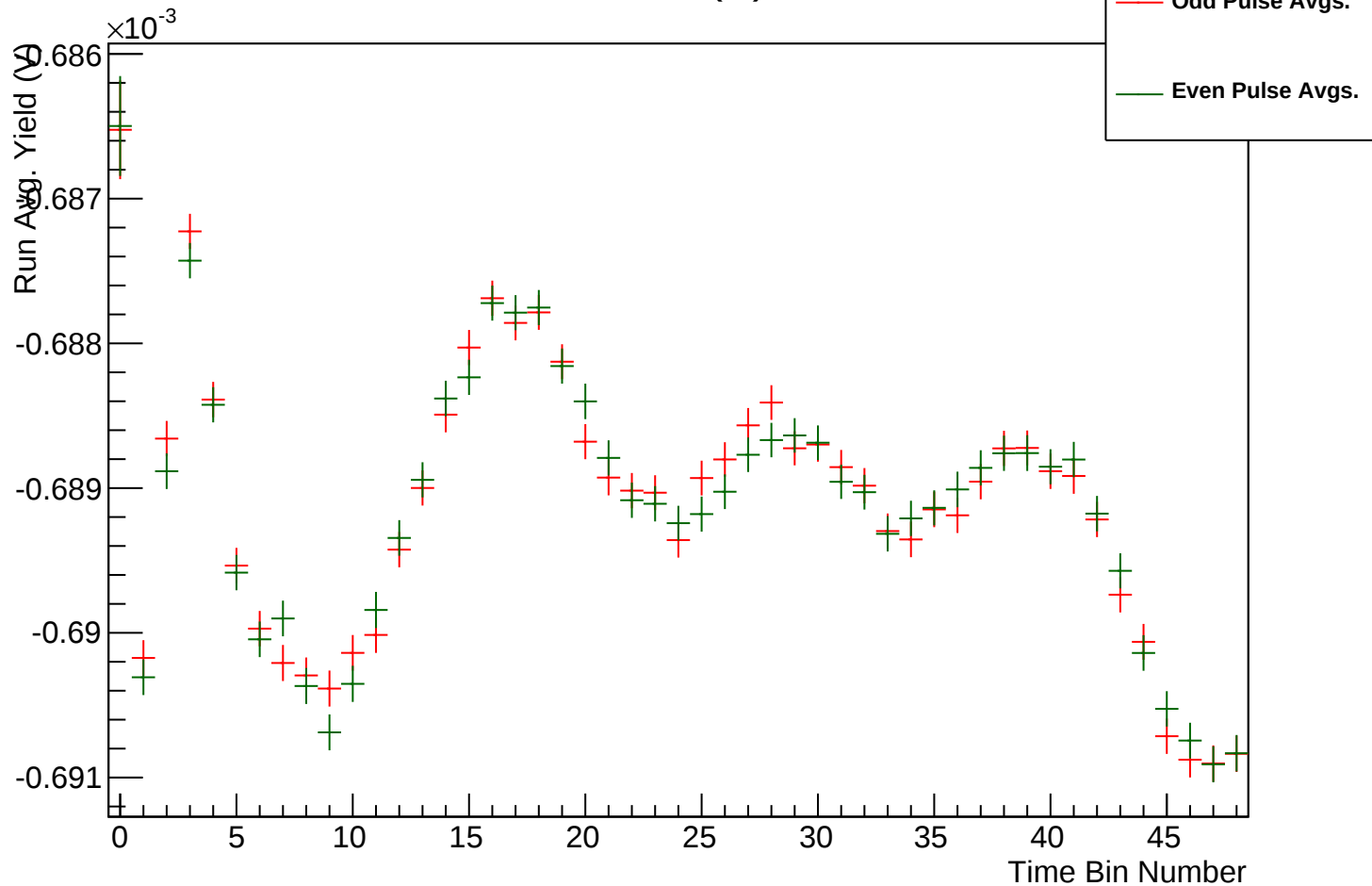
r17784-w81-Yield(V)-OddPulses



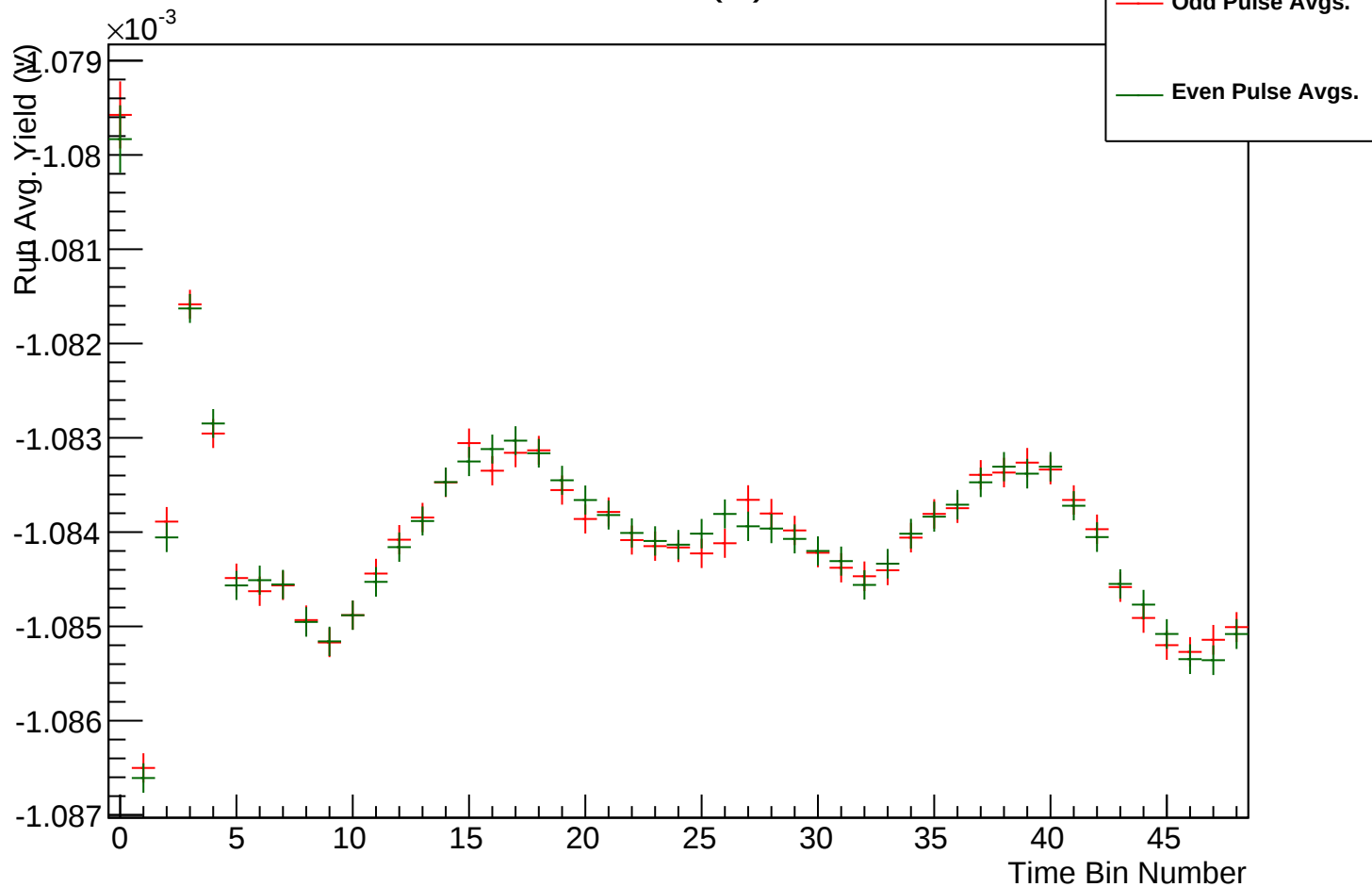
r17784-w82-Yield(V)-OddPulses



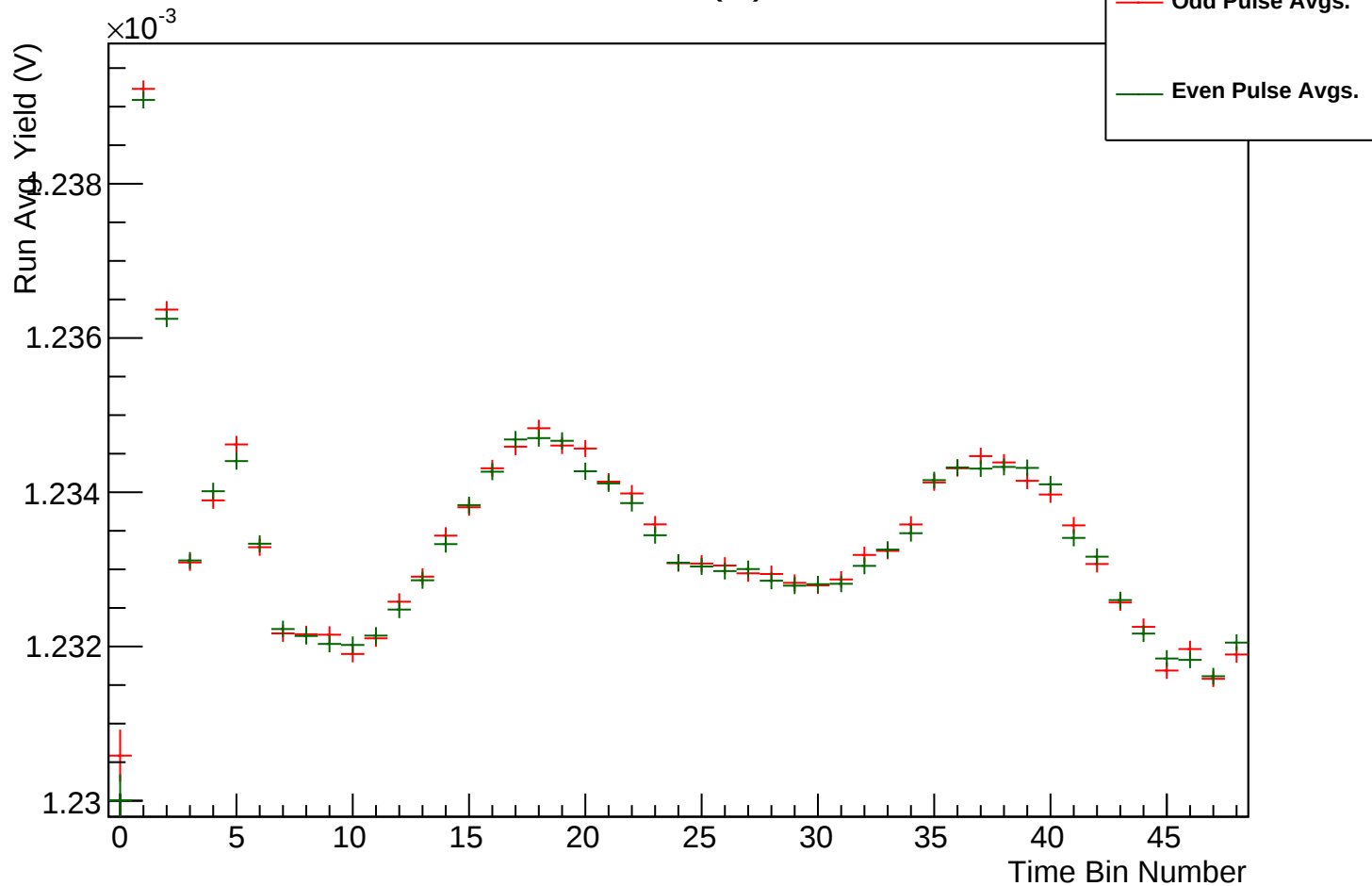
r17784-w83-Yield(V)-OddPulses



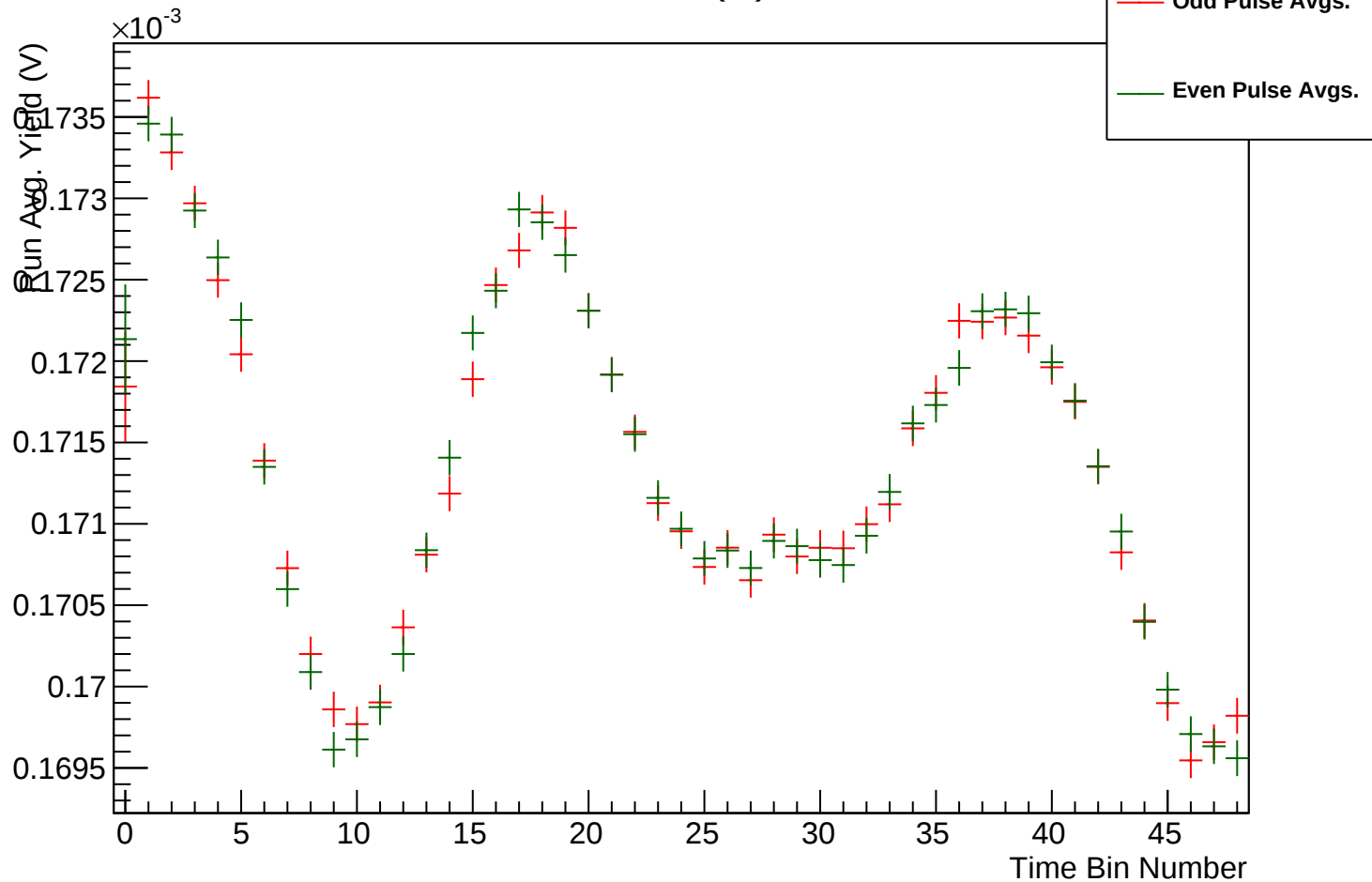
r17784-w84-Yield(V)-OddPulses



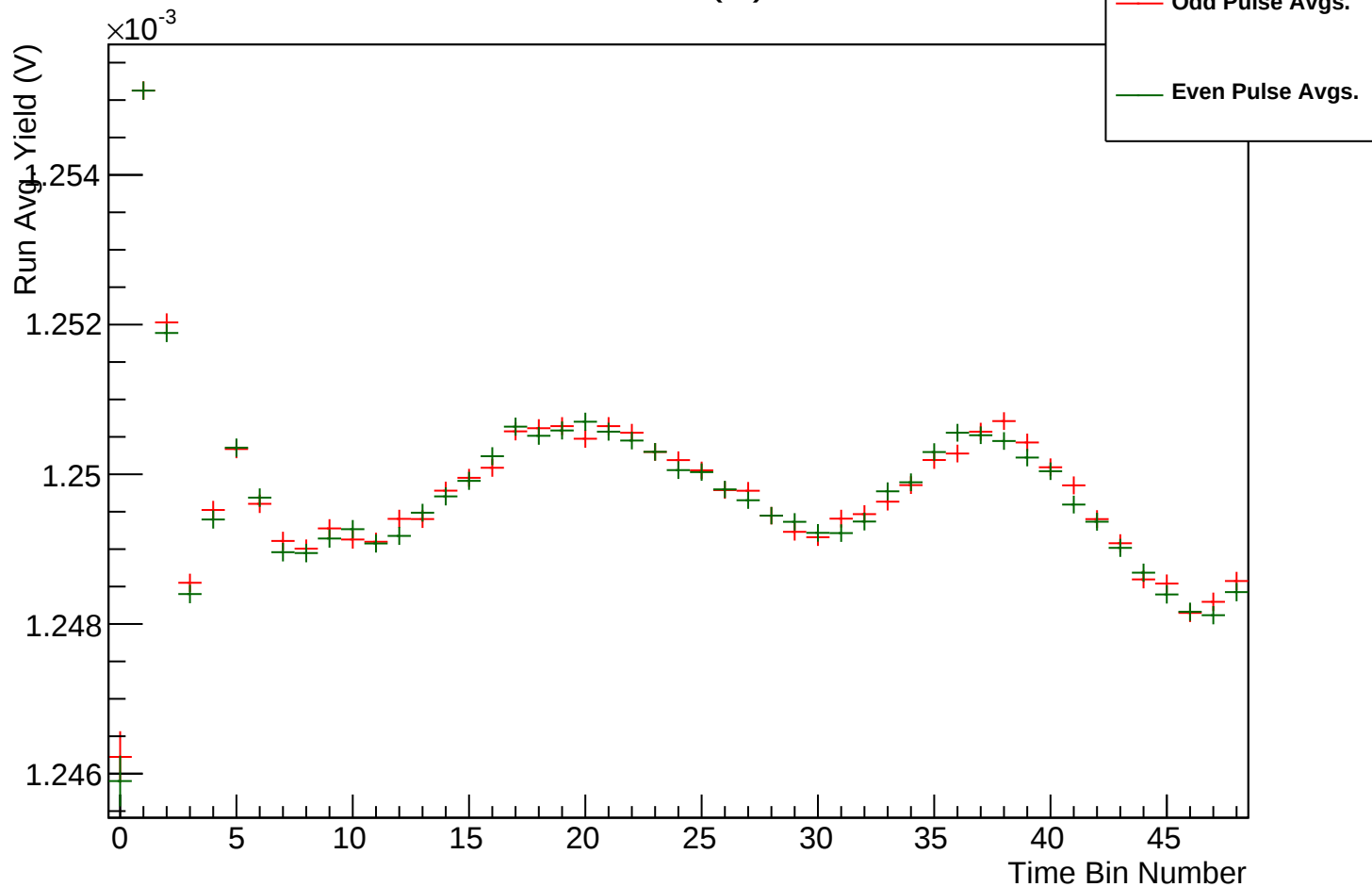
r17784-w85-Yield(V)-OddPulses



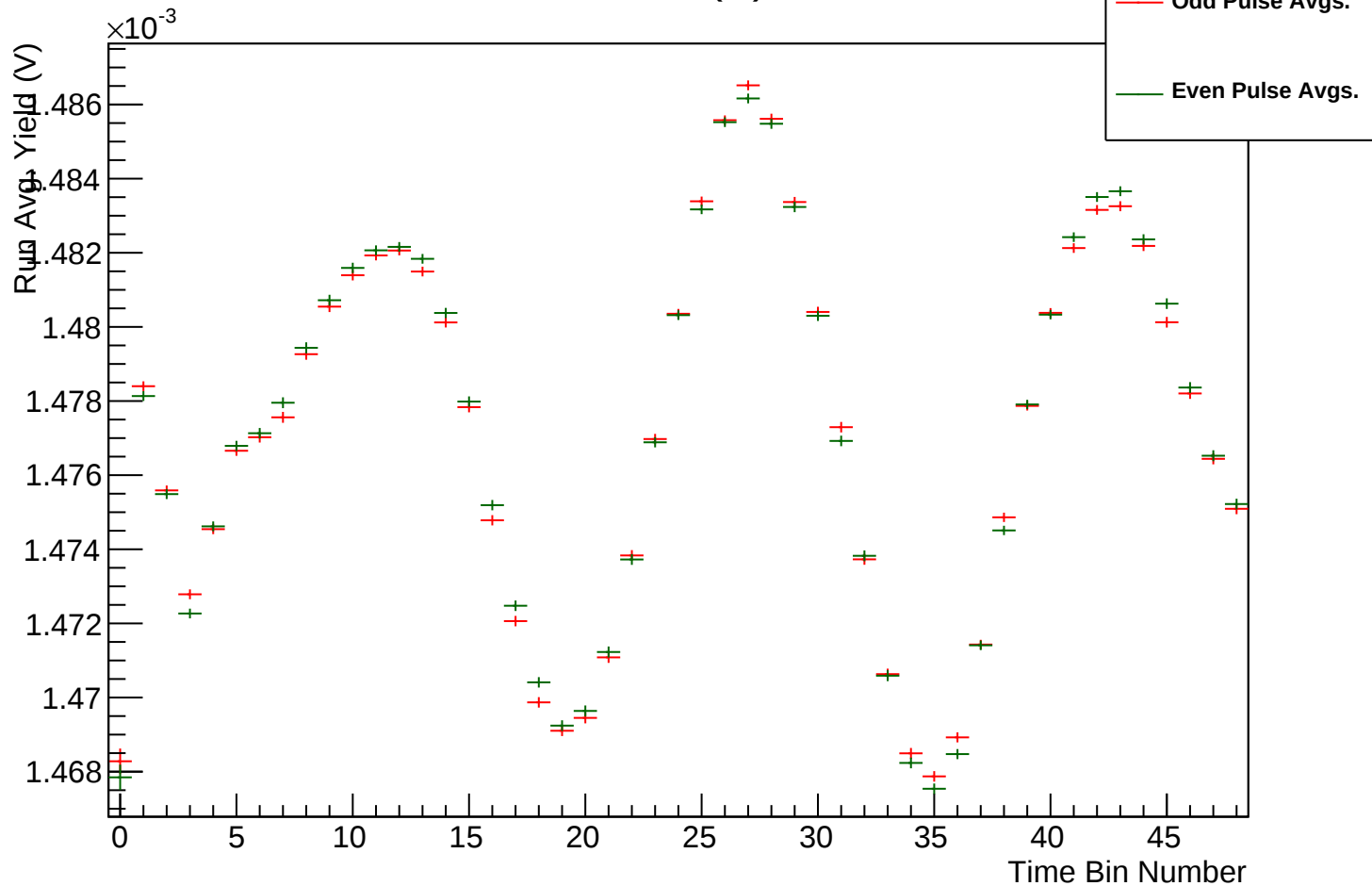
r17784-w86-Yield(V)-OddPulses



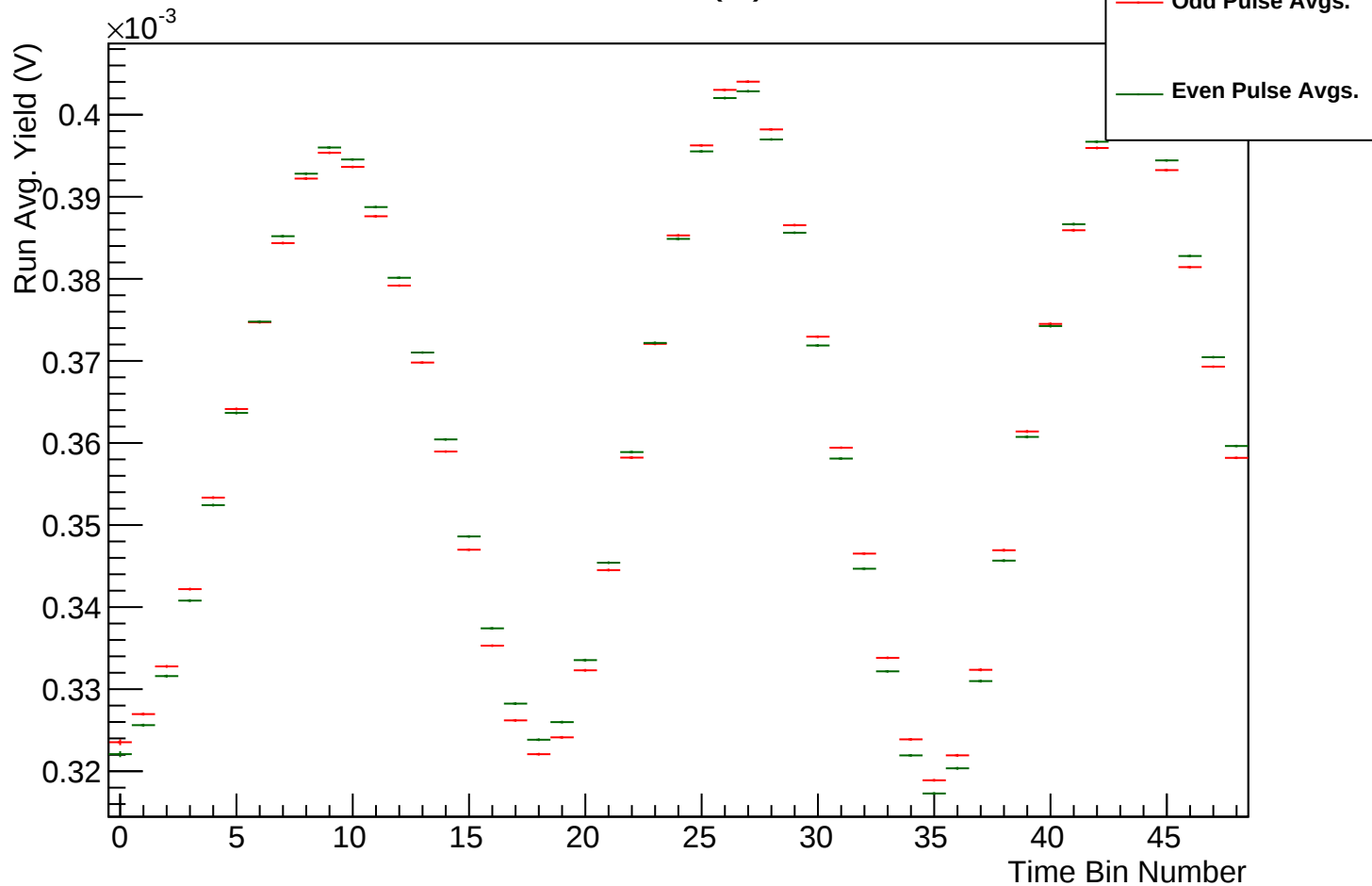
r17784-w87-Yield(V)-OddPulses



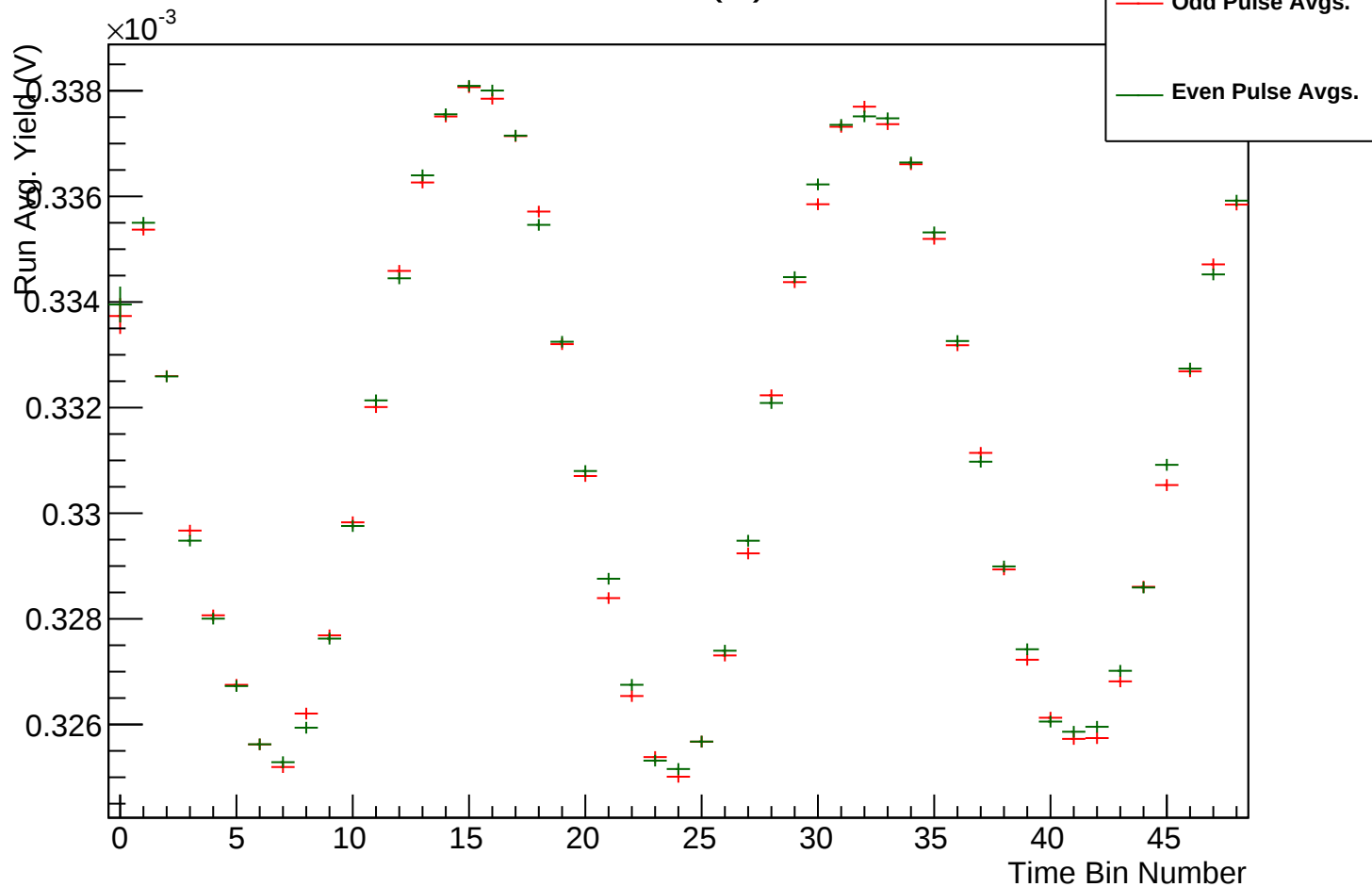
r17784-w88-Yield(V)-OddPulses



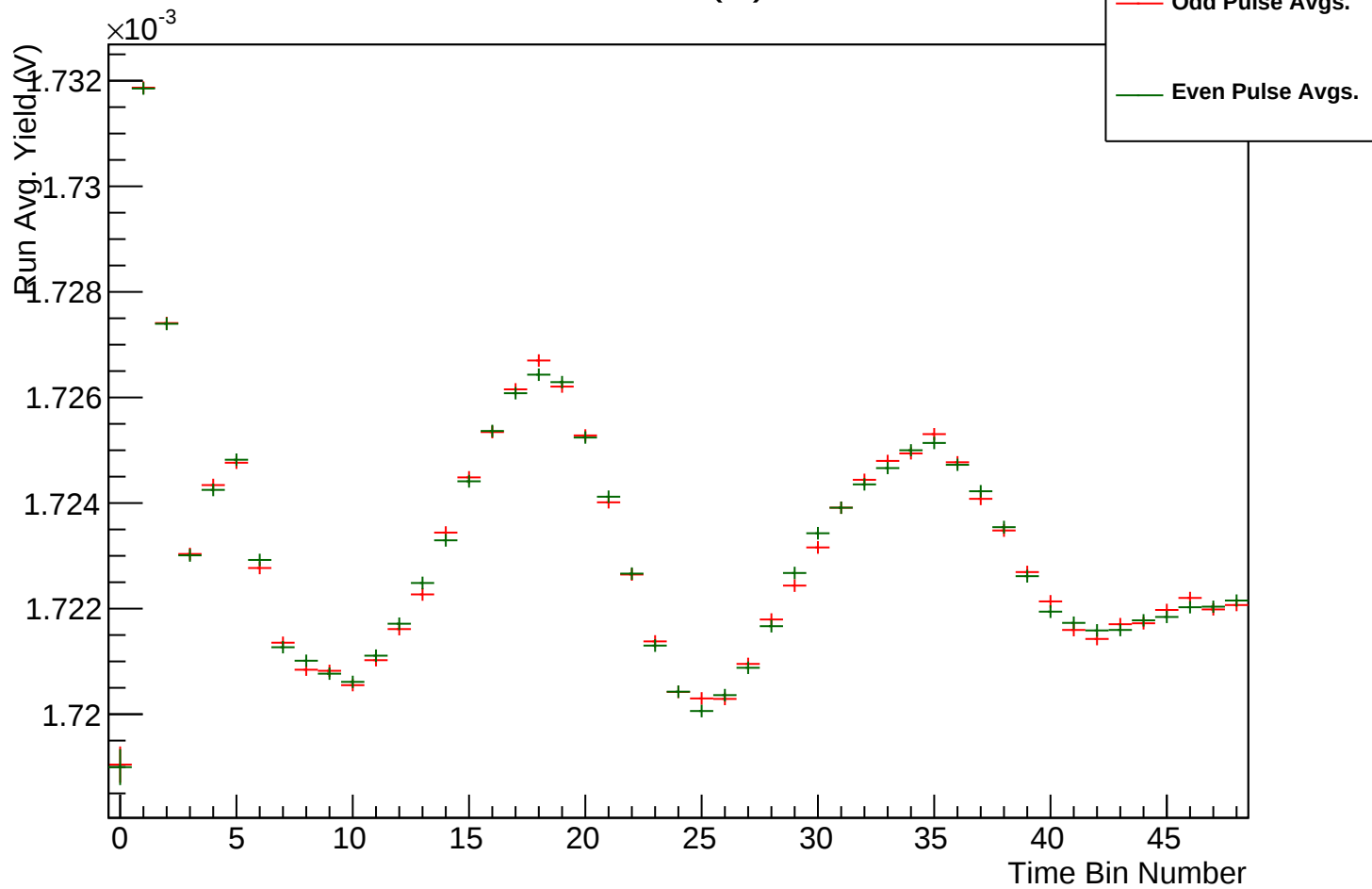
r17784-w89-Yield(V)-OddPulses



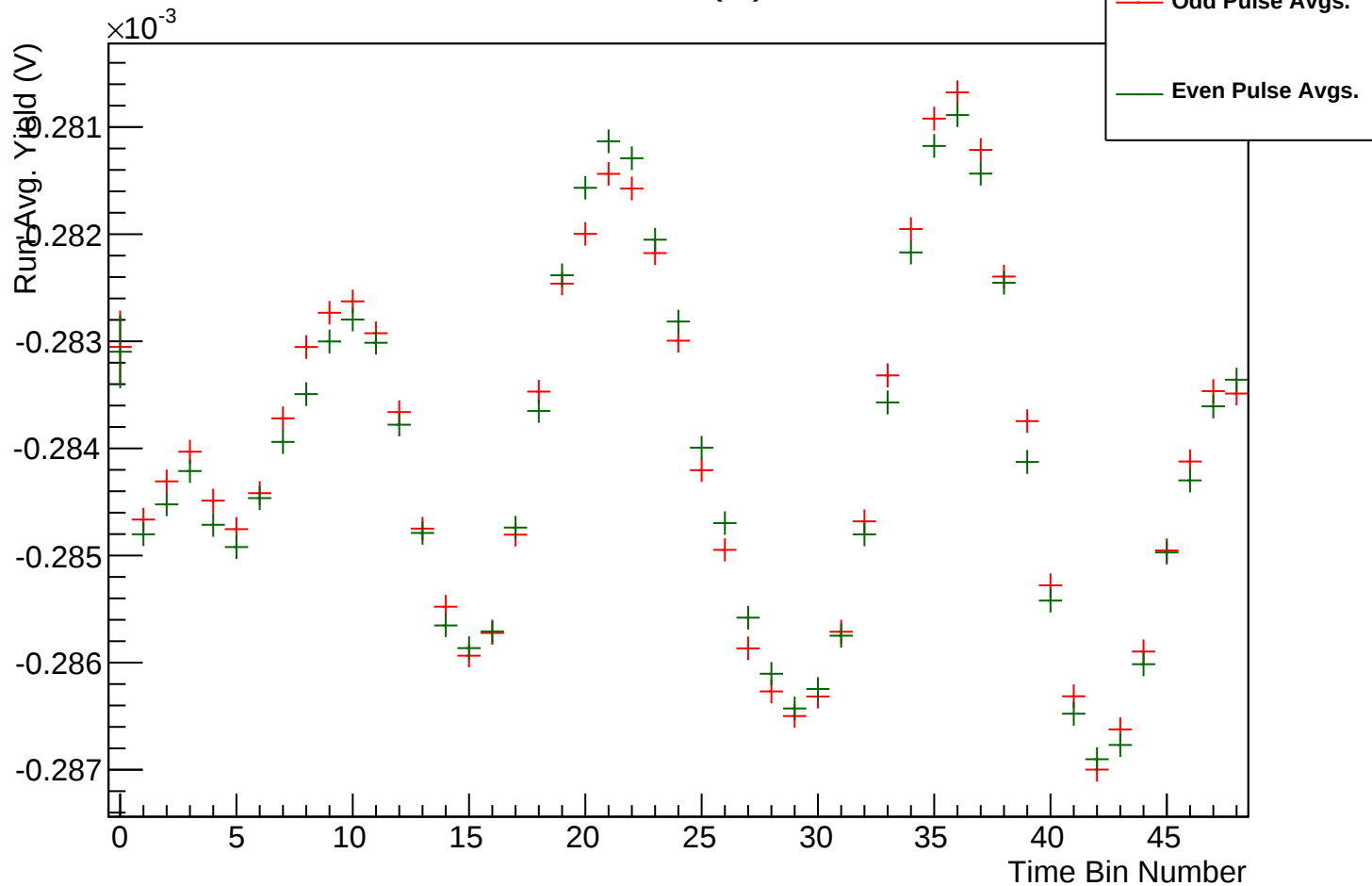
r17784-w90-Yield(V)-OddPulses



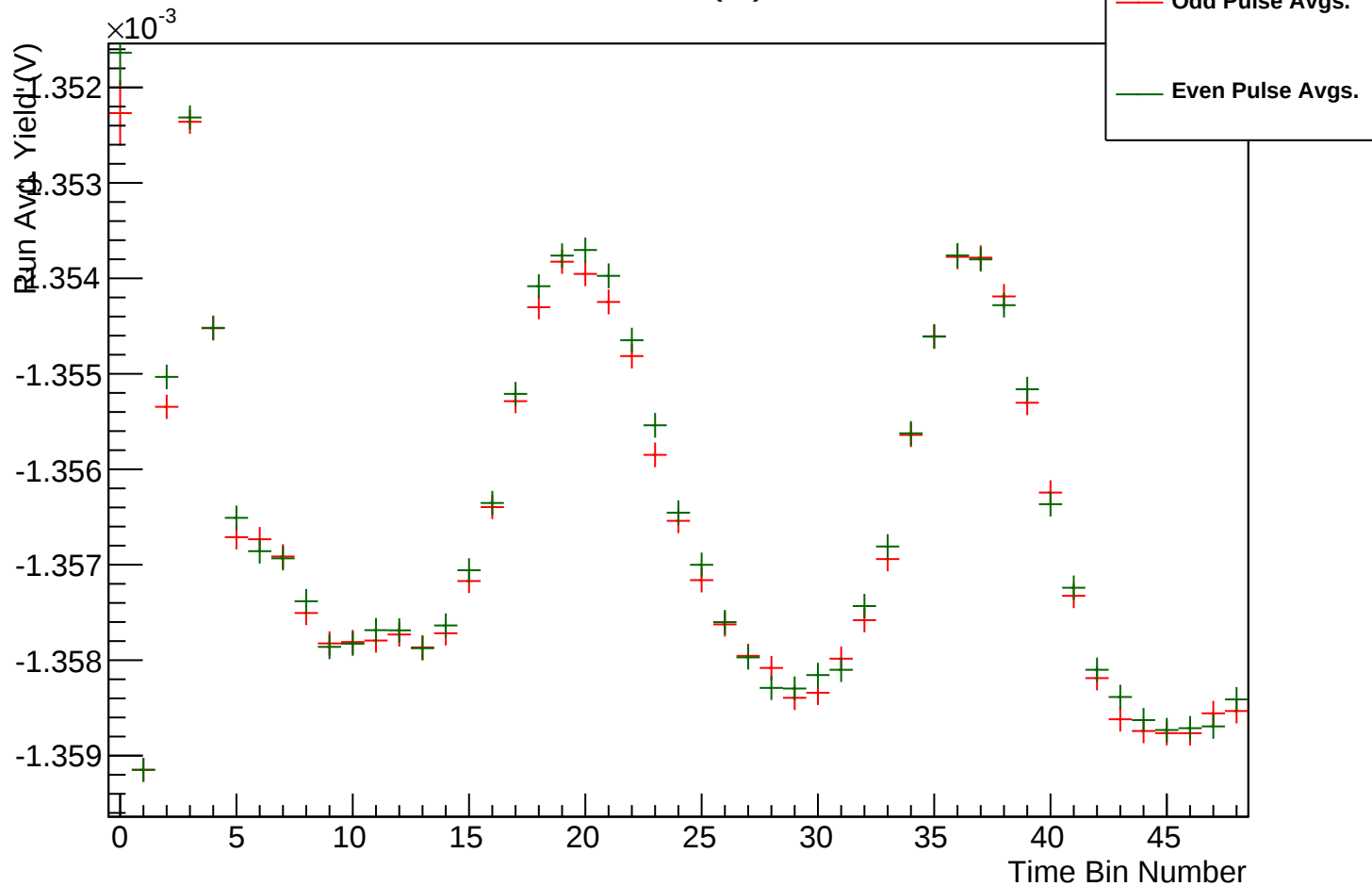
r17784-w91-Yield(V)-OddPulses



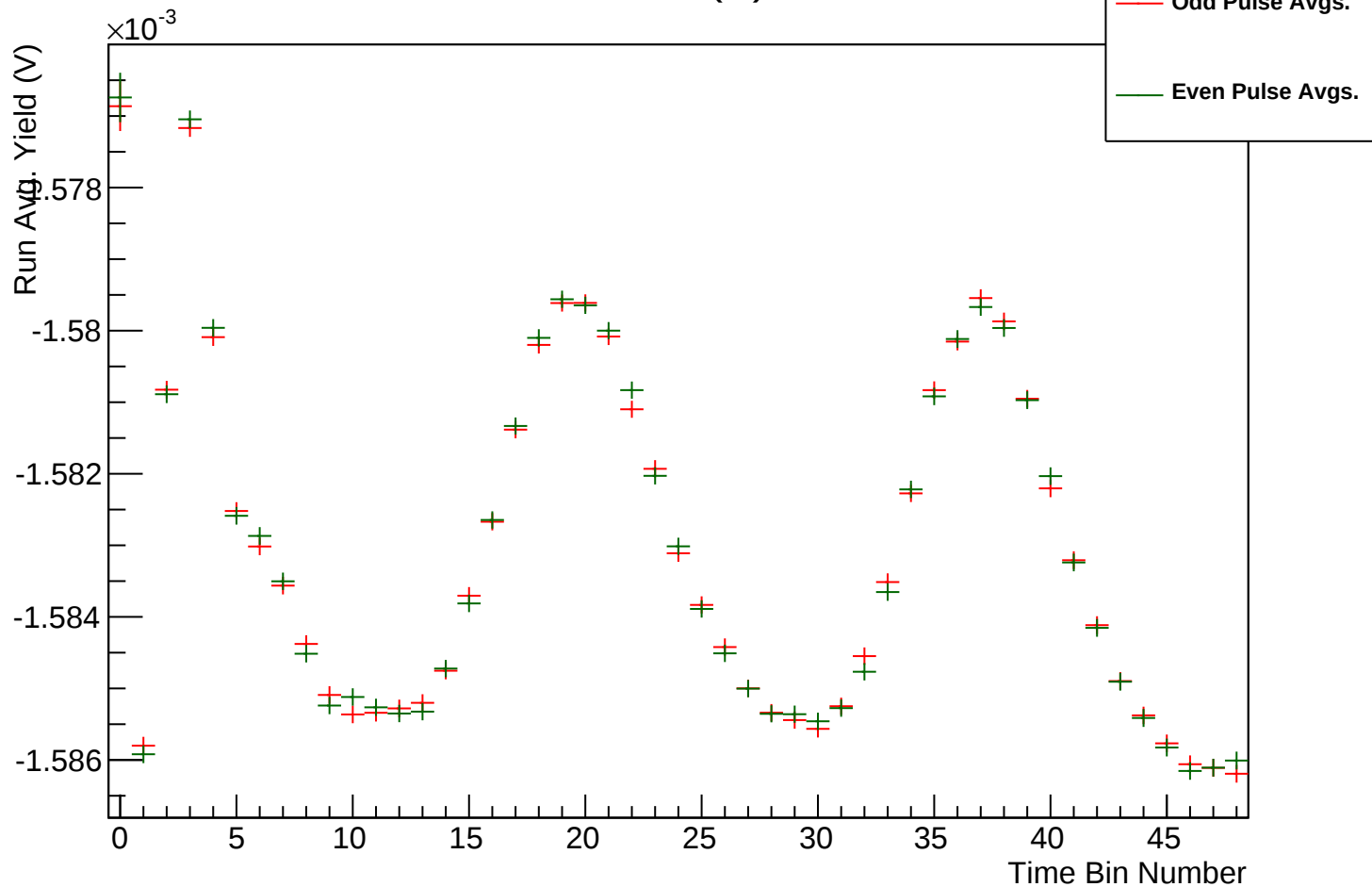
r17784-w92-Yield(V)-OddPulses



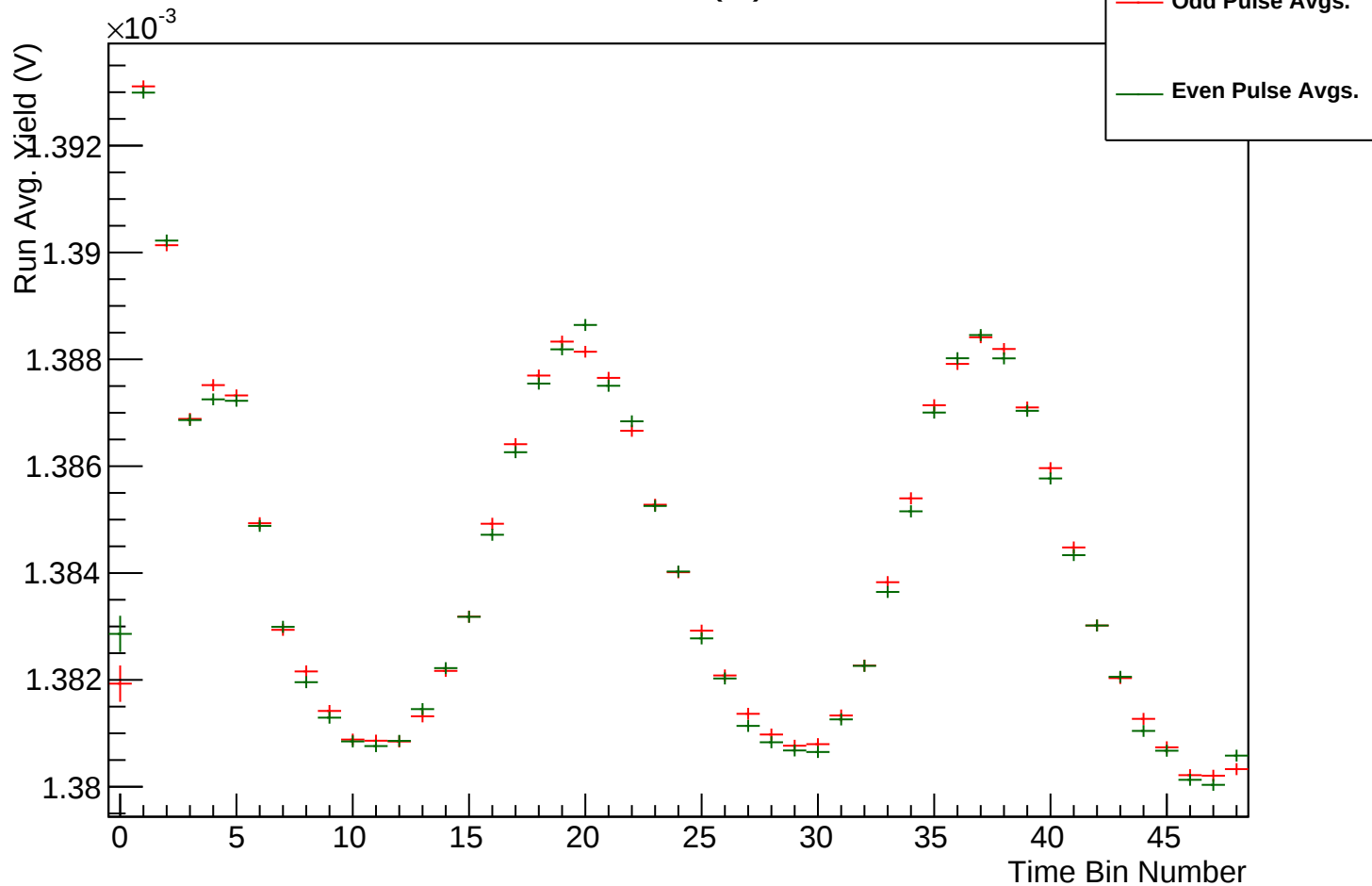
r17784-w93-Yield(V)-OddPulses



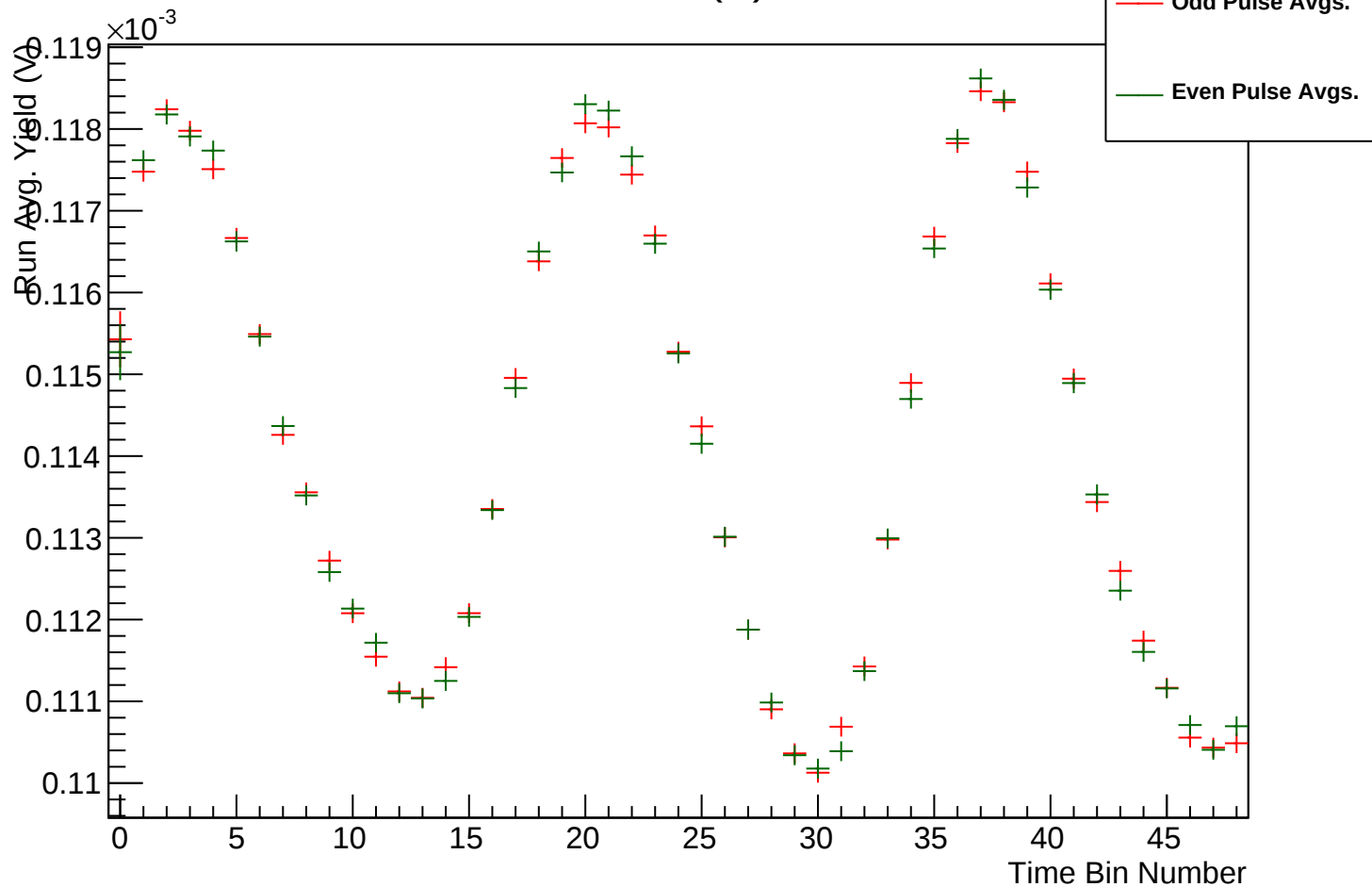
r17784-w94-Yield(V)-OddPulses



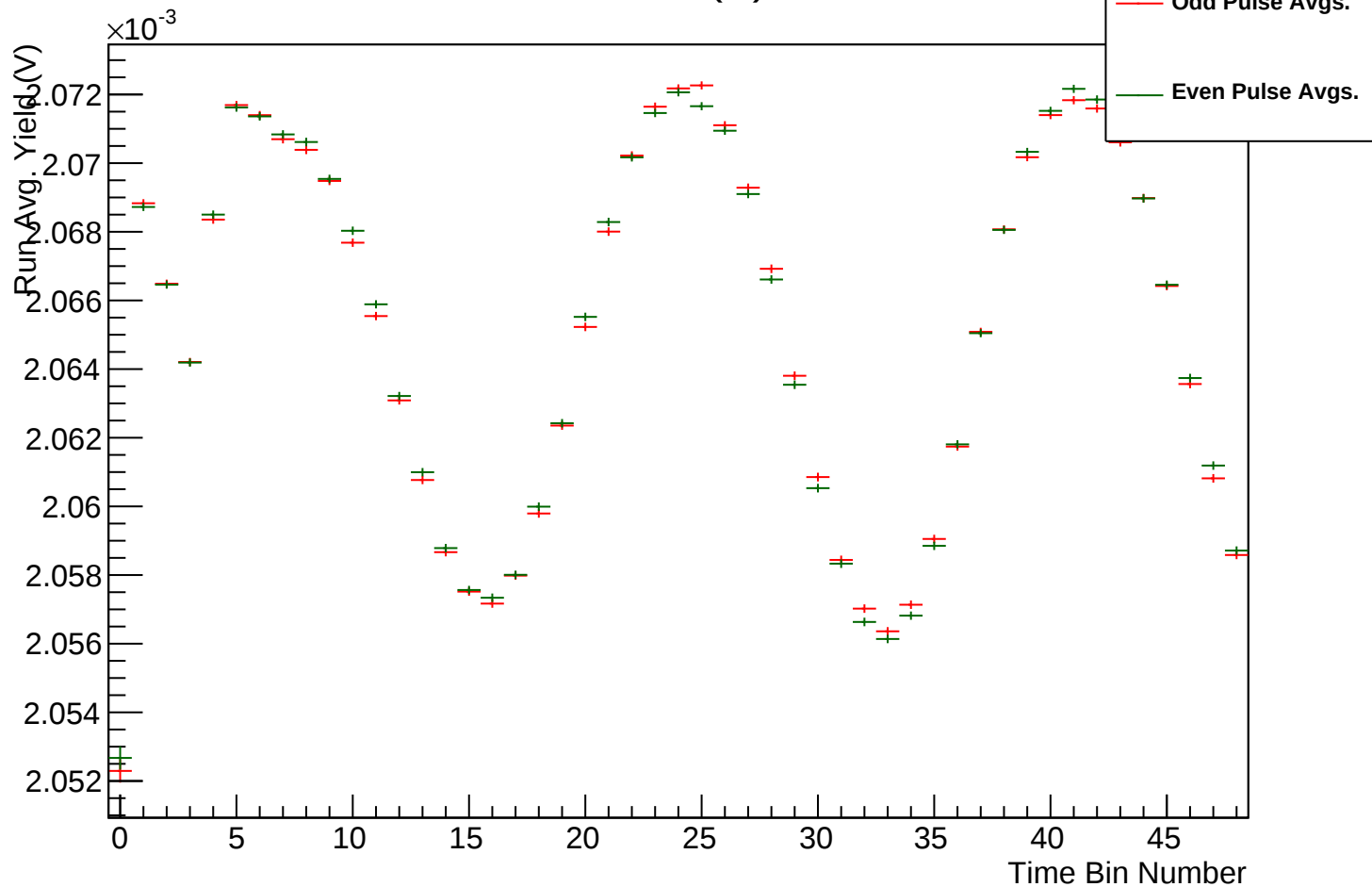
r17784-w95-Yield(V)-OddPulses



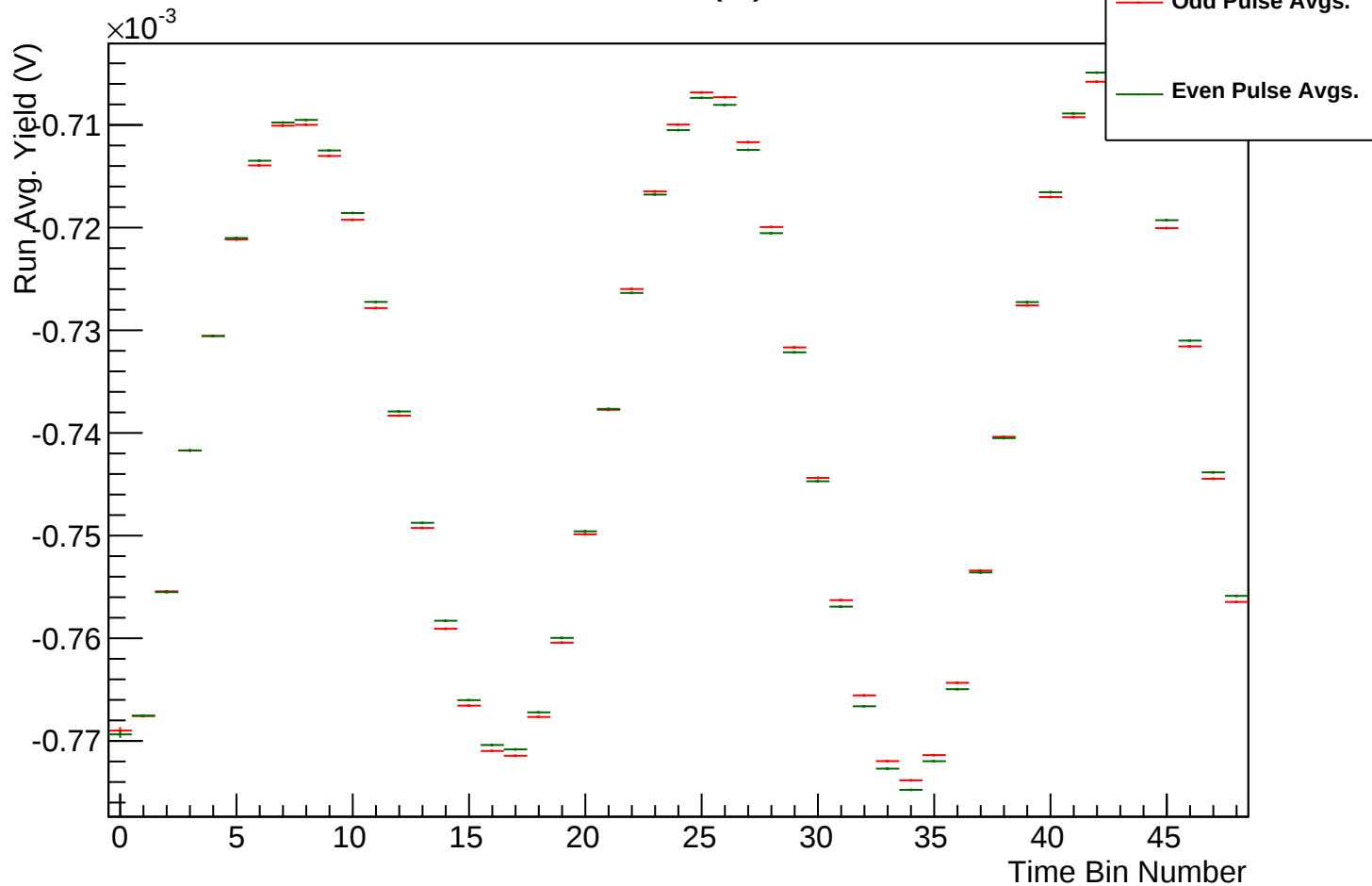
r17784-w96-Yield(V)-OddPulses



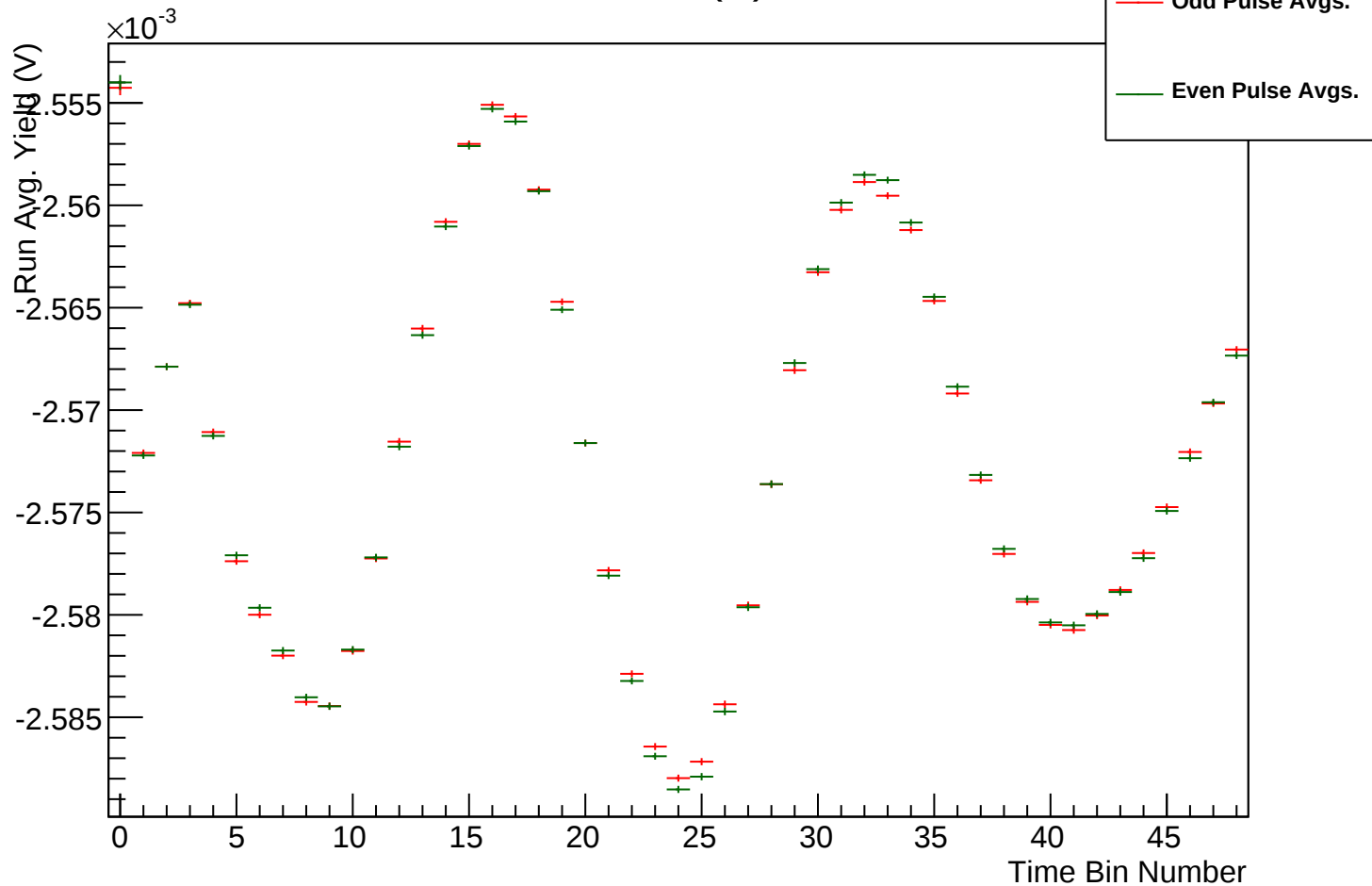
r17784-w97-Yield(V)-OddPulses



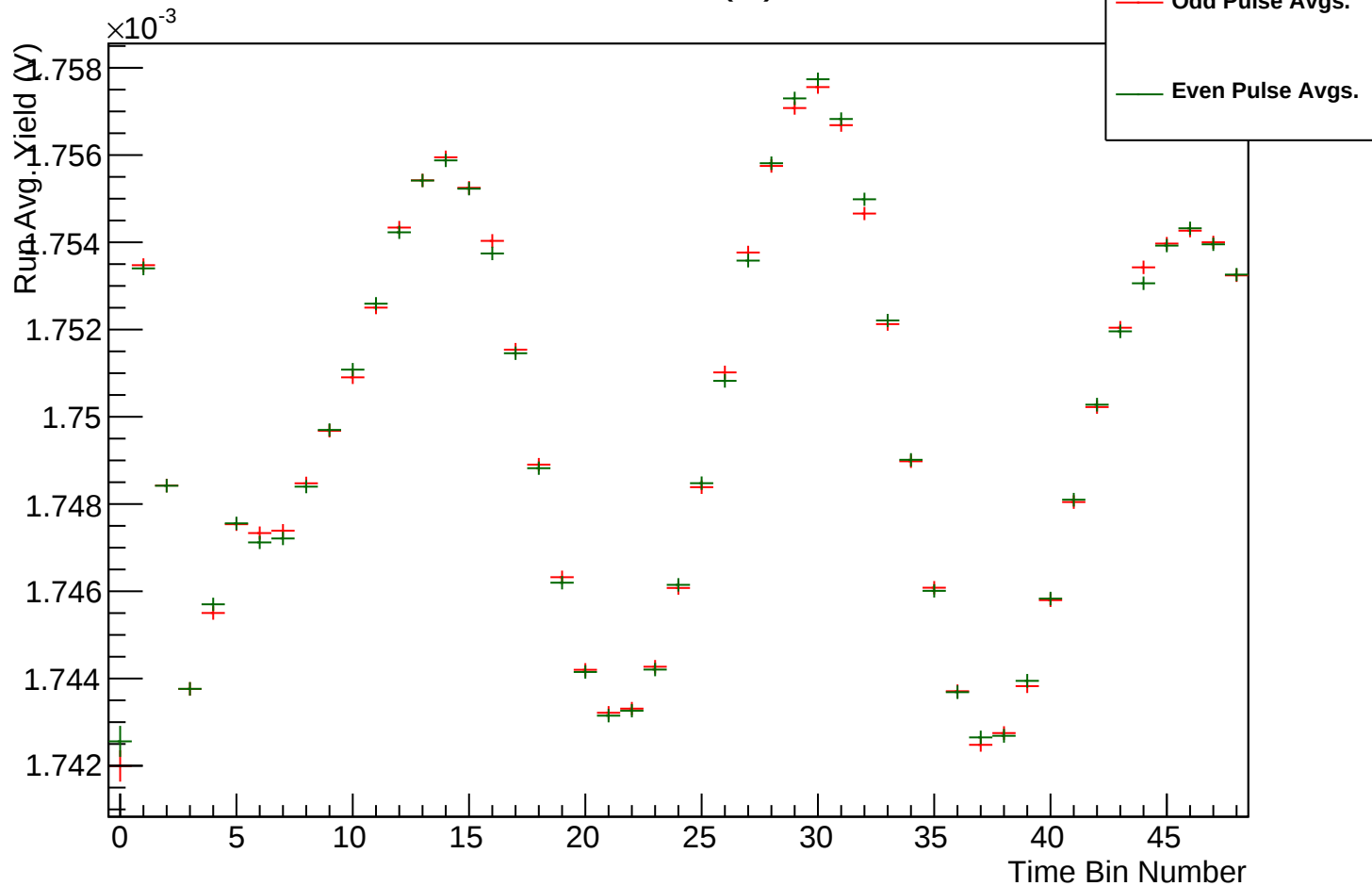
r17784-w98-Yield(V)-OddPulses



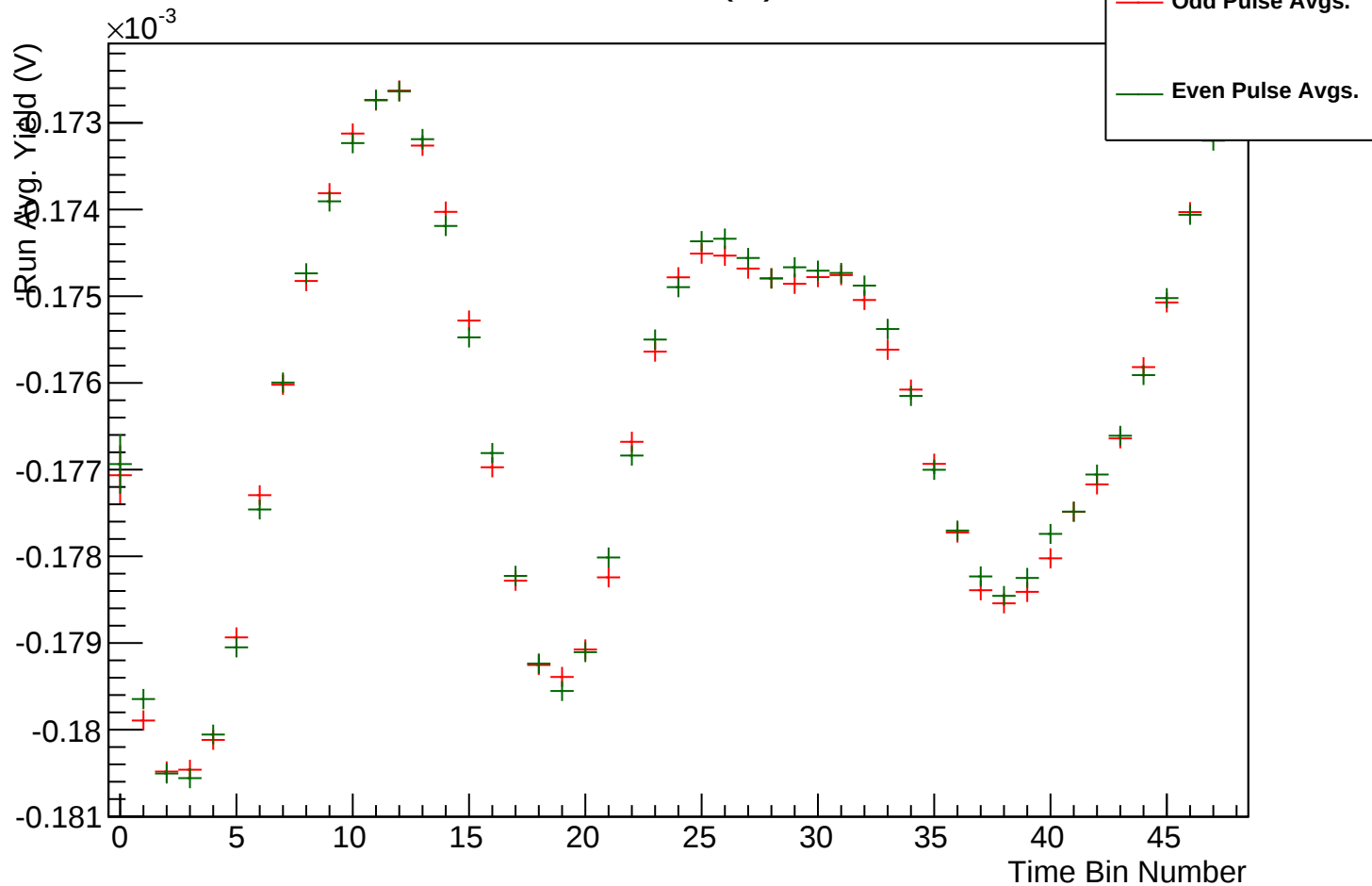
r17784-w99-Yield(V)-OddPulses



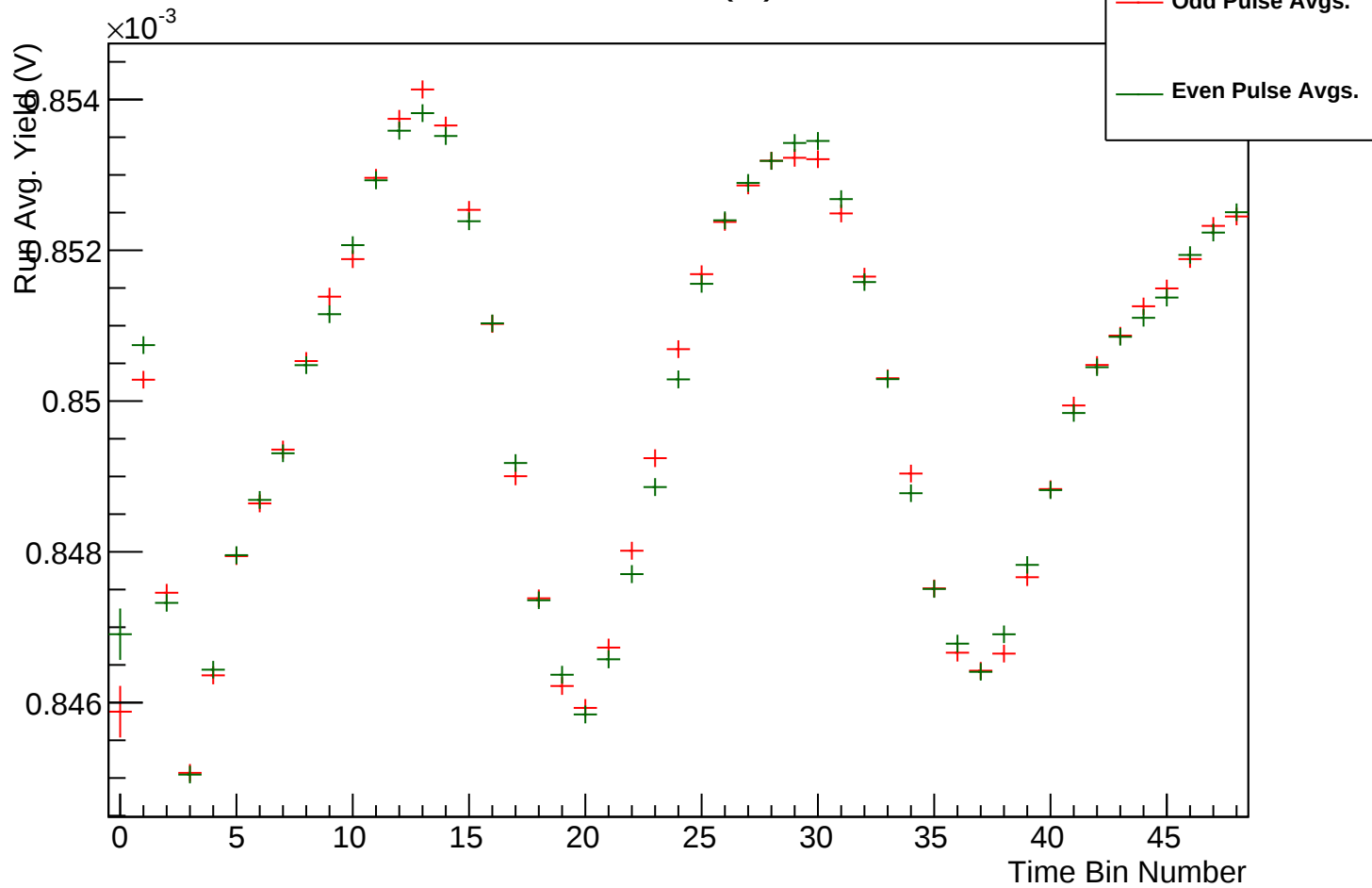
r17784-w100-Yield(V)-OddPulses



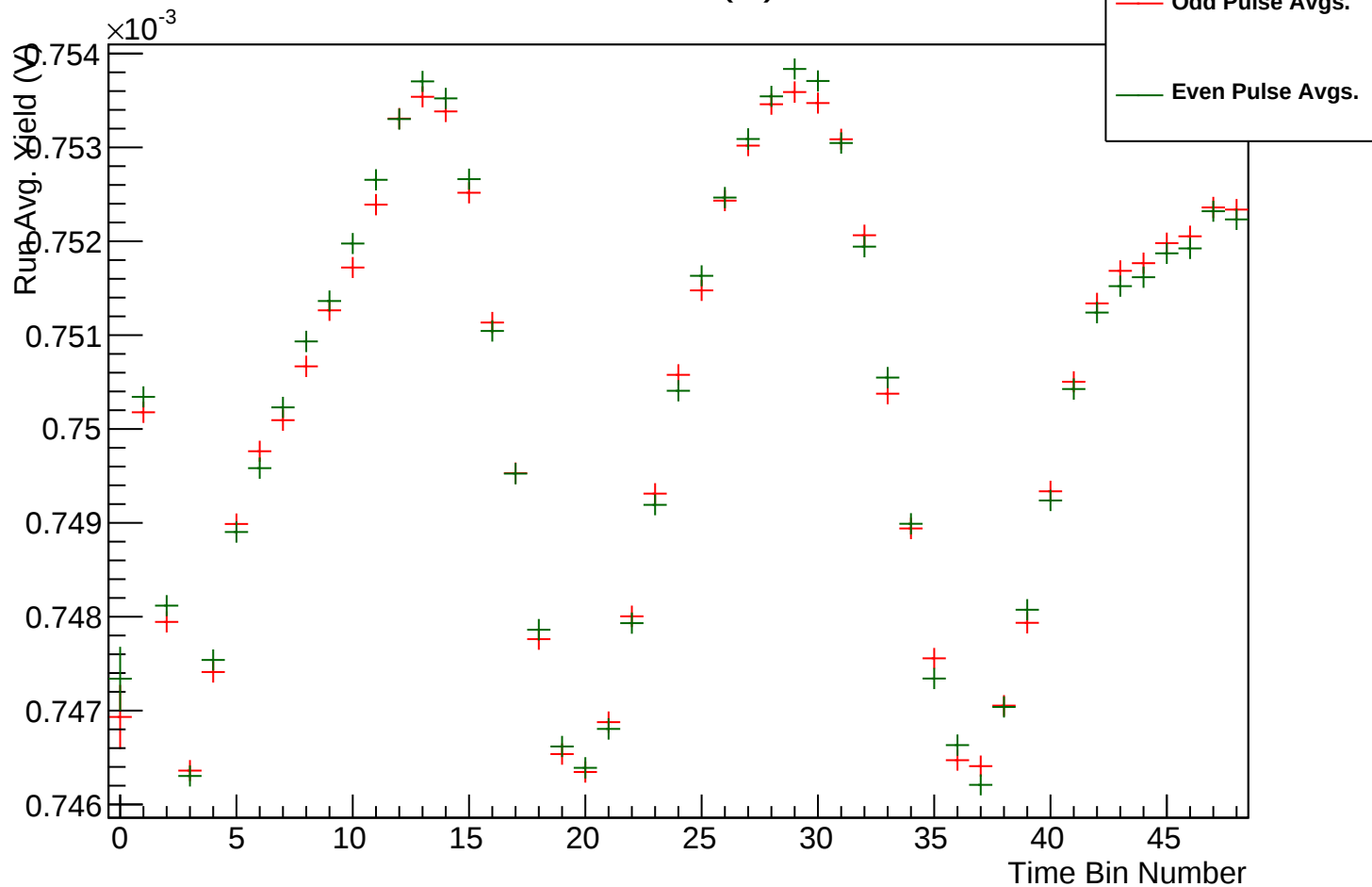
r17784-w101-Yield(V)-OddPulses



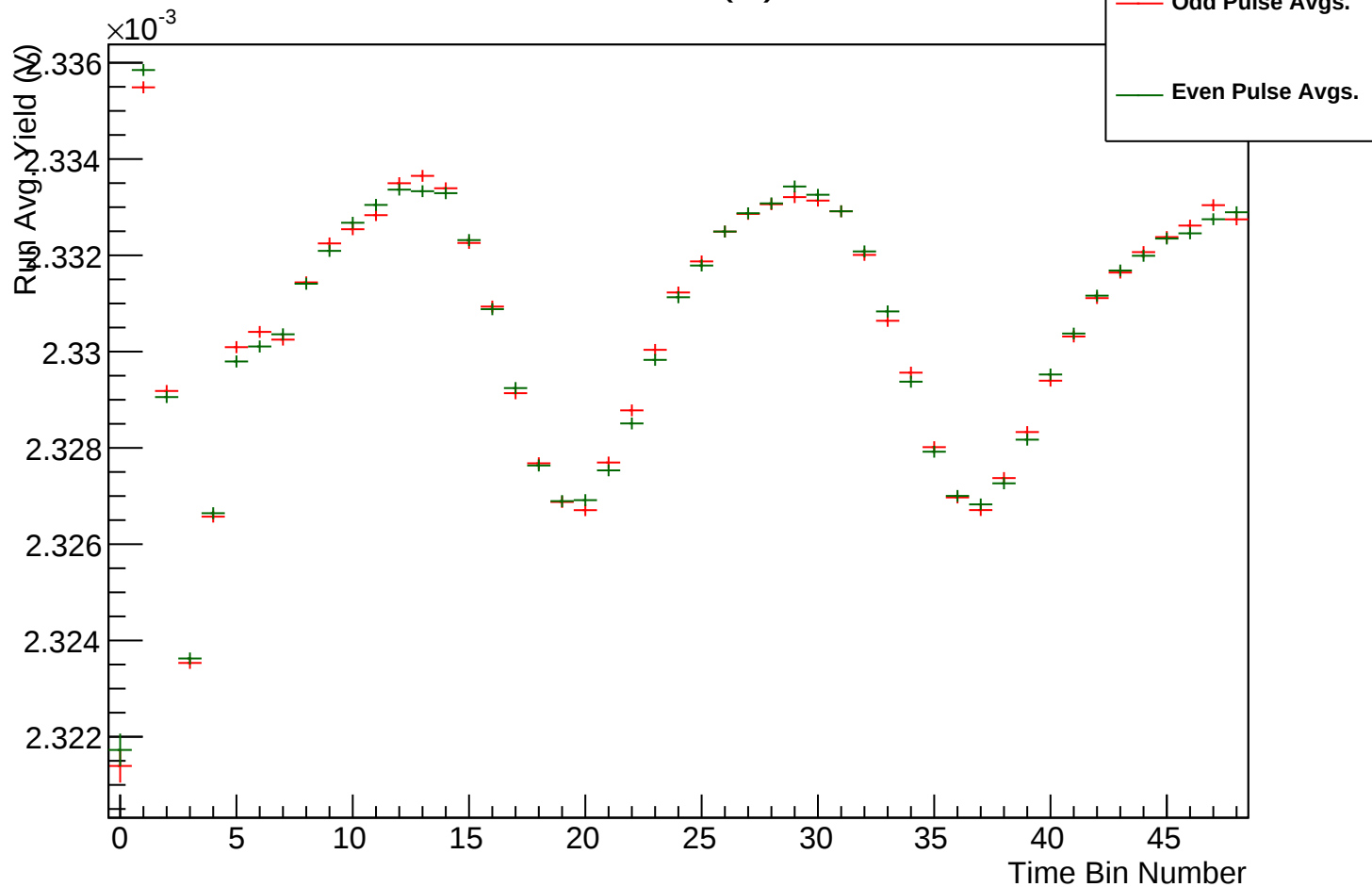
r17784-w102-Yield(V)-OddPulses



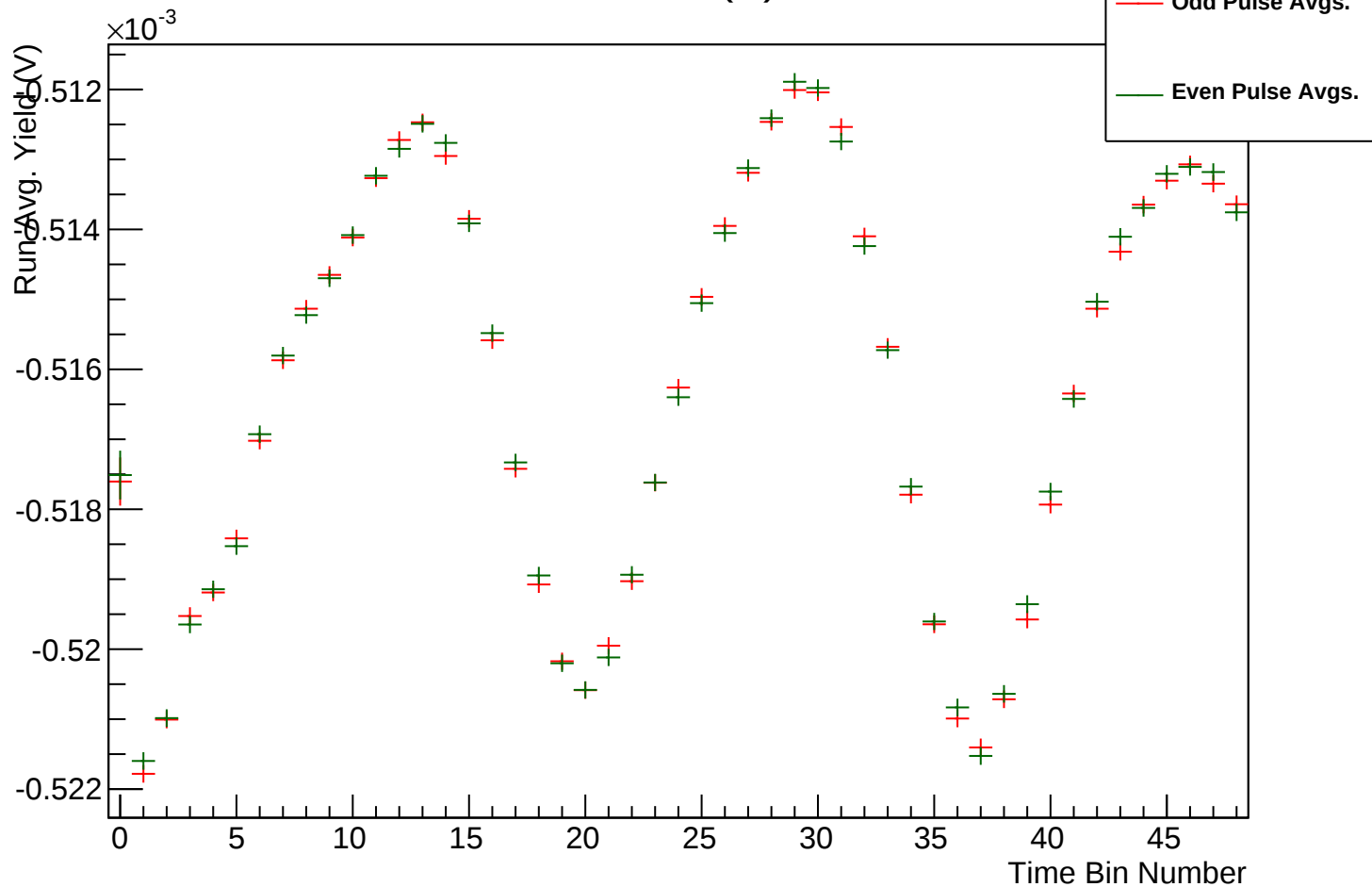
r17784-w103-Yield(V)-OddPulses



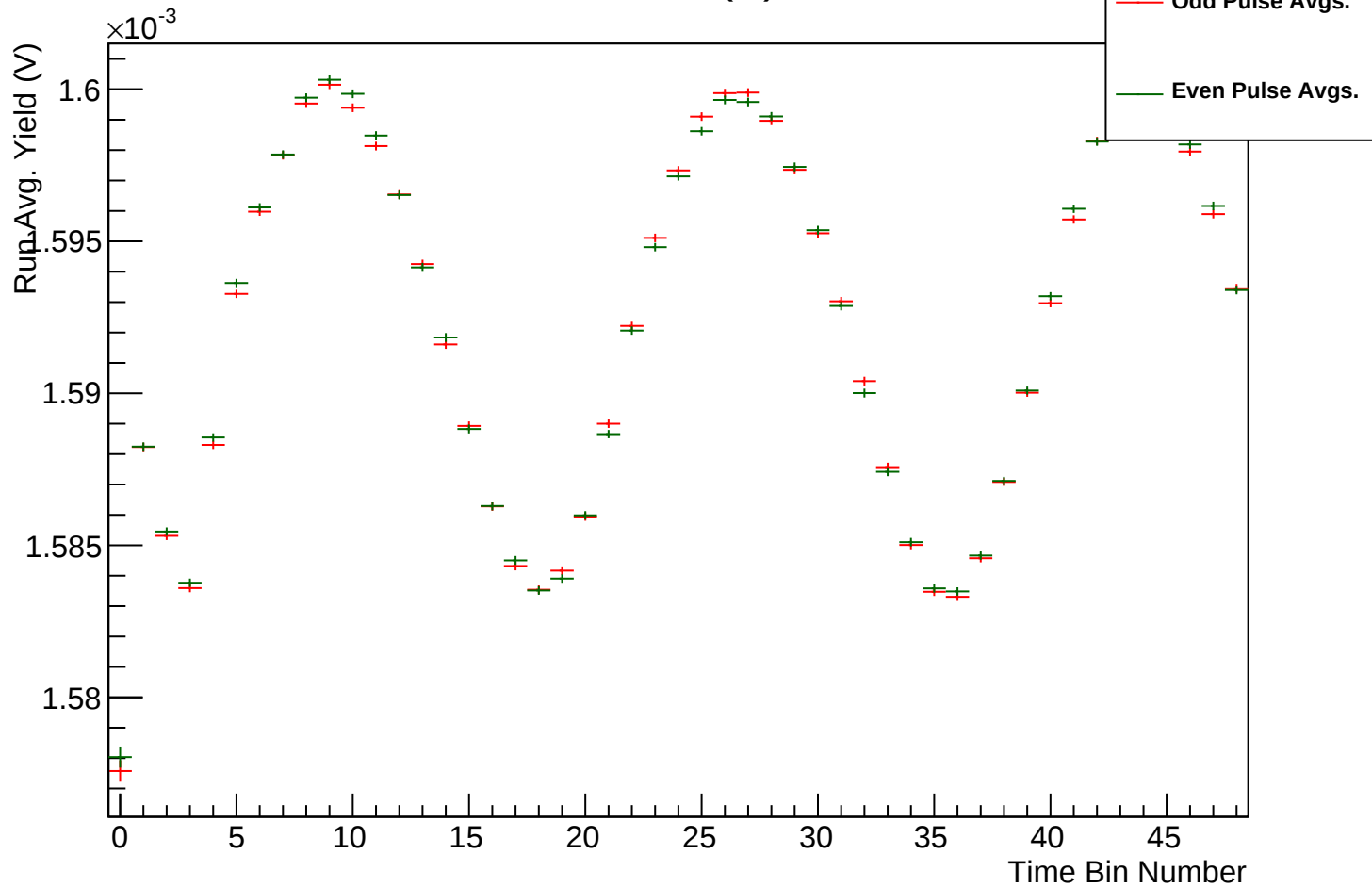
r17784-w104-Yield(V)-OddPulses



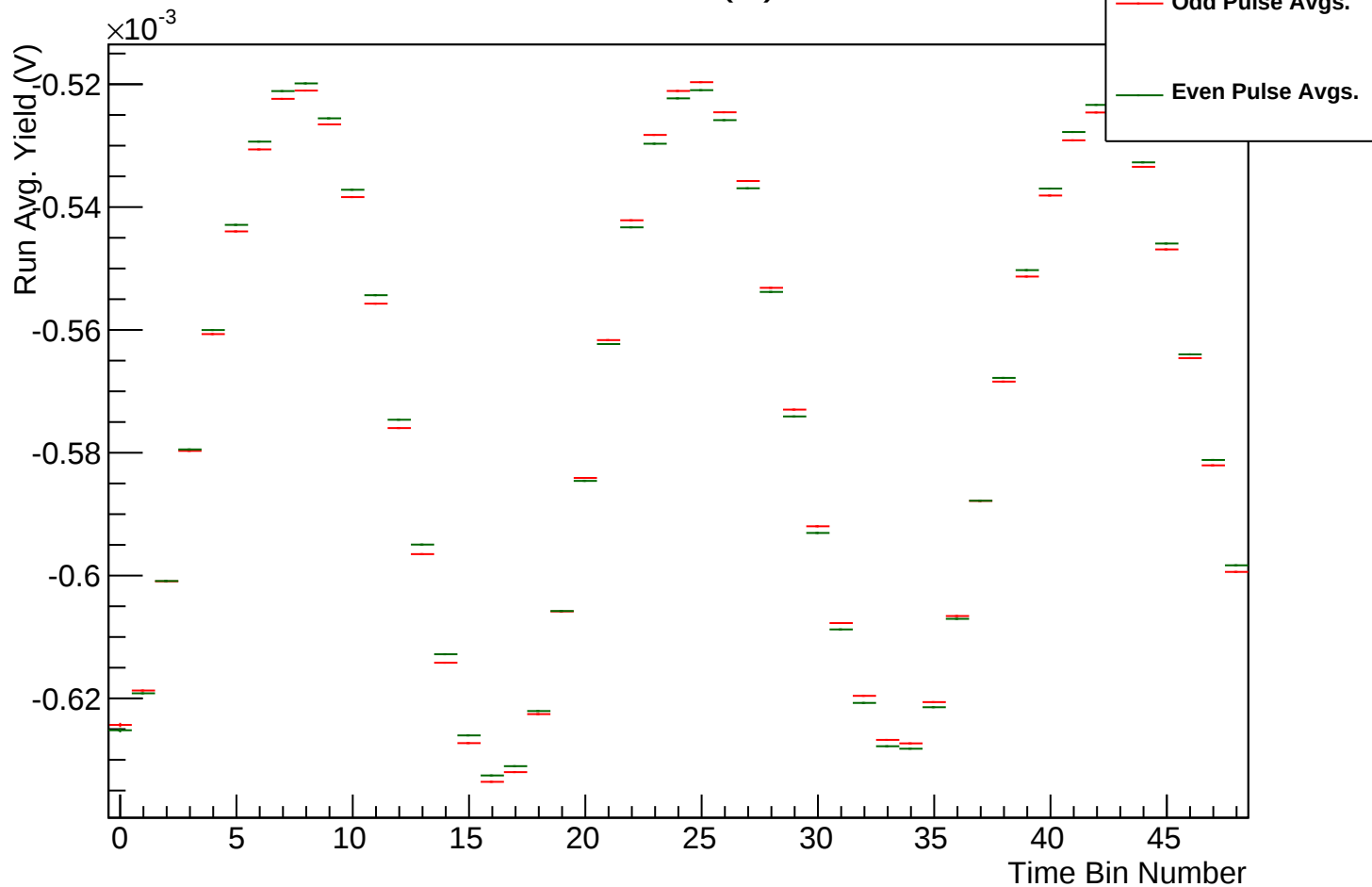
r17784-w105-Yield(V)-OddPulses



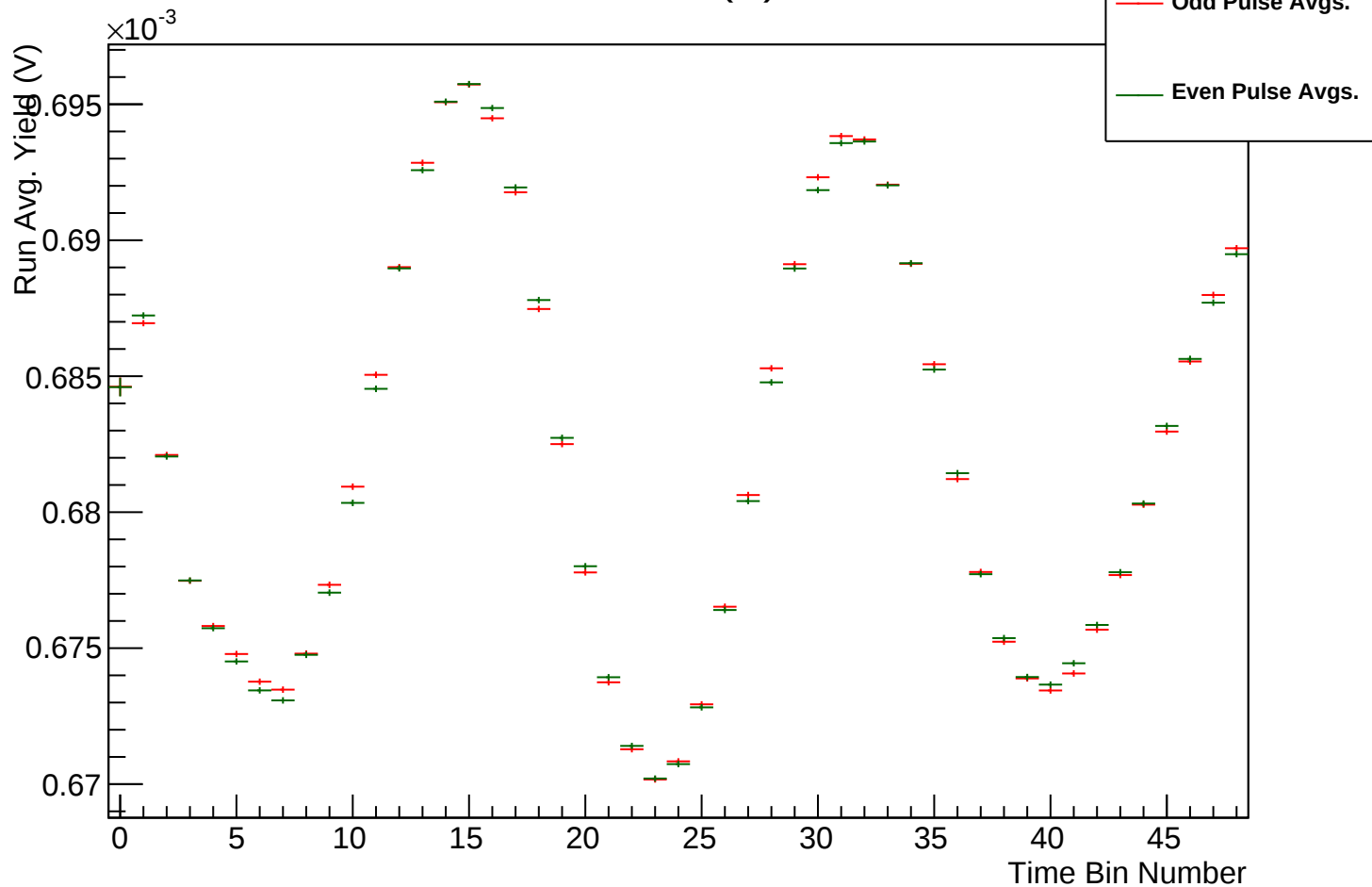
r17784-w106-Yield(V)-OddPulses



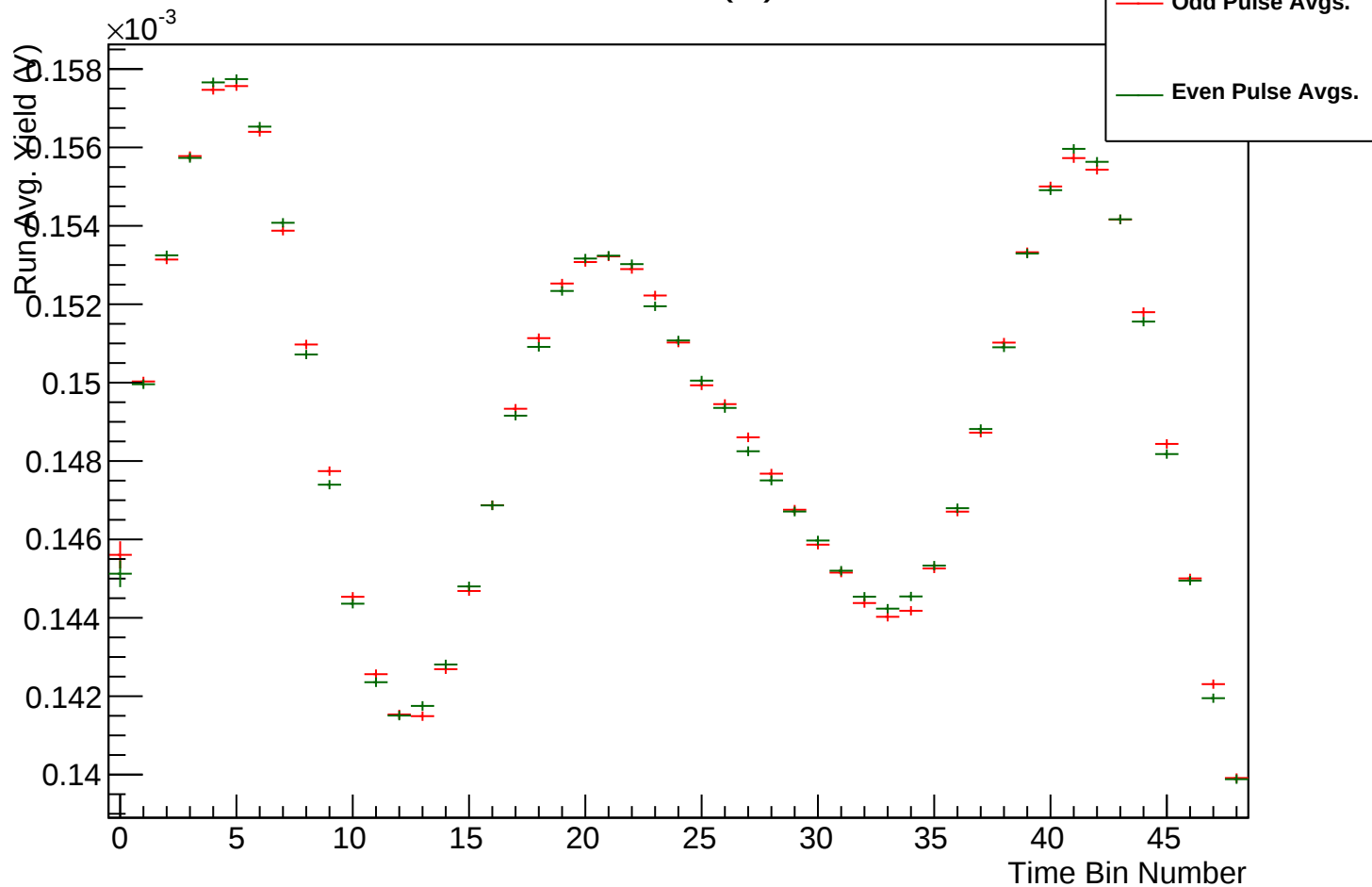
r17784-w107-Yield(V)-OddPulses



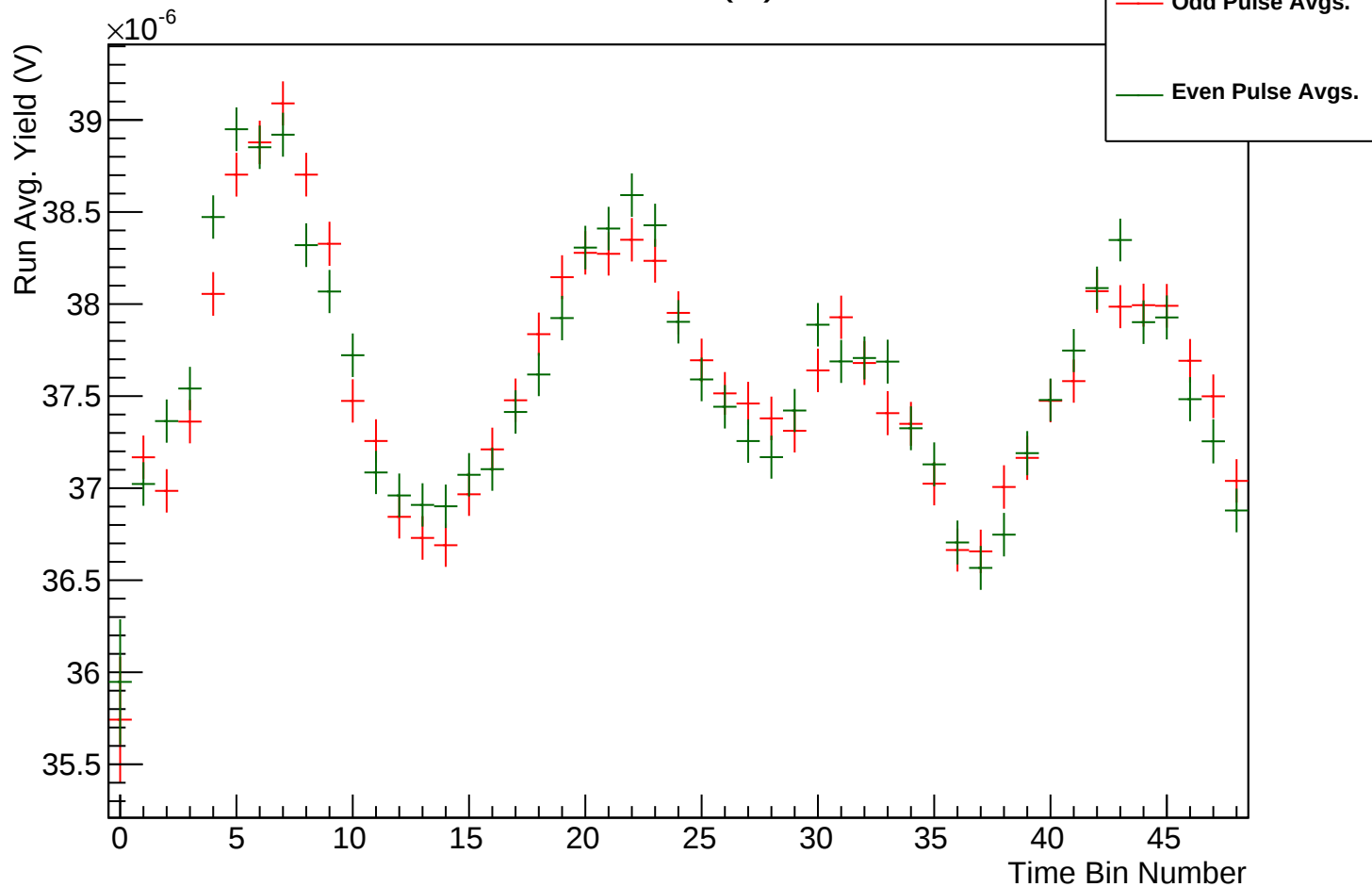
r17784-w108-Yield(V)-OddPulses



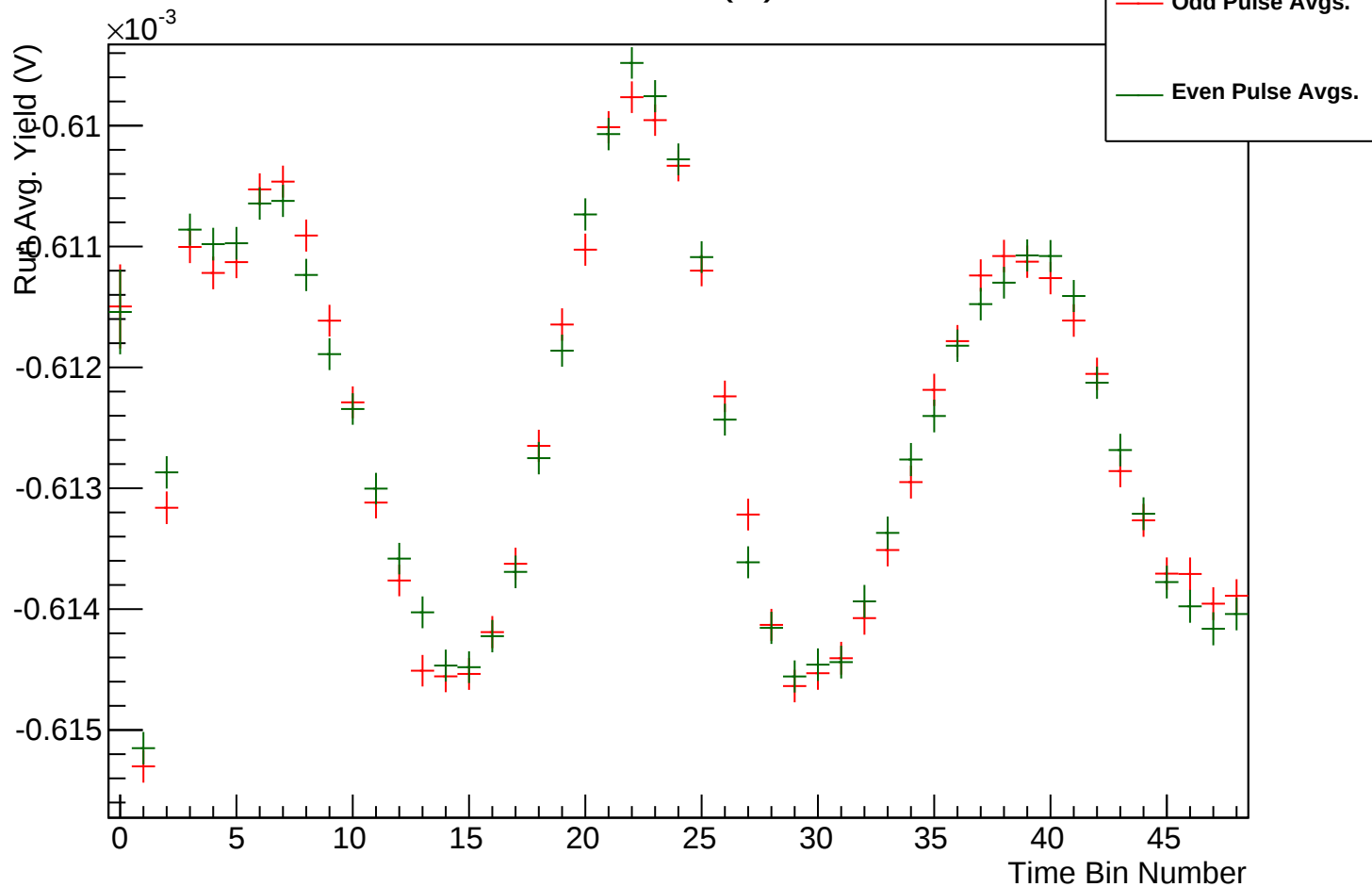
r17784-w109-Yield(V)-OddPulses



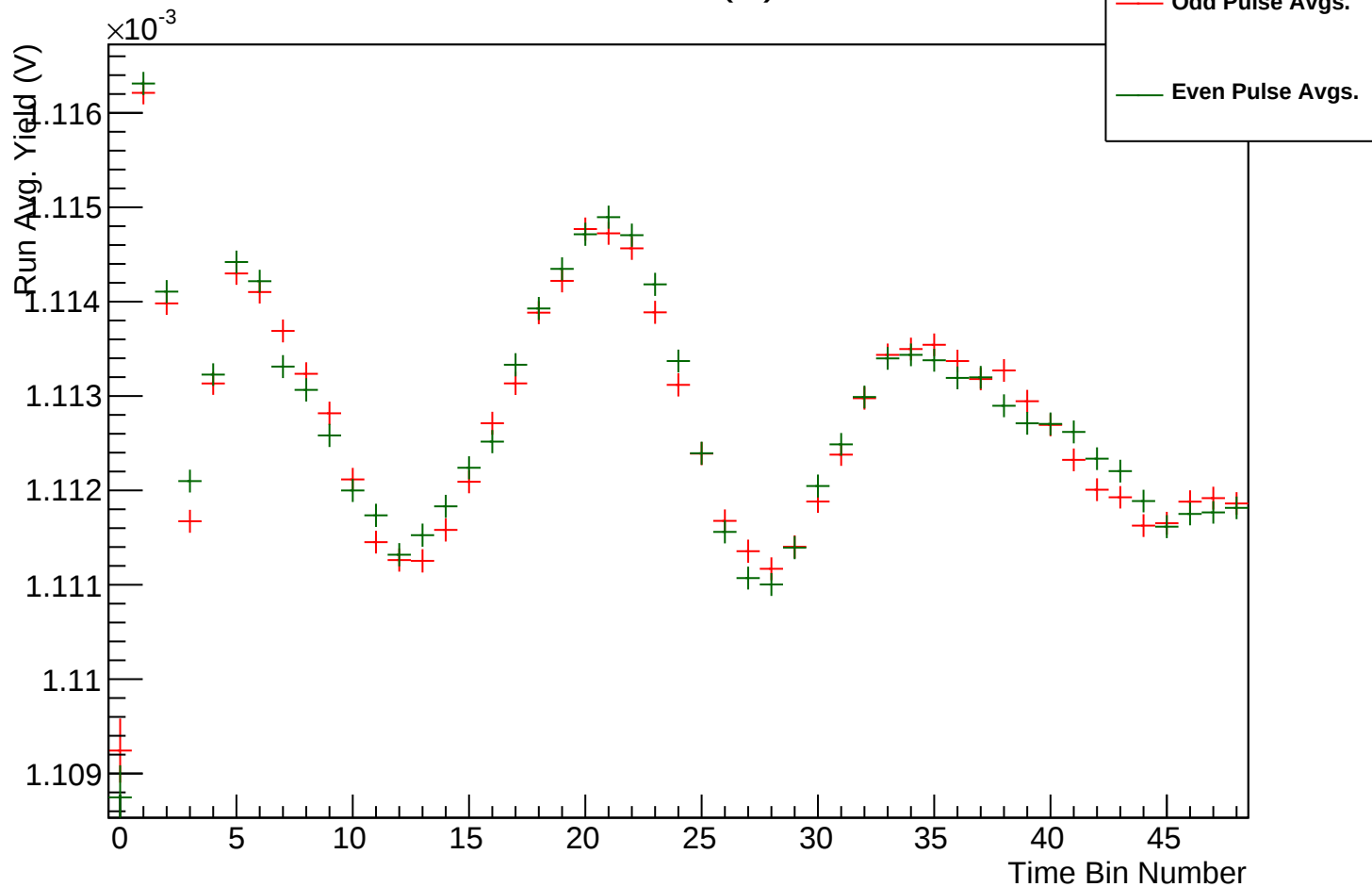
r17784-w110-Yield(V)-OddPulses



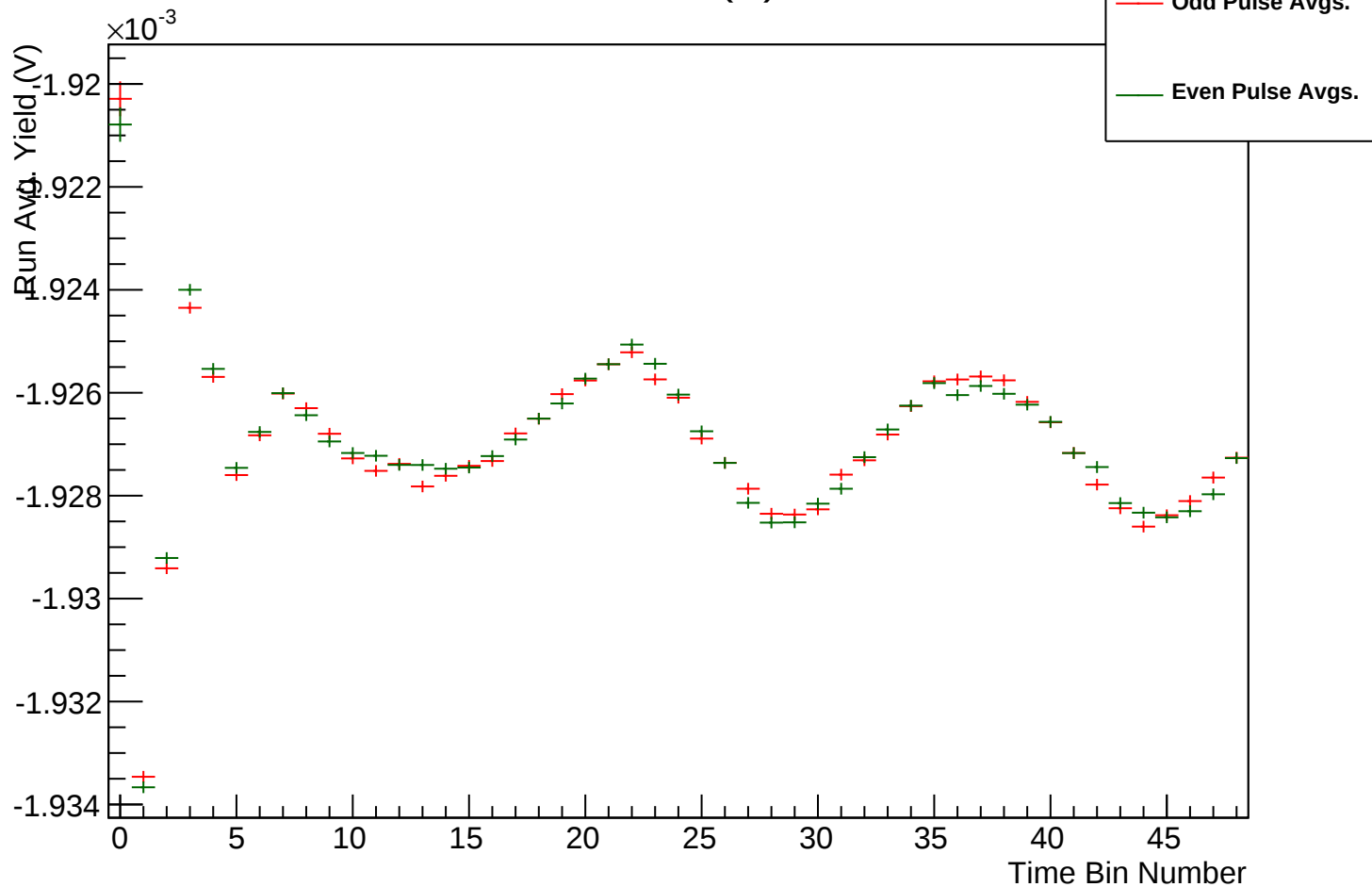
r17784-w111-Yield(V)-OddPulses



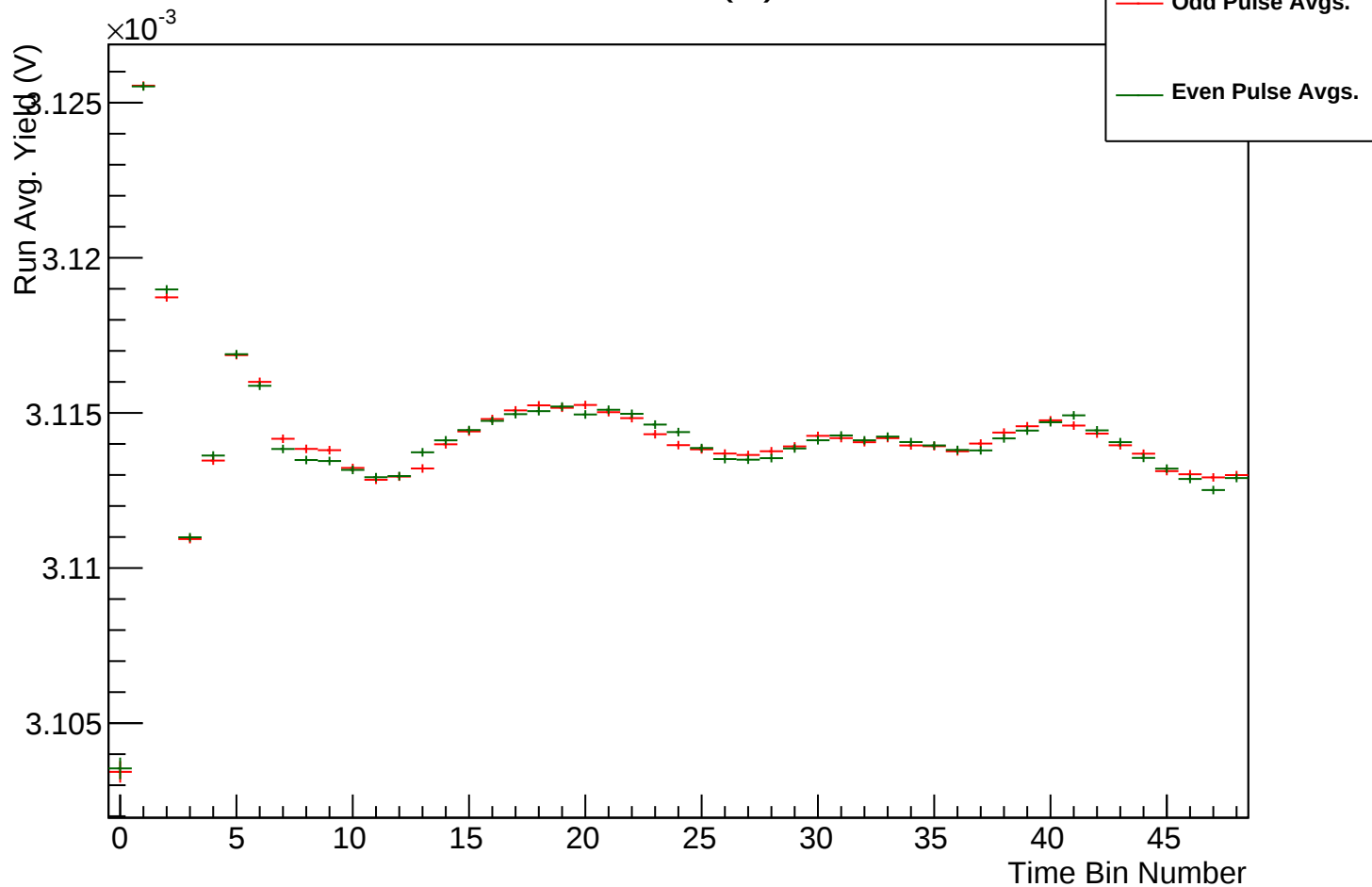
r17784-w112-Yield(V)-OddPulses



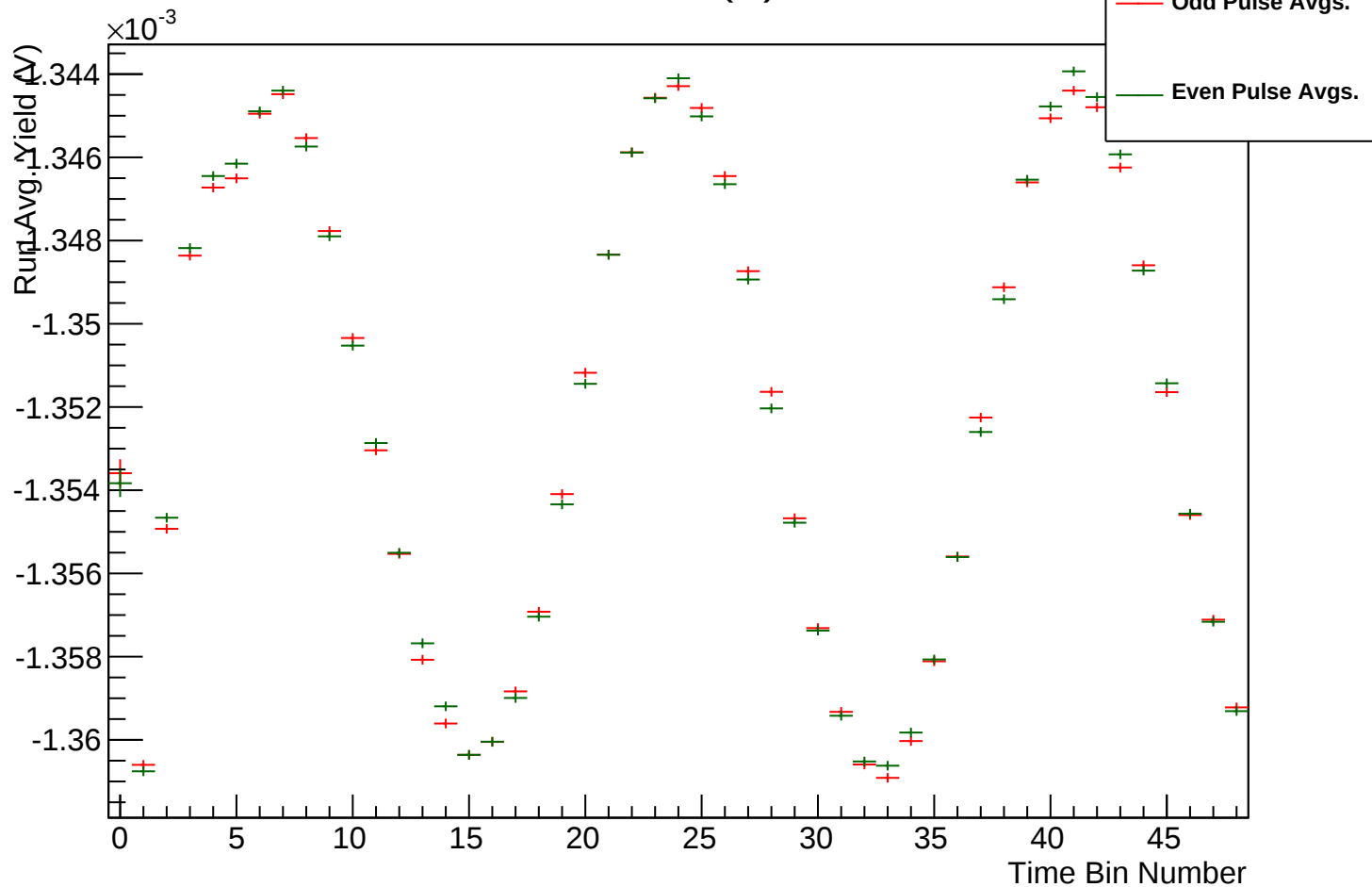
r17784-w113-Yield(V)-OddPulses



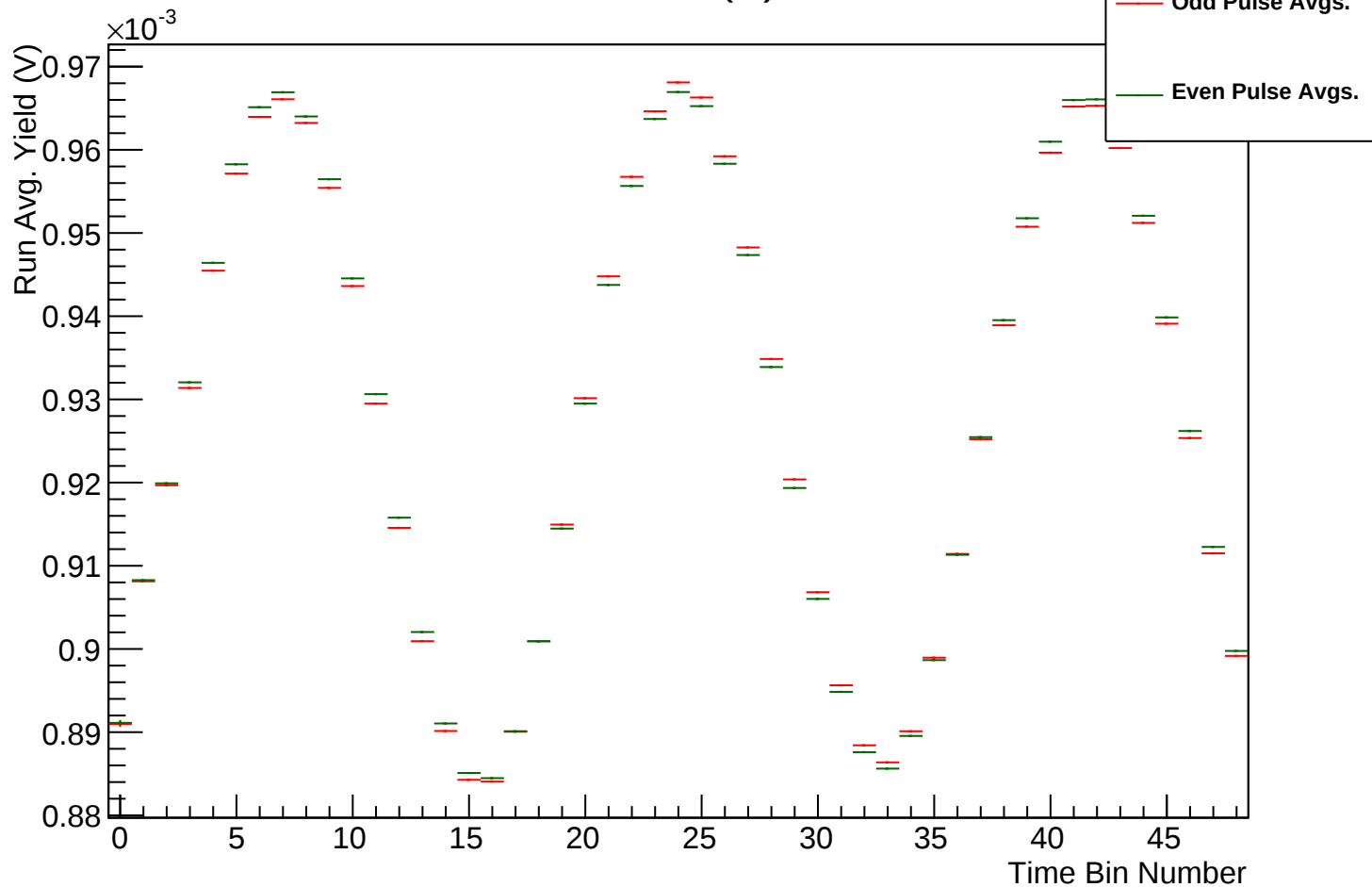
r17784-w114-Yield(V)-OddPulses



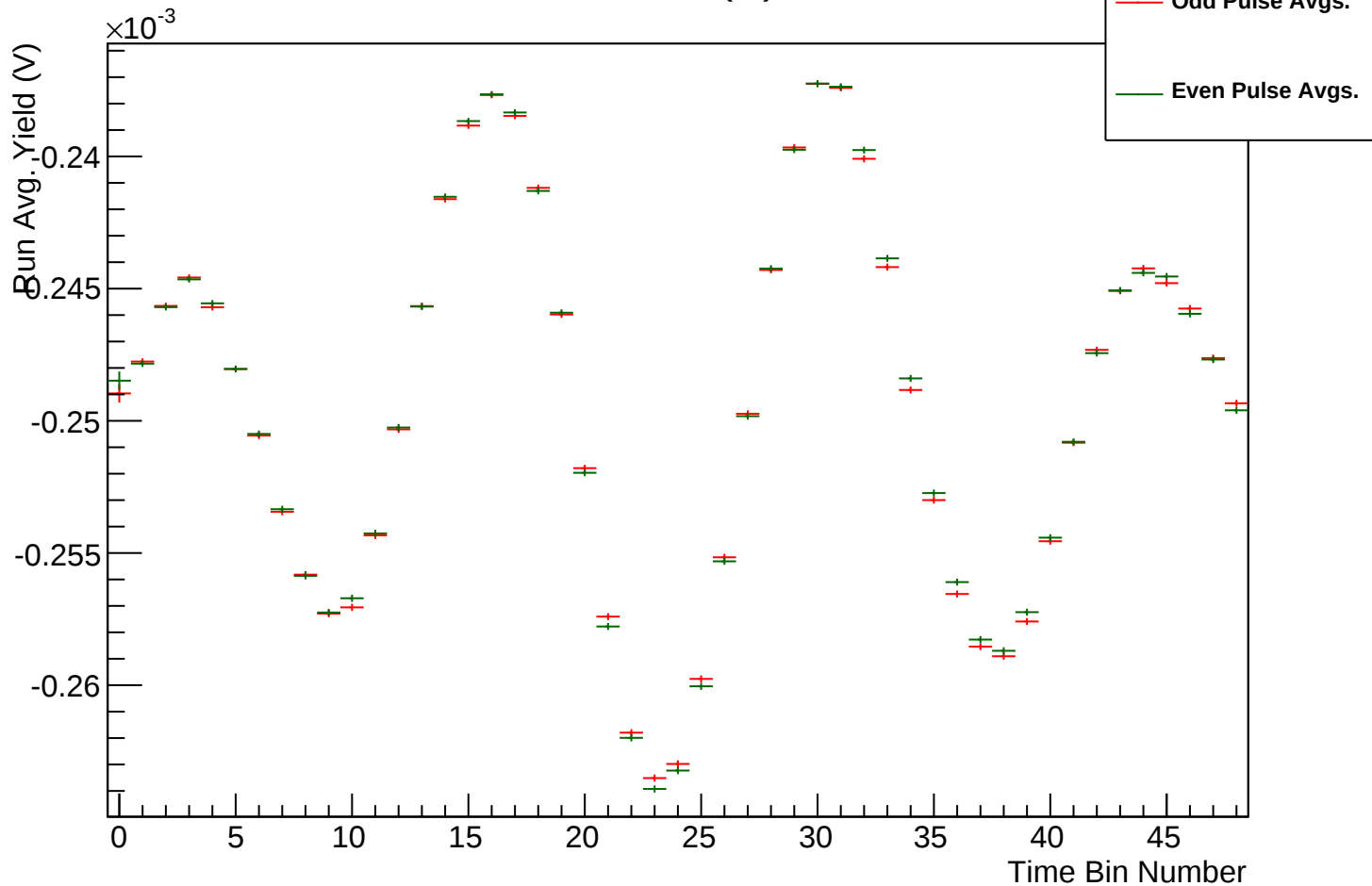
r17784-w115-Yield(V)-OddPulses



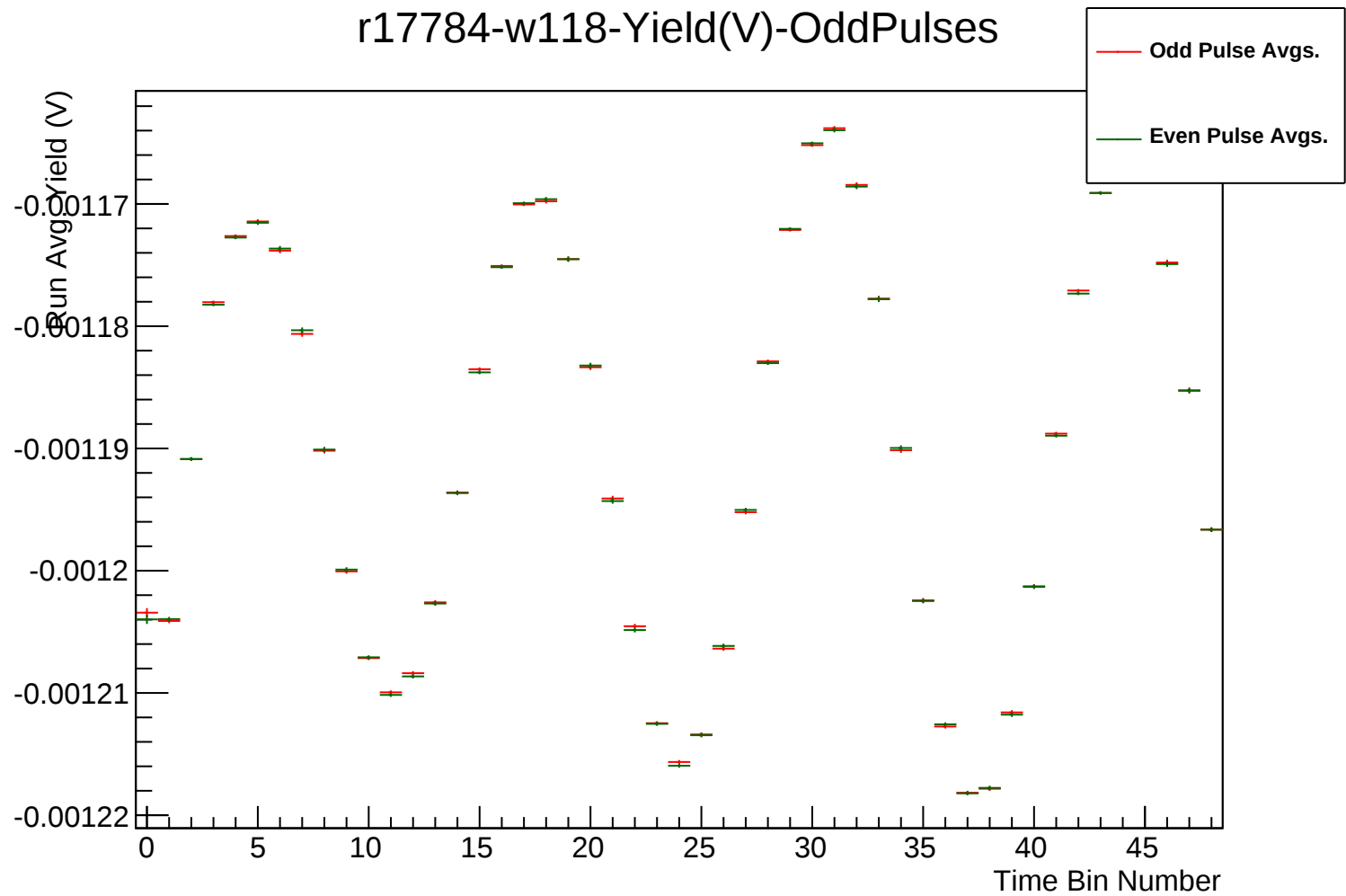
r17784-w116-Yield(V)-OddPulses



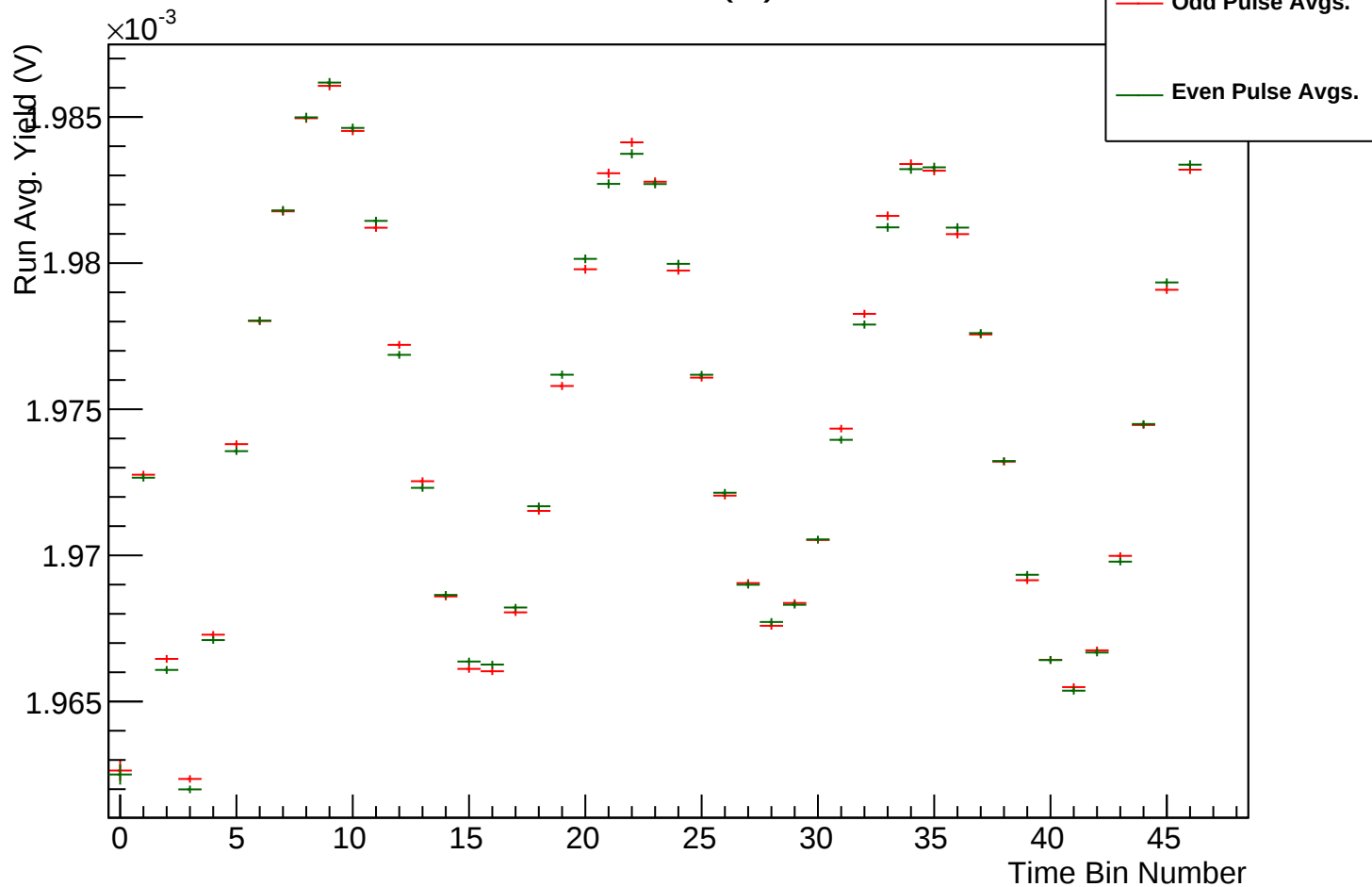
r17784-w117-Yield(V)-OddPulses



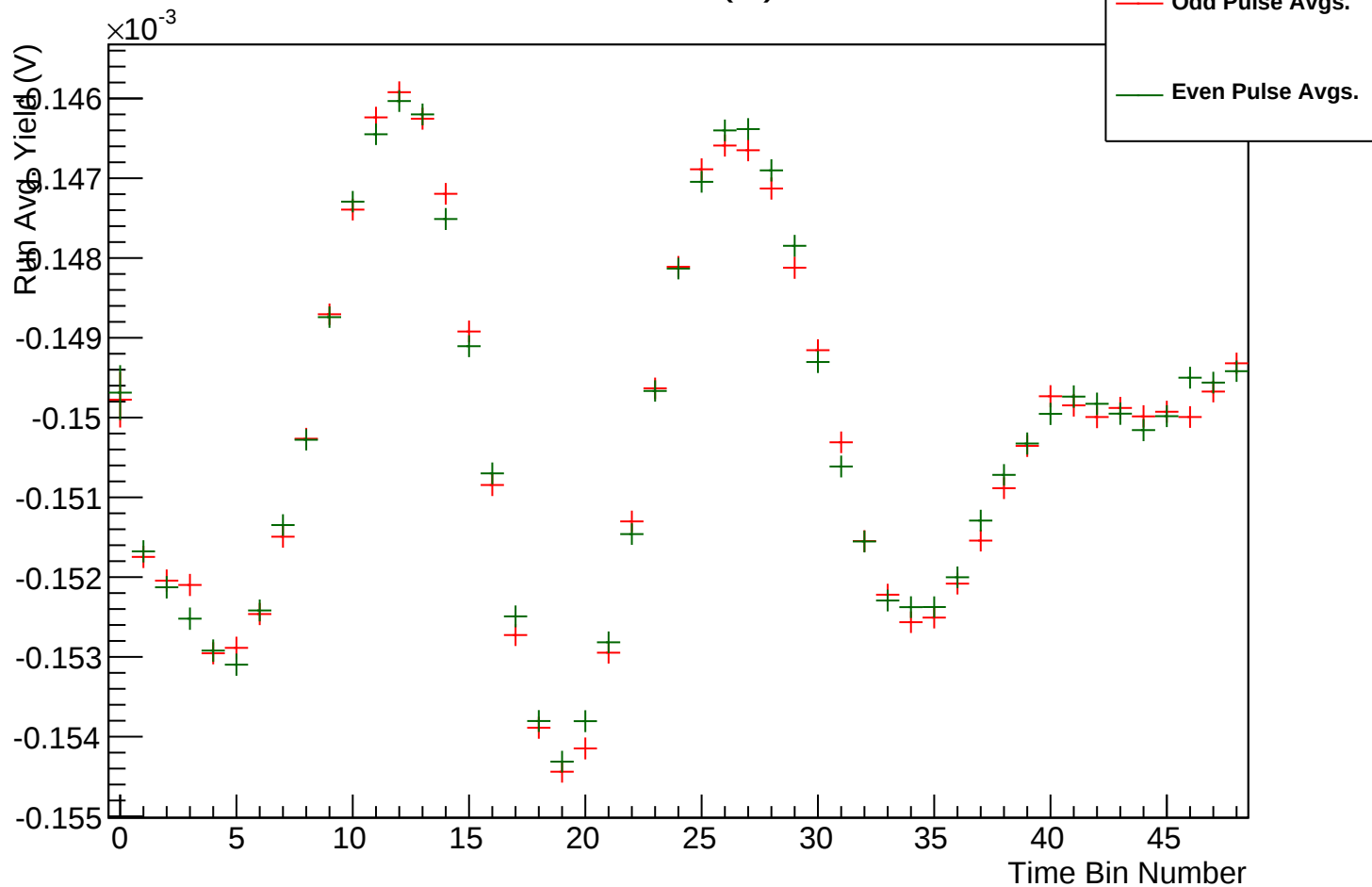
r17784-w118-Yield(V)-OddPulses



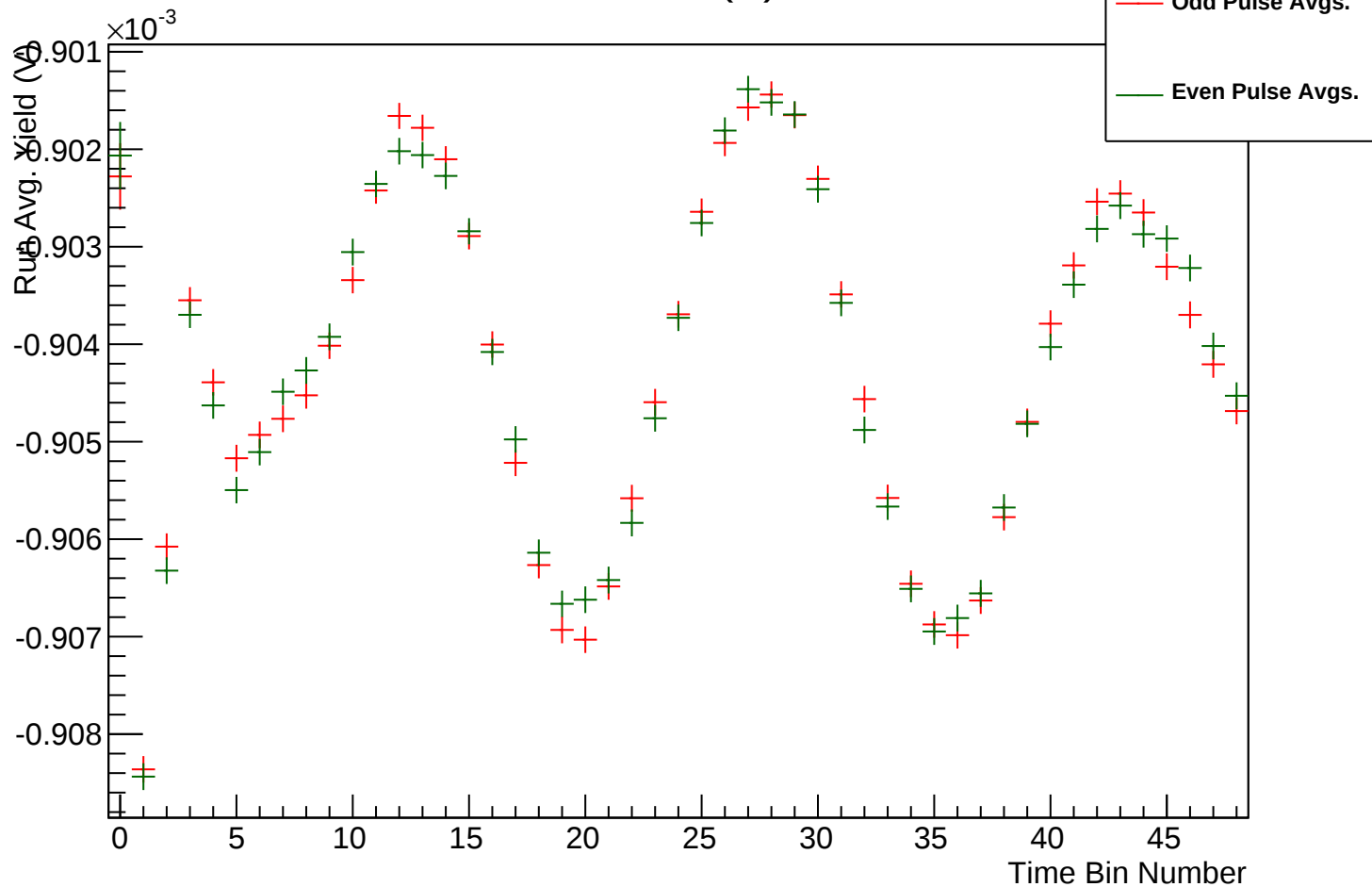
r17784-w119-Yield(V)-OddPulses



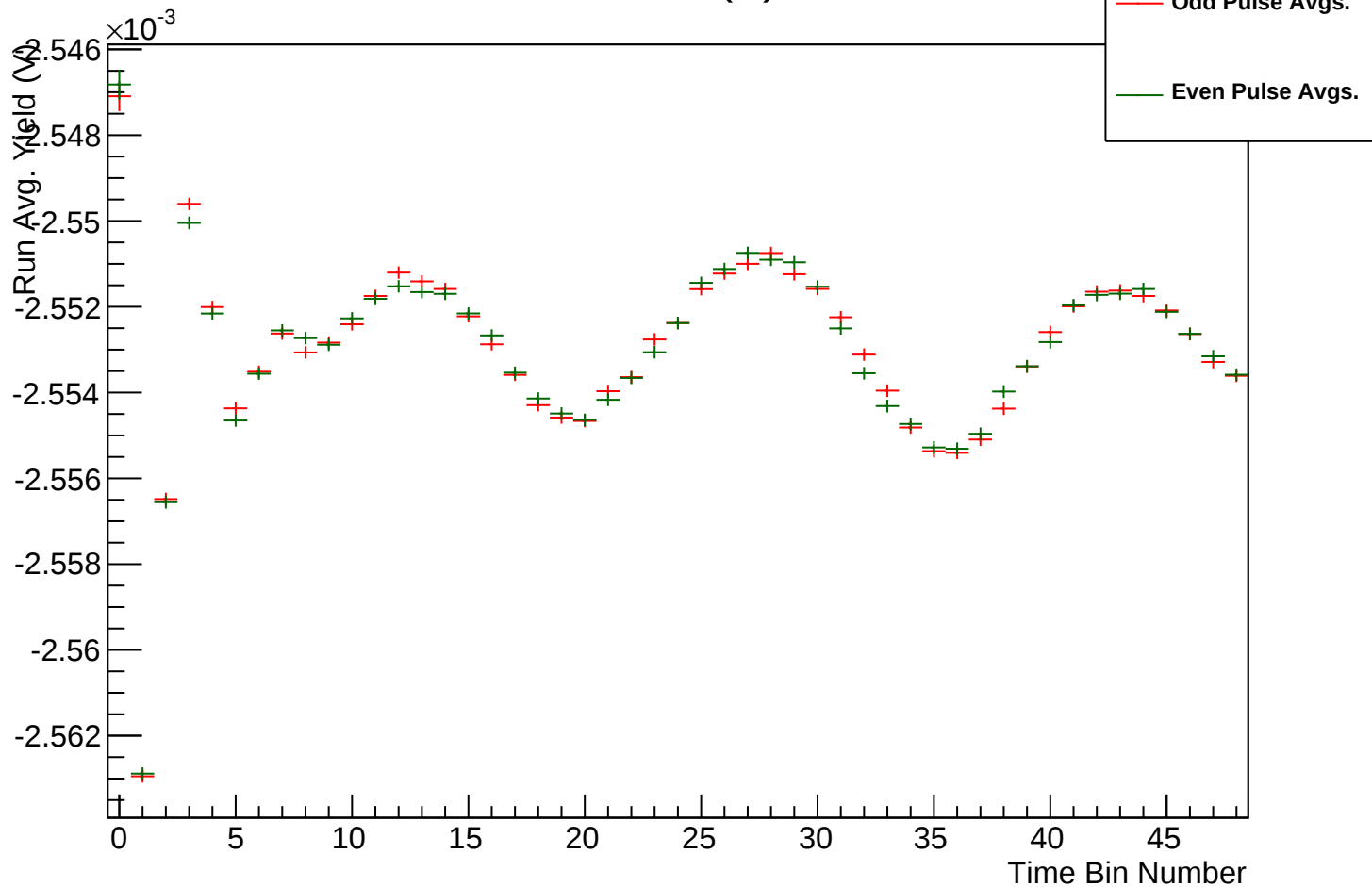
r17784-w120-Yield(V)-OddPulses



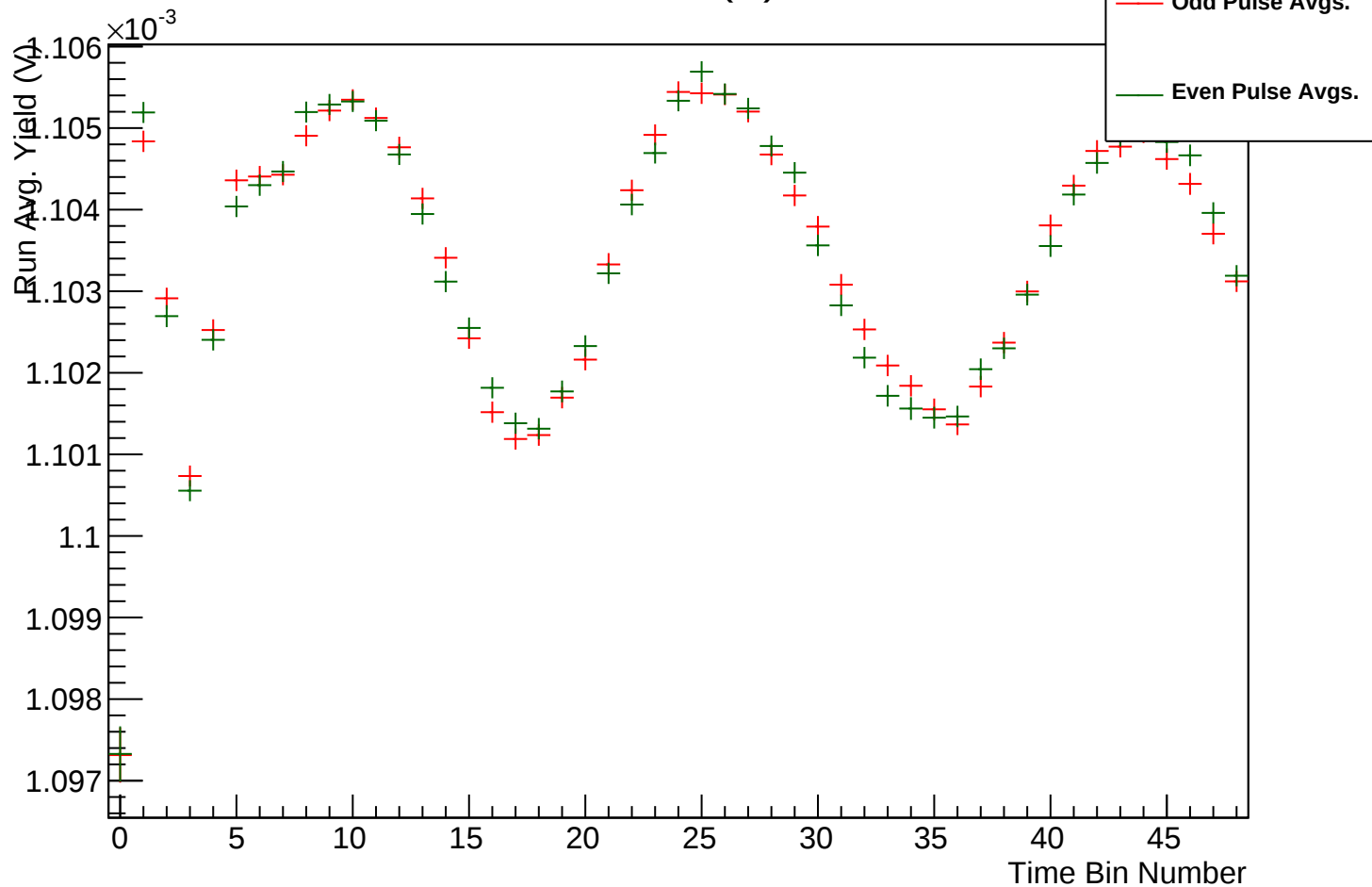
r17784-w121-Yield(V)-OddPulses



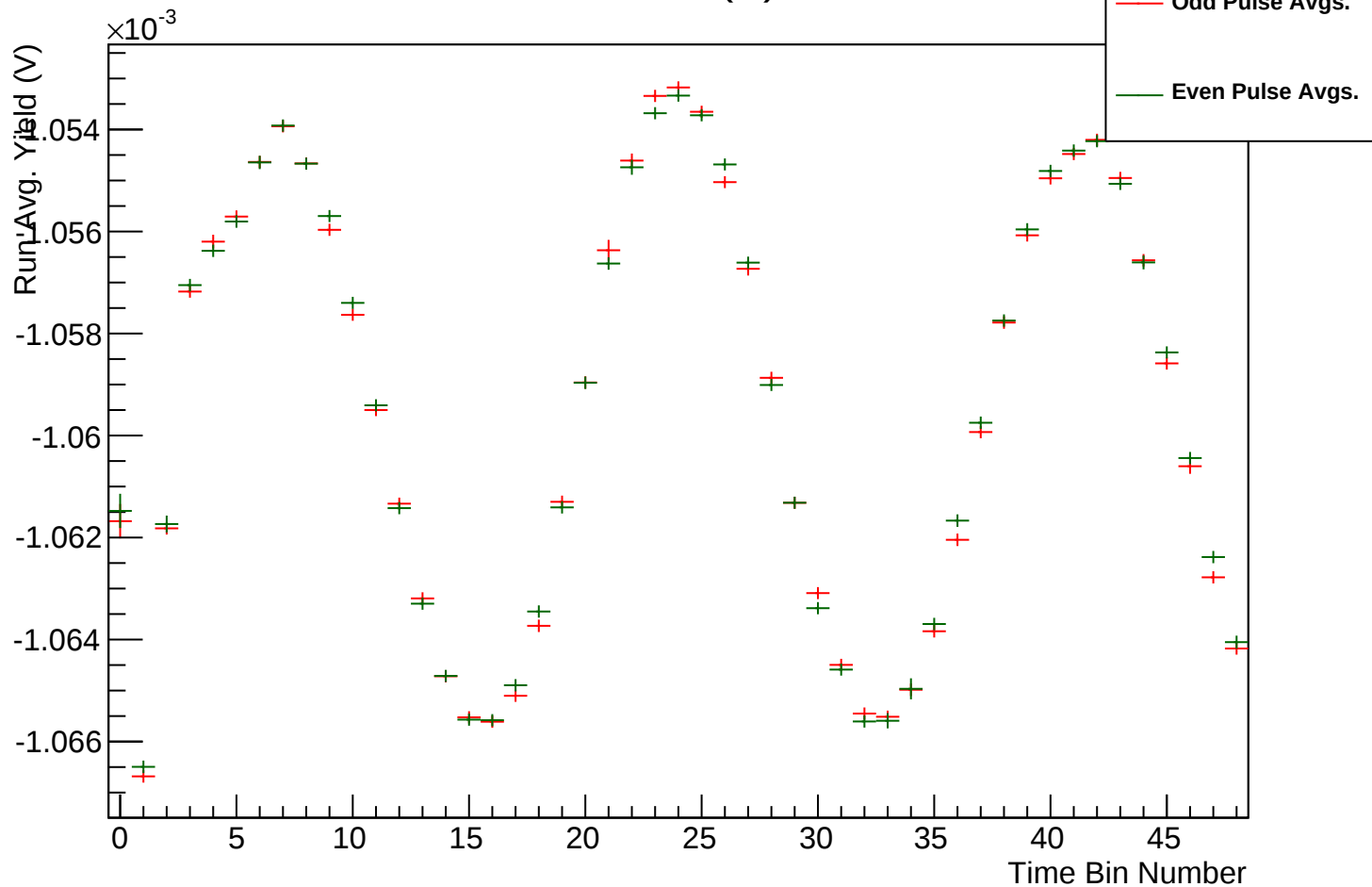
r17784-w122-Yield(V)-OddPulses



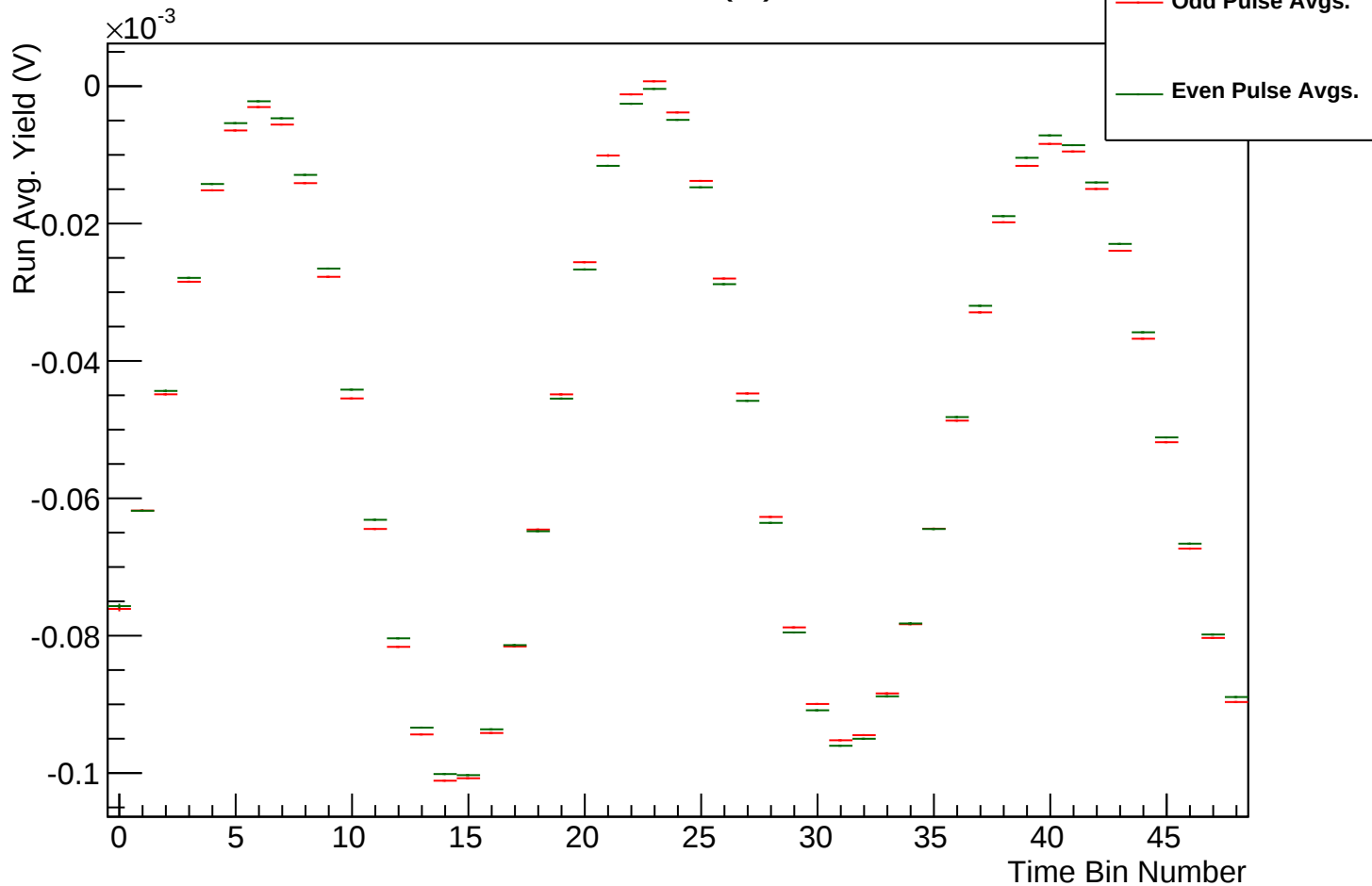
r17784-w123-Yield(V)-OddPulses



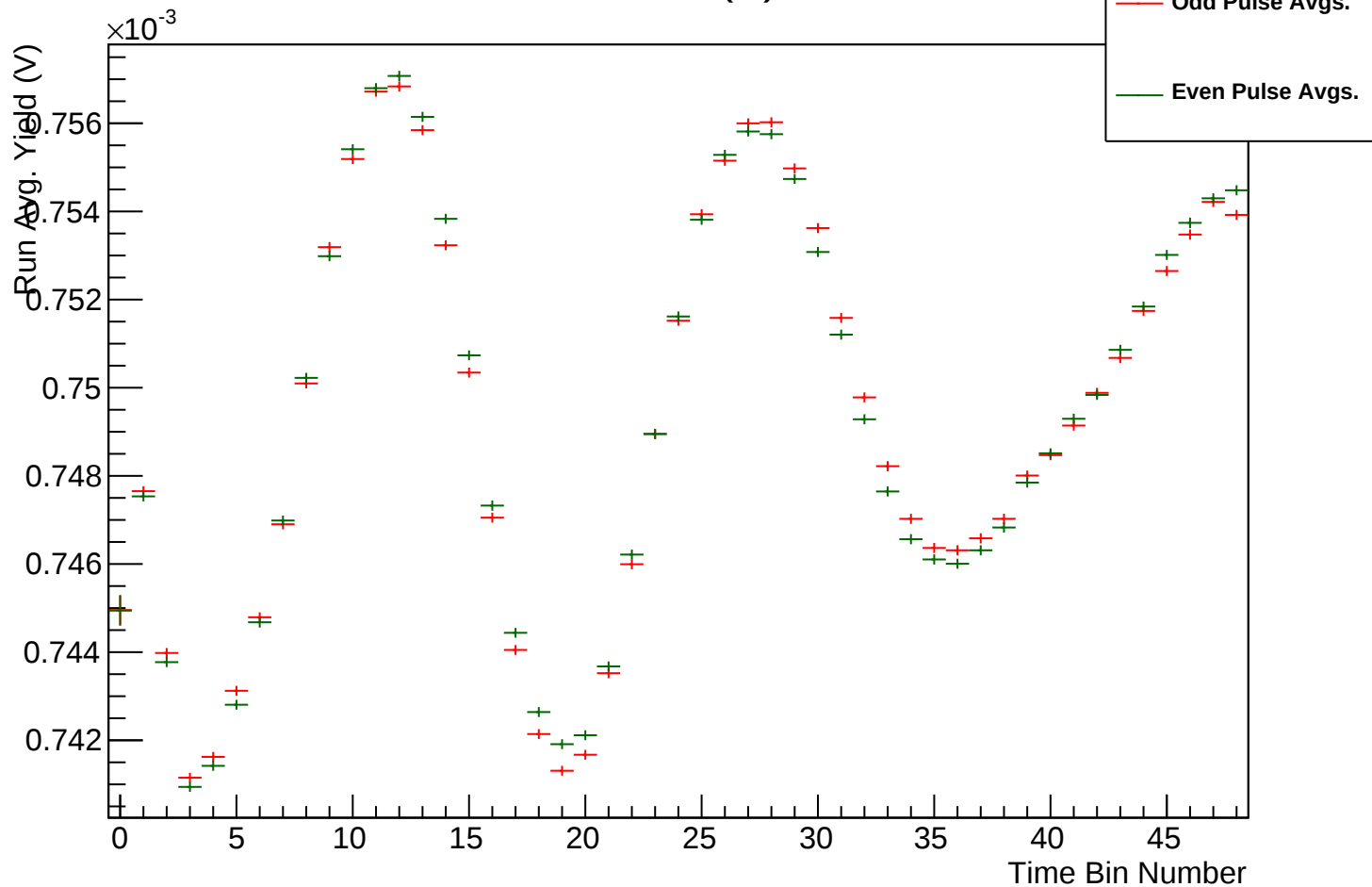
r17784-w124-Yield(V)-OddPulses



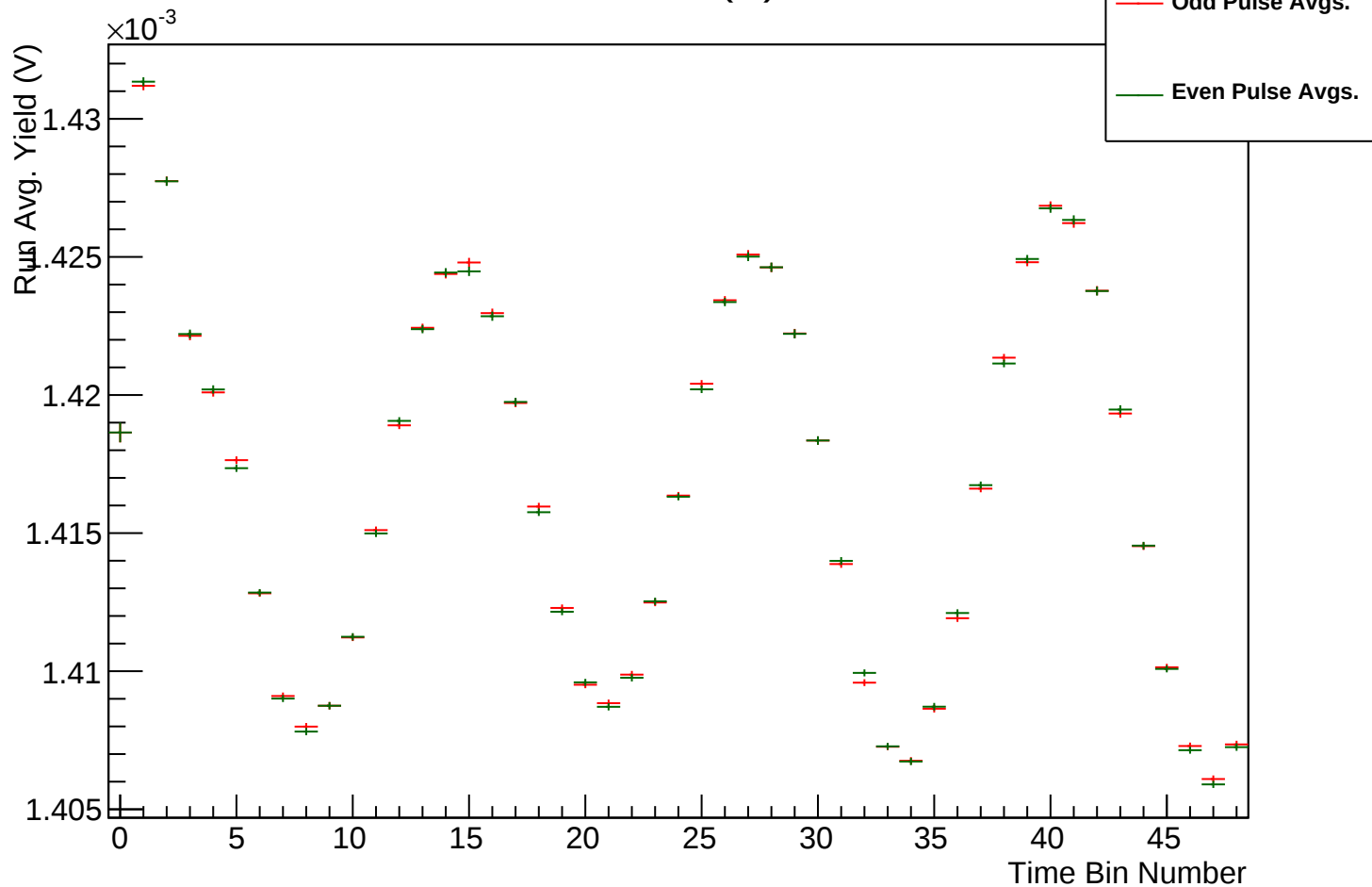
r17784-w125-Yield(V)-OddPulses



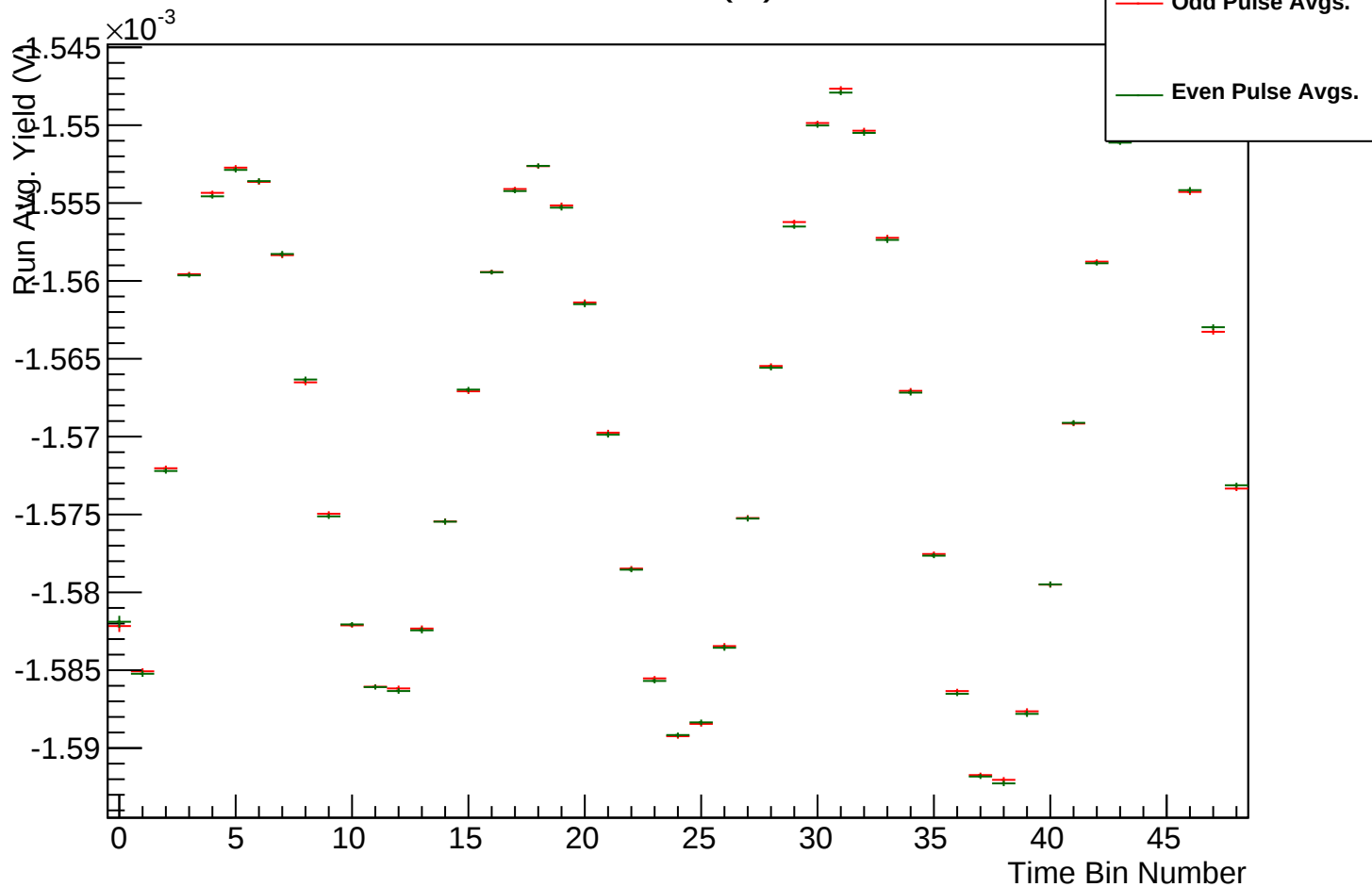
r17784-w126-Yield(V)-OddPulses



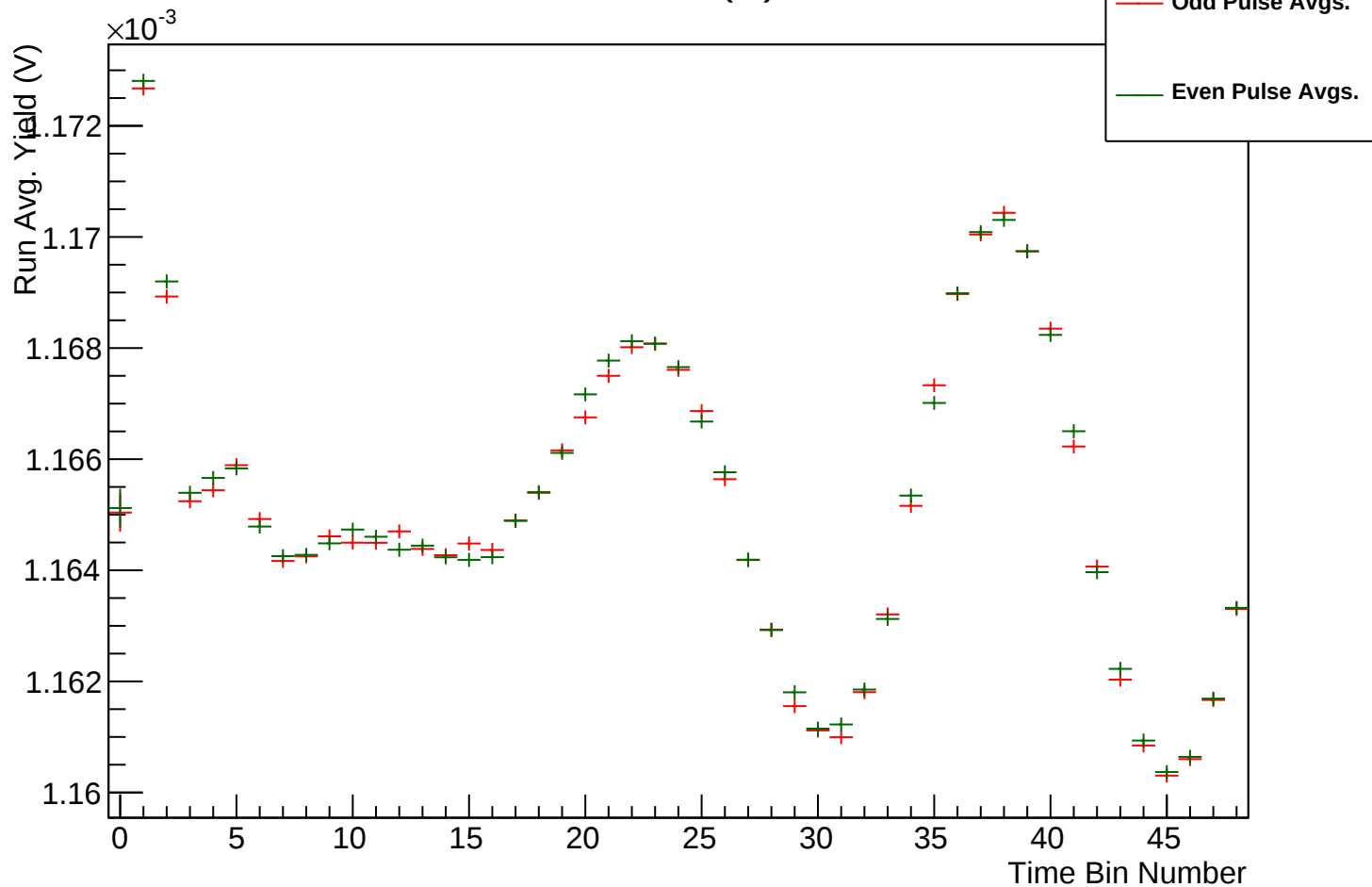
r17784-w127-Yield(V)-OddPulses



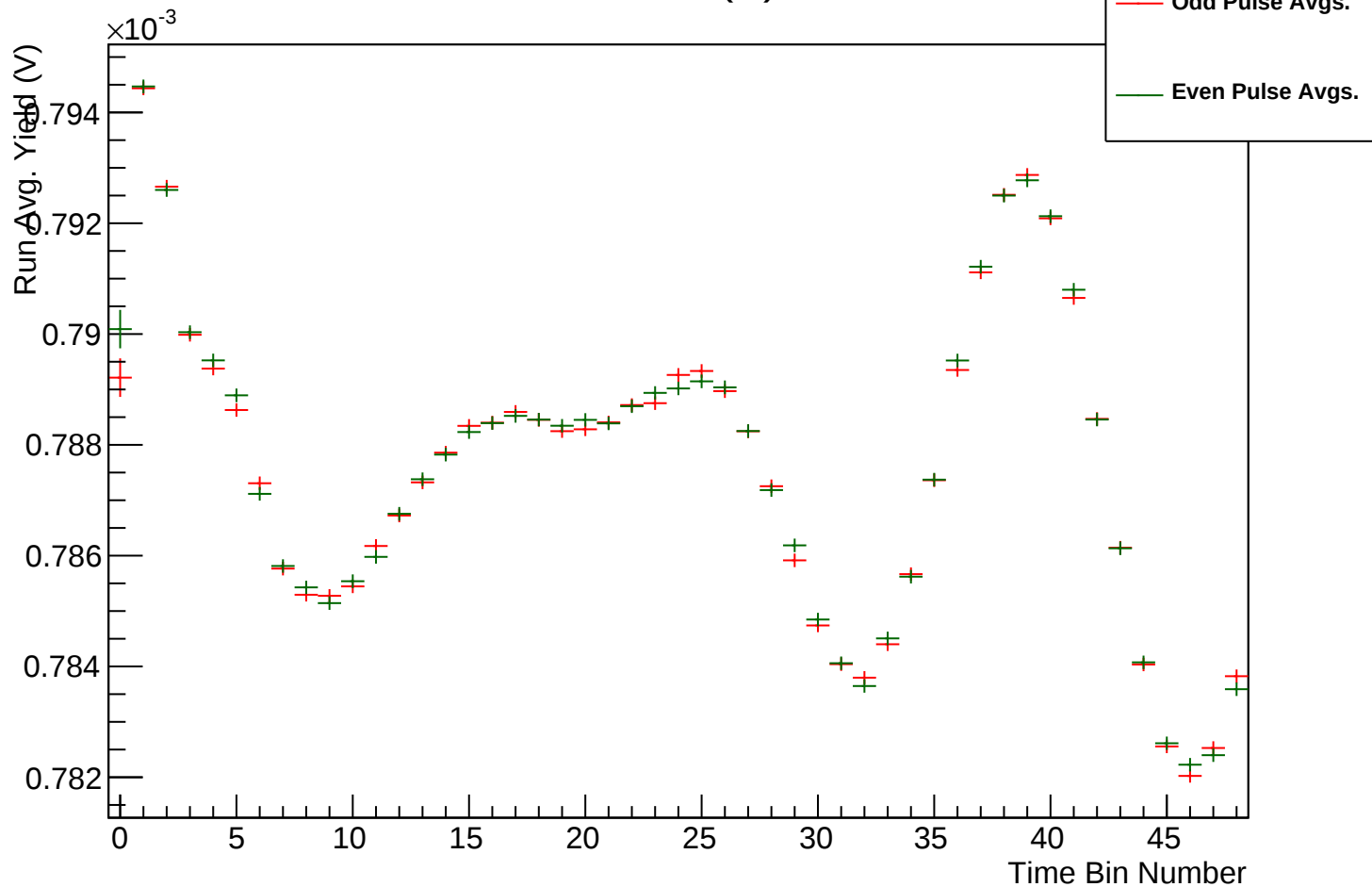
r17784-w128-Yield(V)-OddPulses



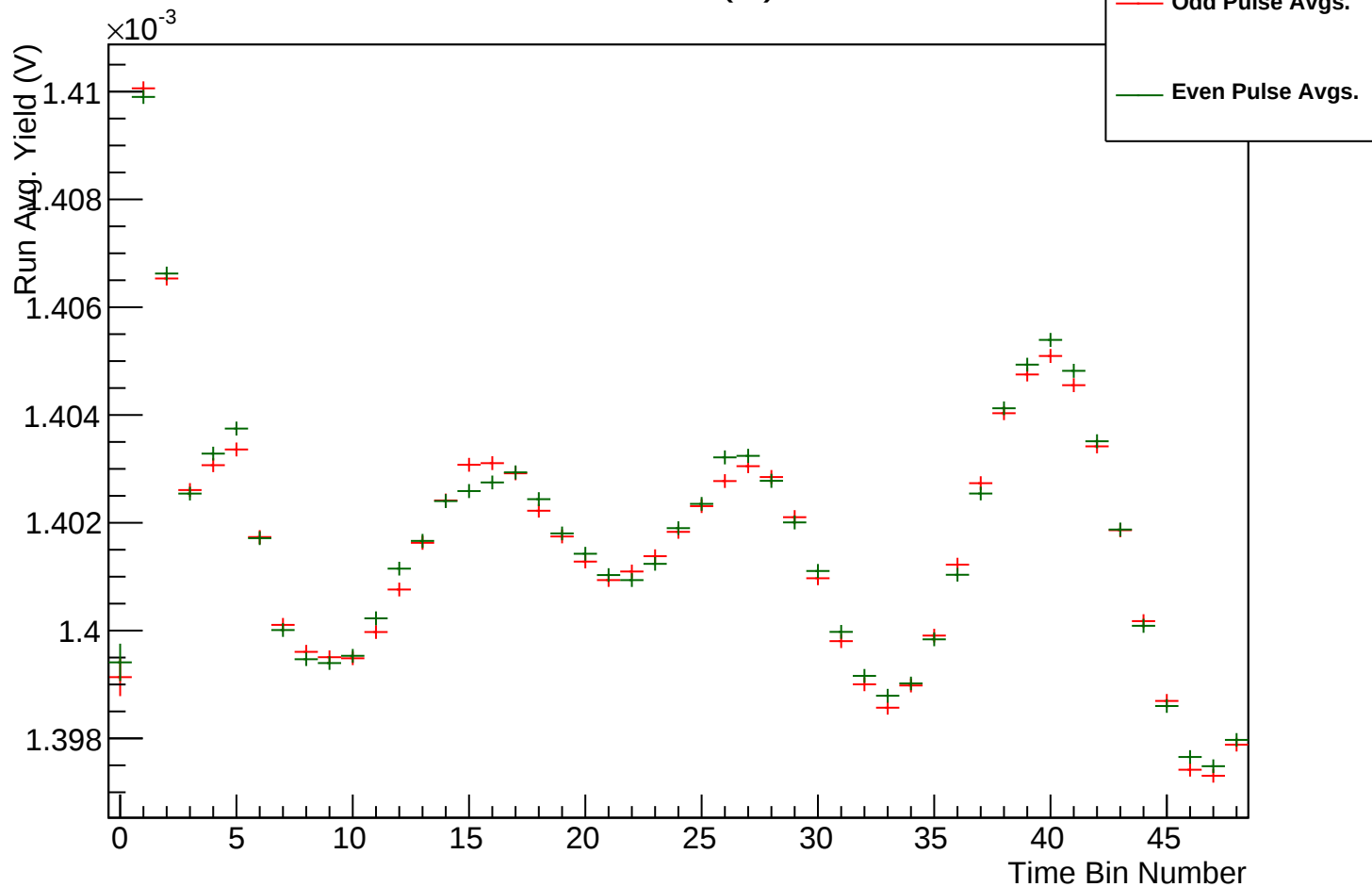
r17784-w129-Yield(V)-OddPulses



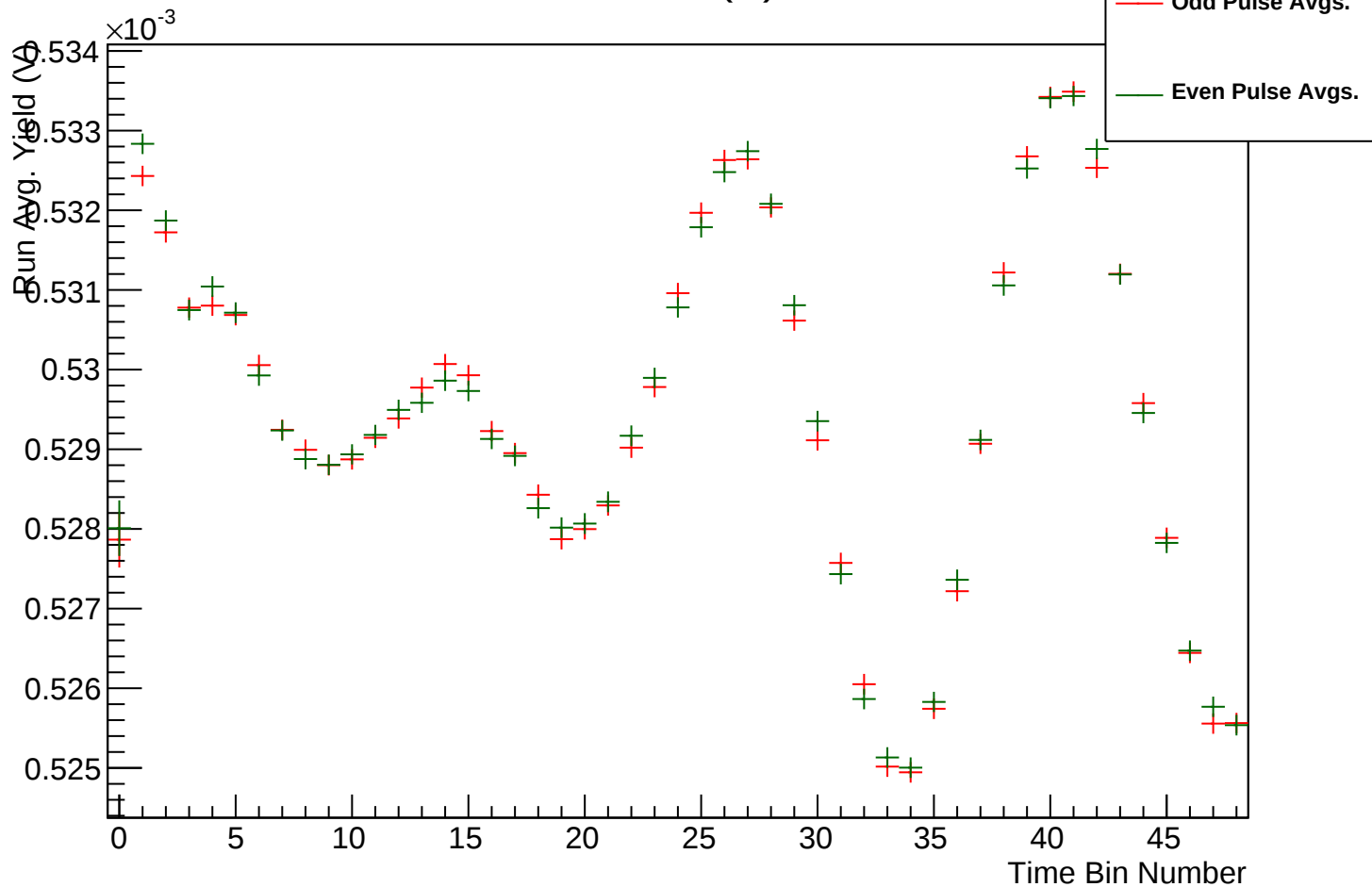
r17784-w130-Yield(V)-OddPulses



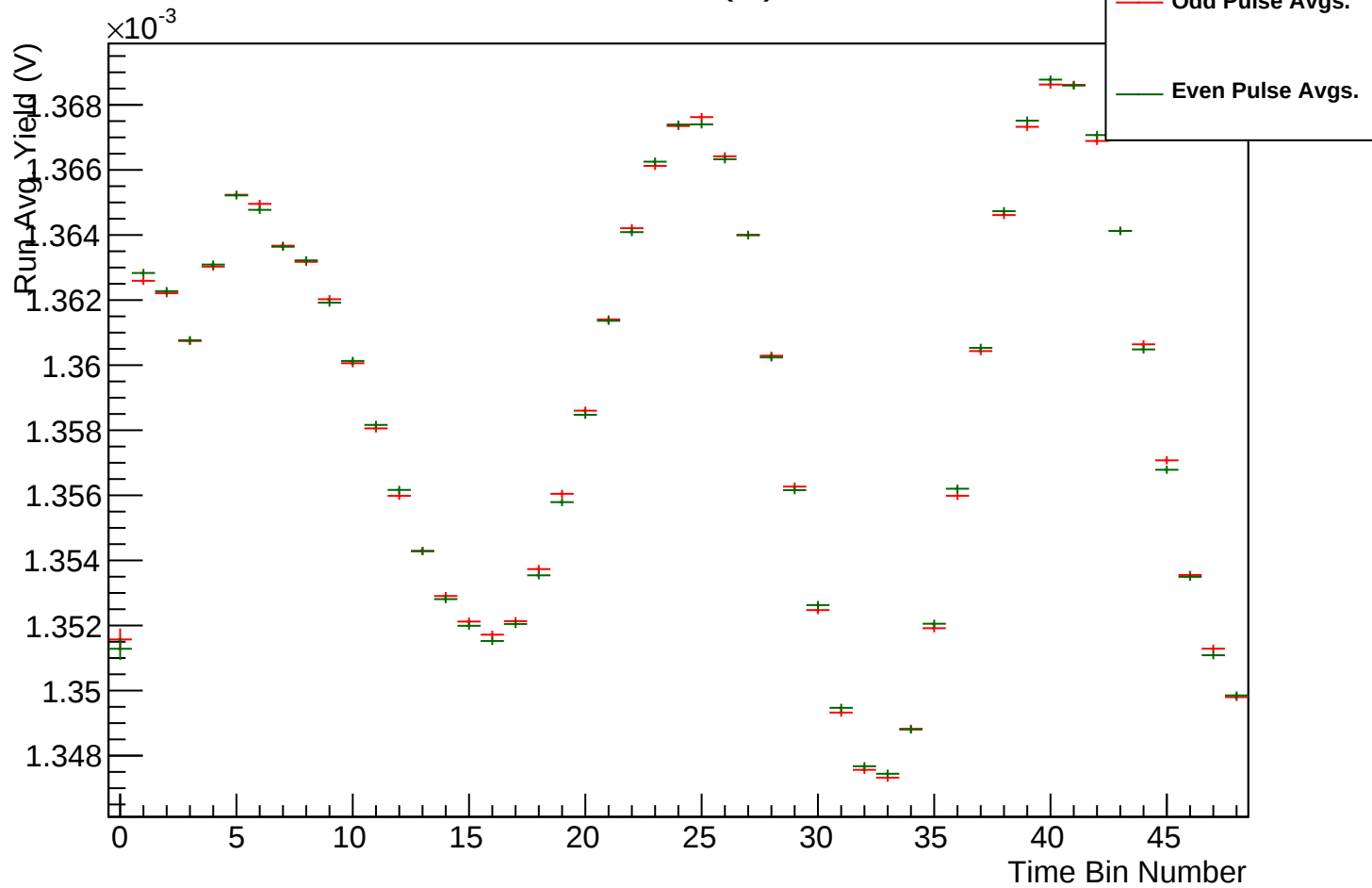
r17784-w131-Yield(V)-OddPulses



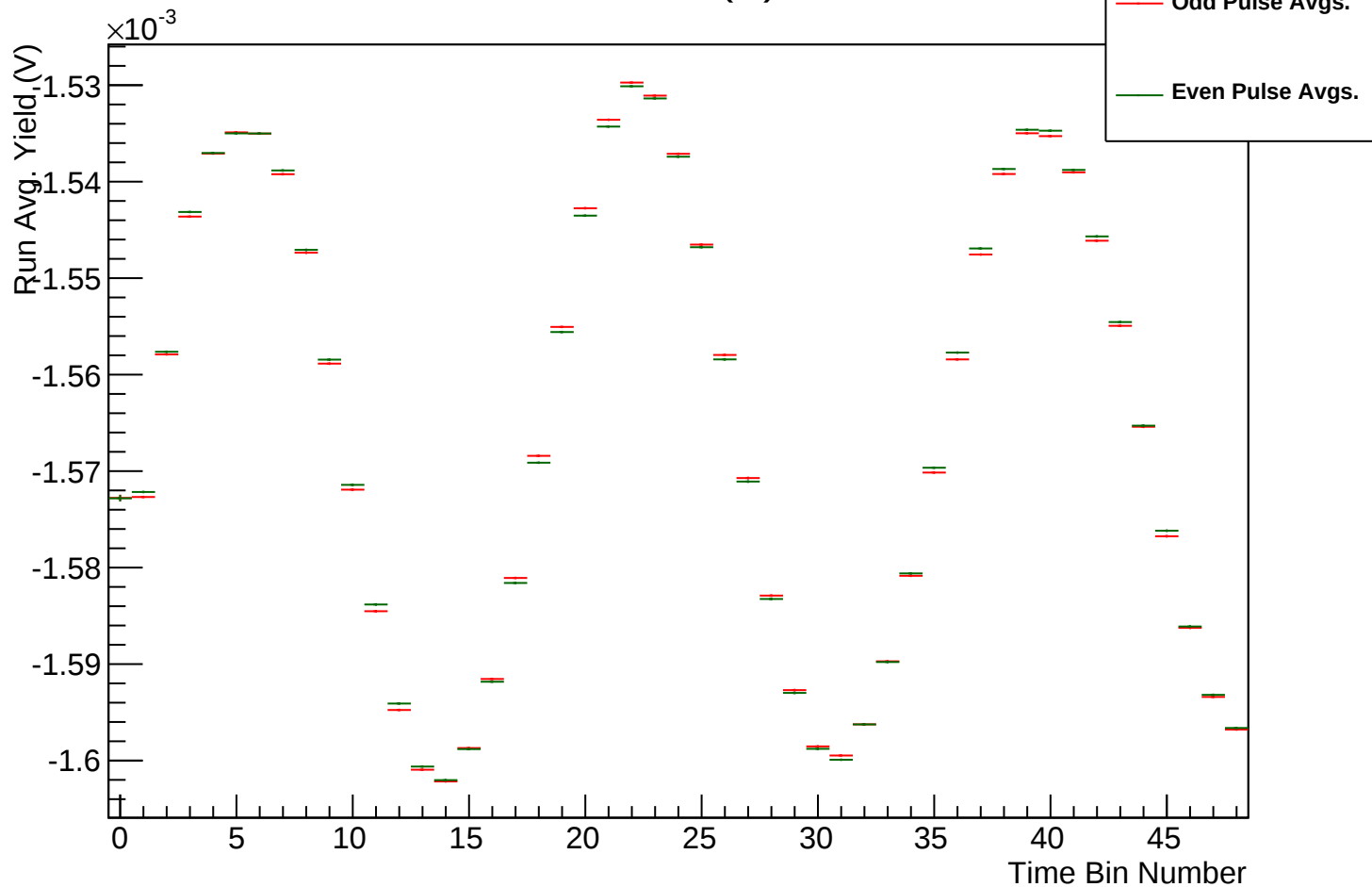
r17784-w132-Yield(V)-OddPulses



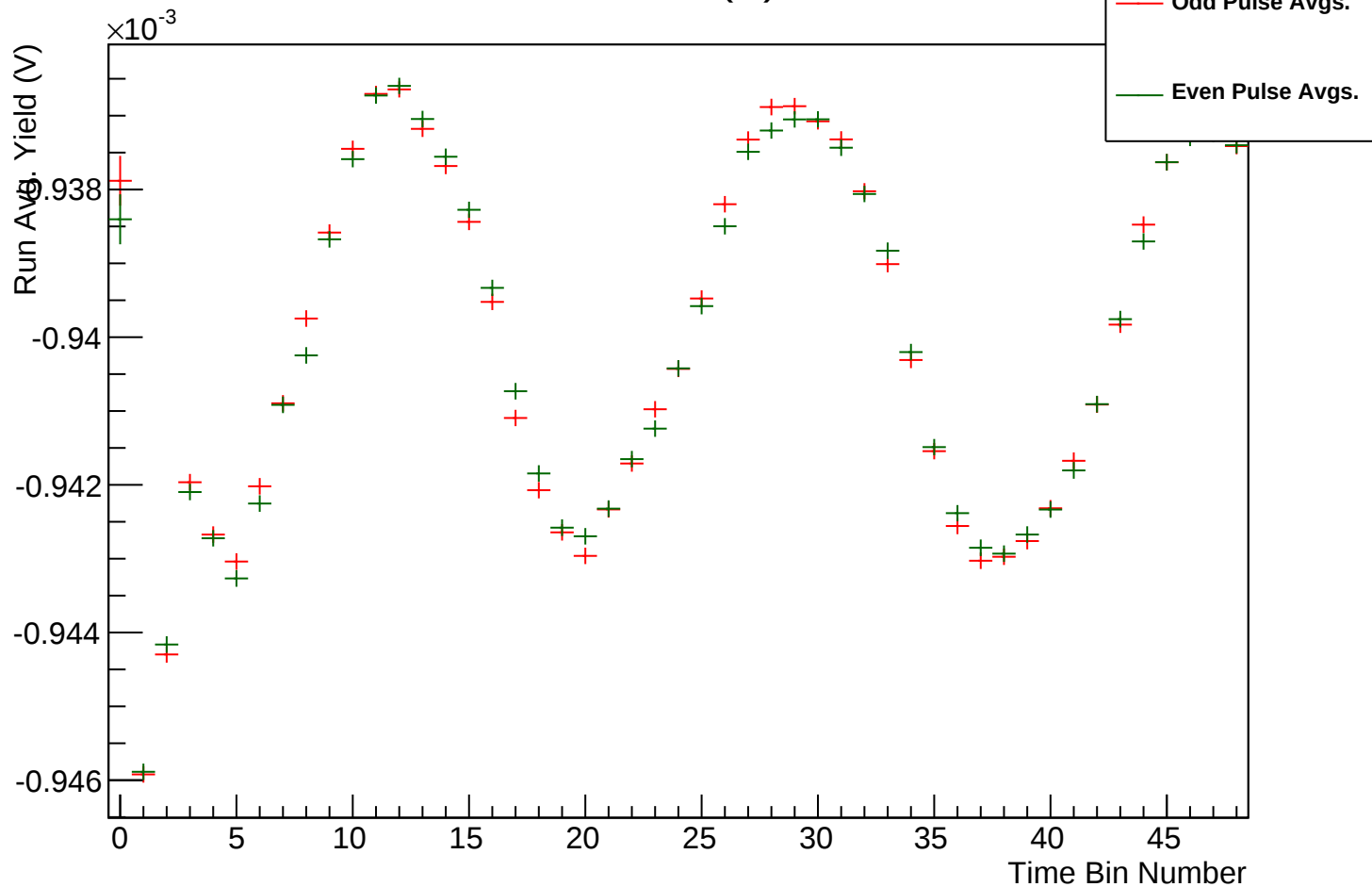
r17784-w133-Yield(V)-OddPulses



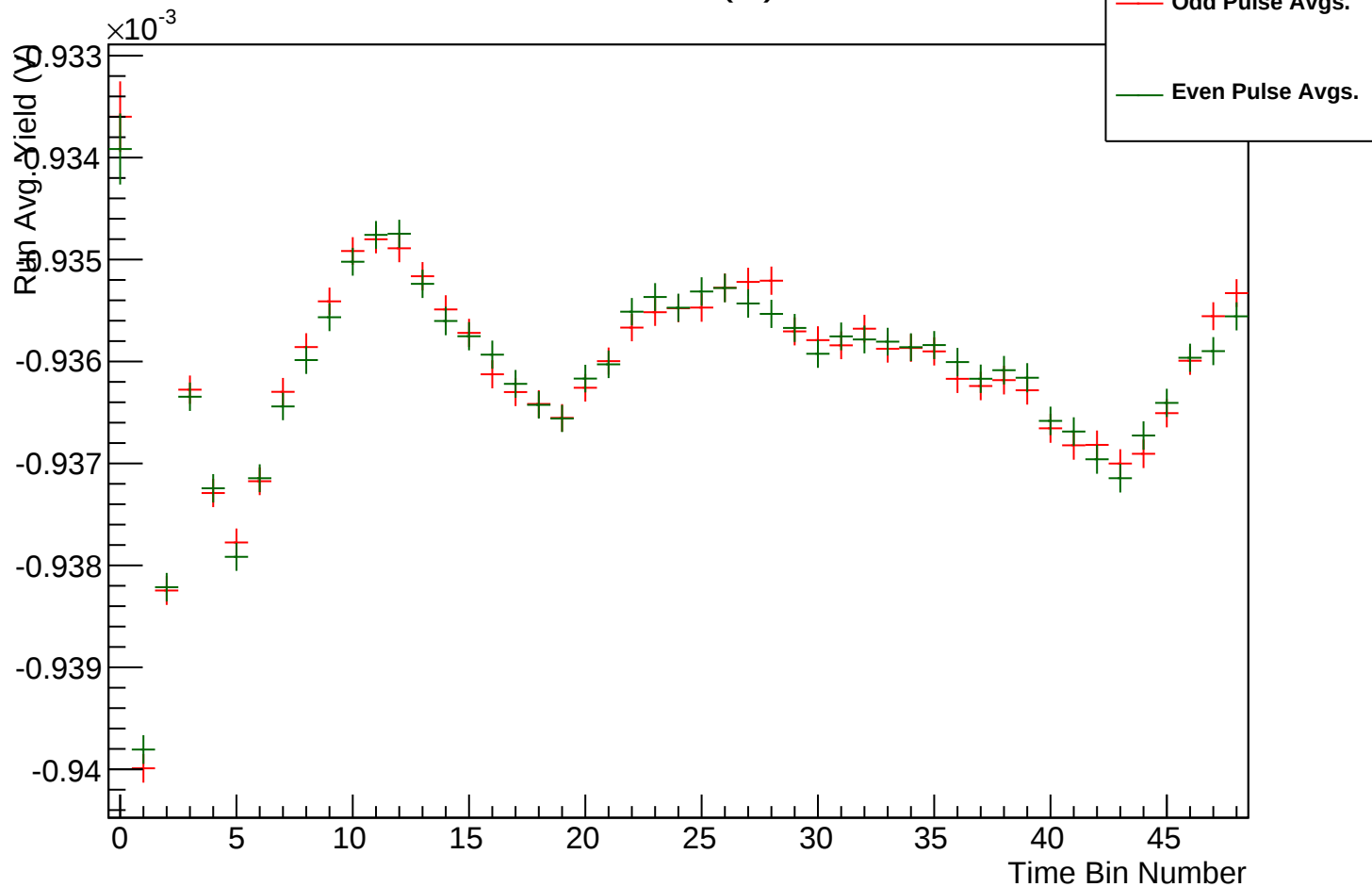
r17784-w134-Yield(V)-OddPulses



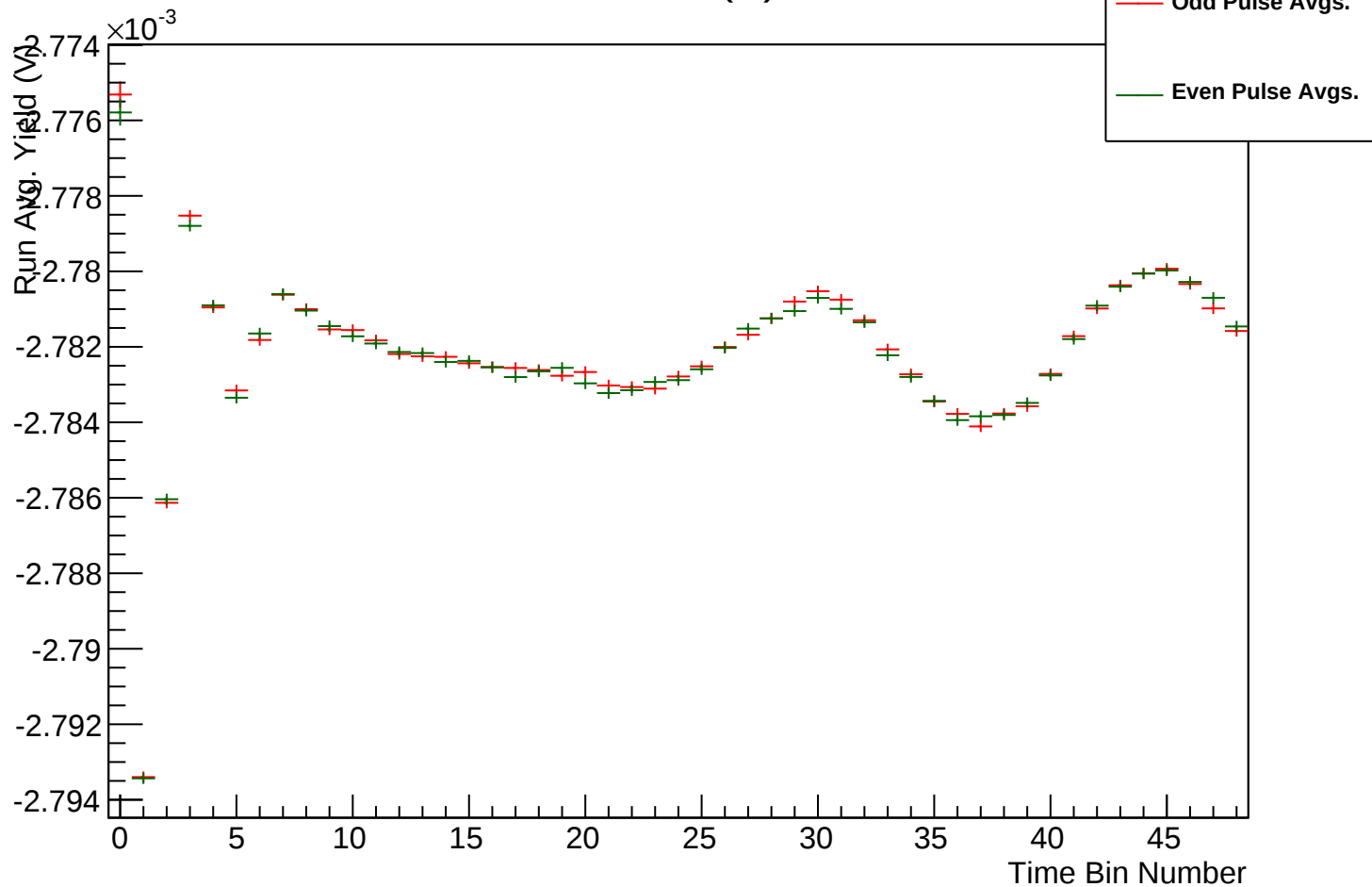
r17784-w135-Yield(V)-OddPulses



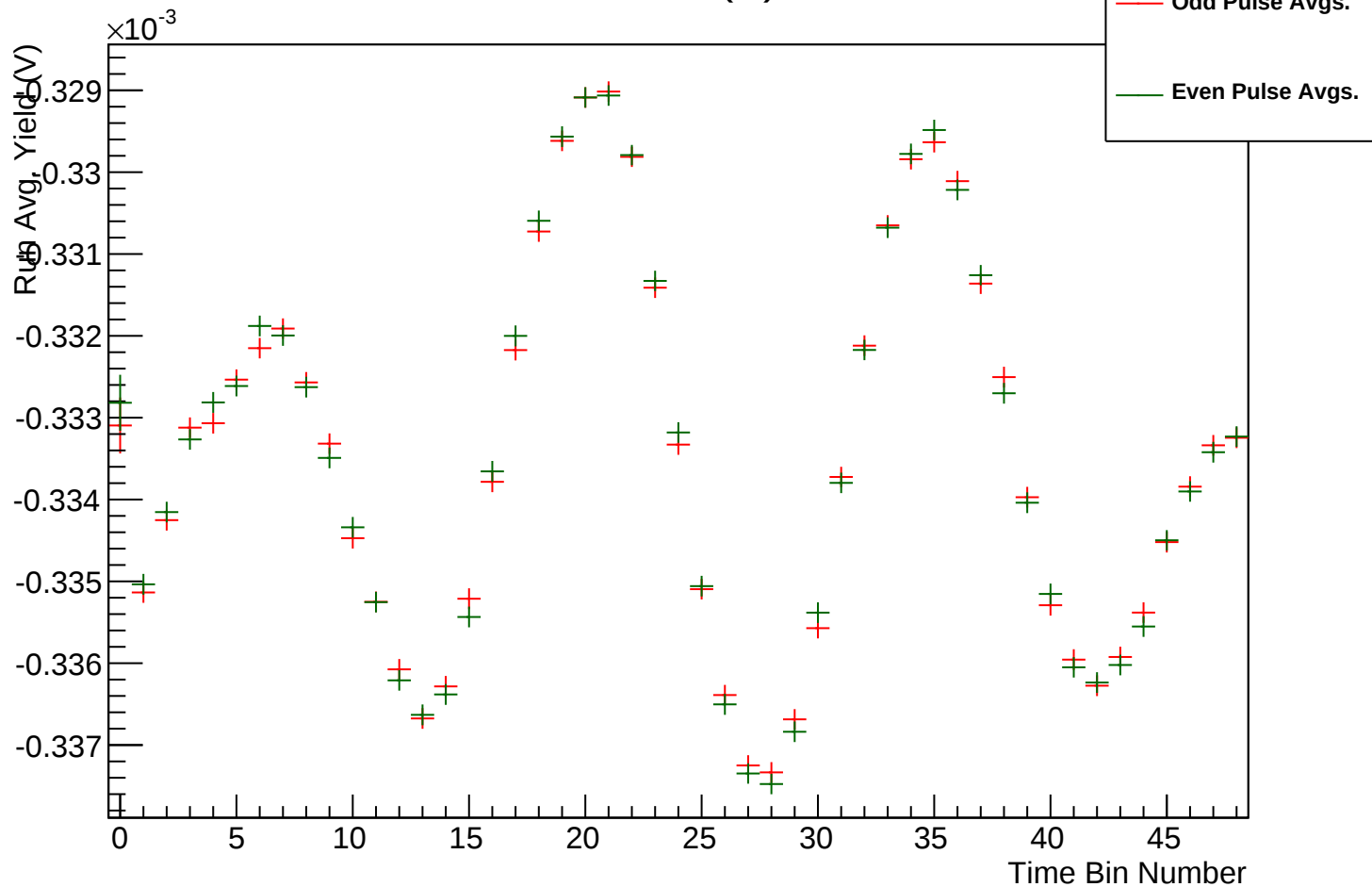
r17784-w136-Yield(V)-OddPulses



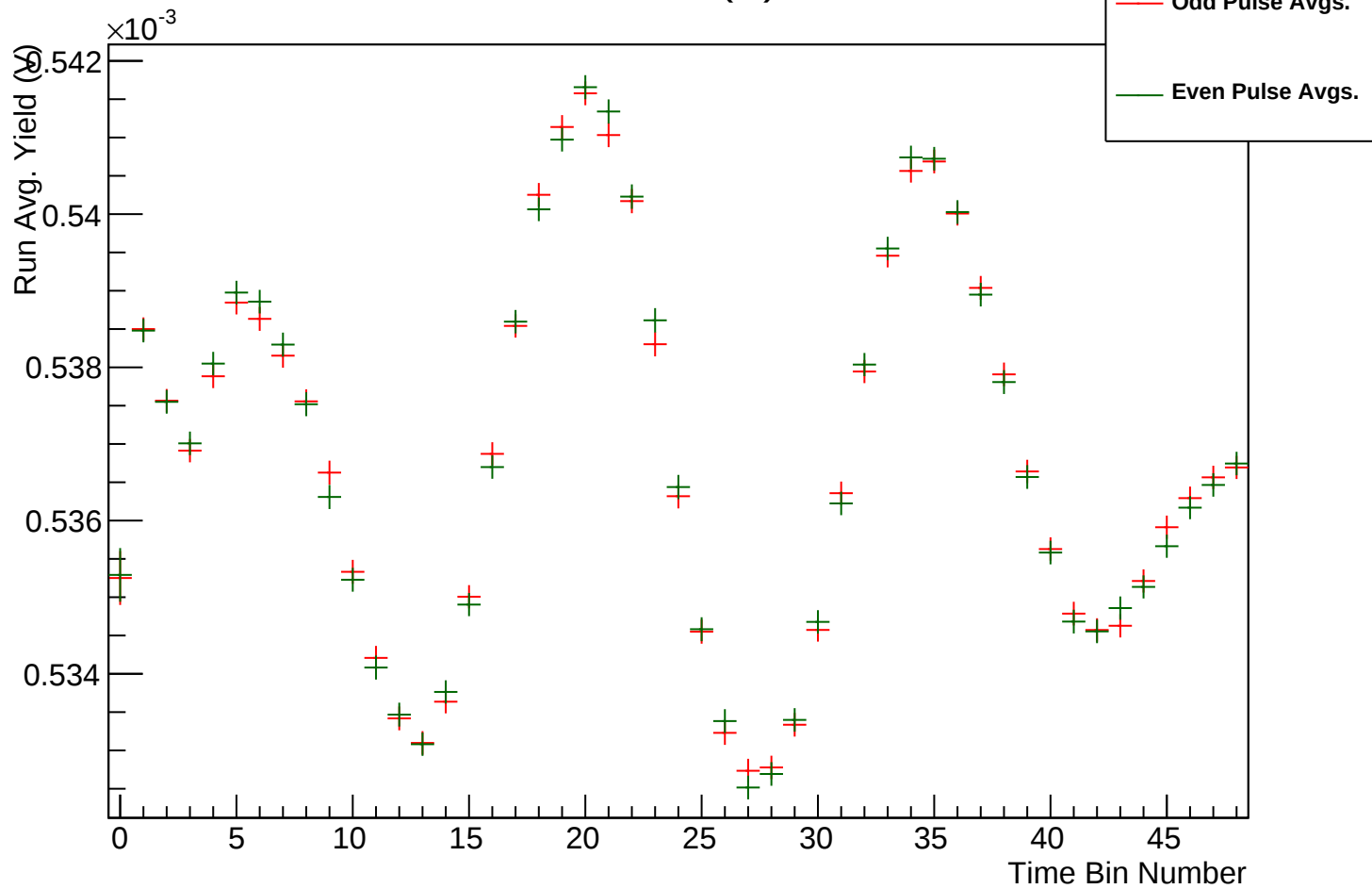
r17784-w137-Yield(V)-OddPulses



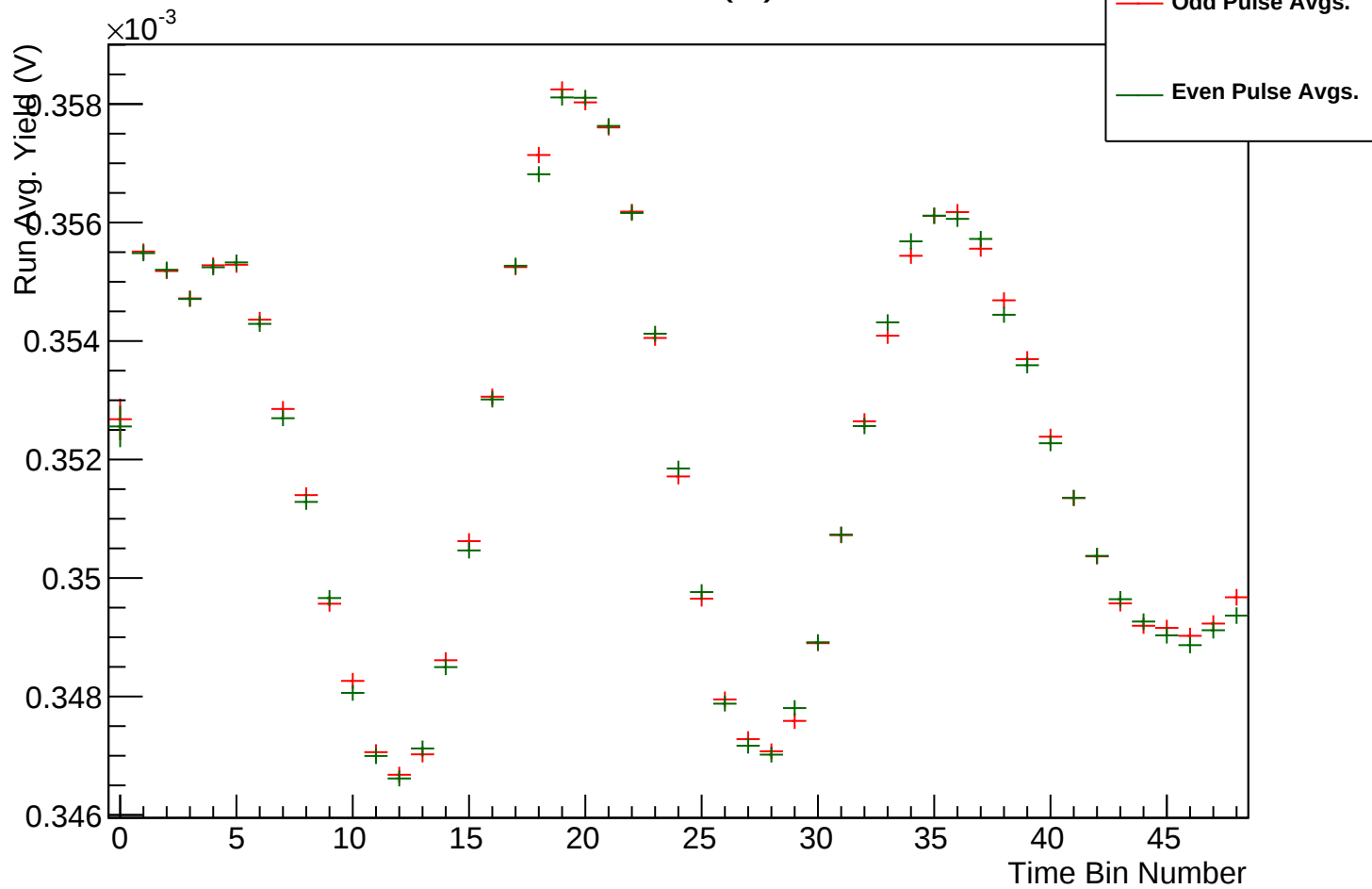
r17784-w138-Yield(V)-OddPulses



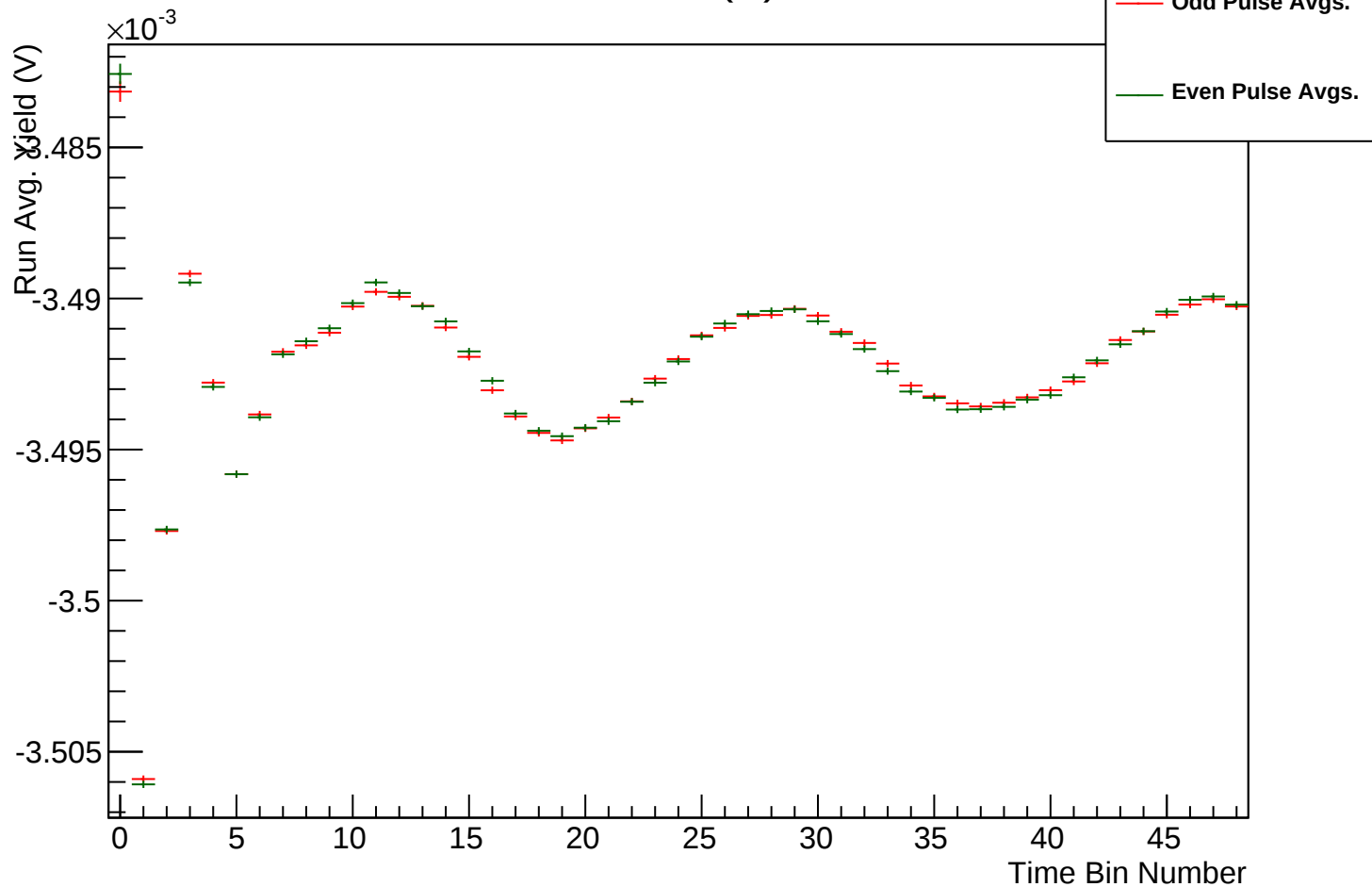
r17784-w139-Yield(V)-OddPulses



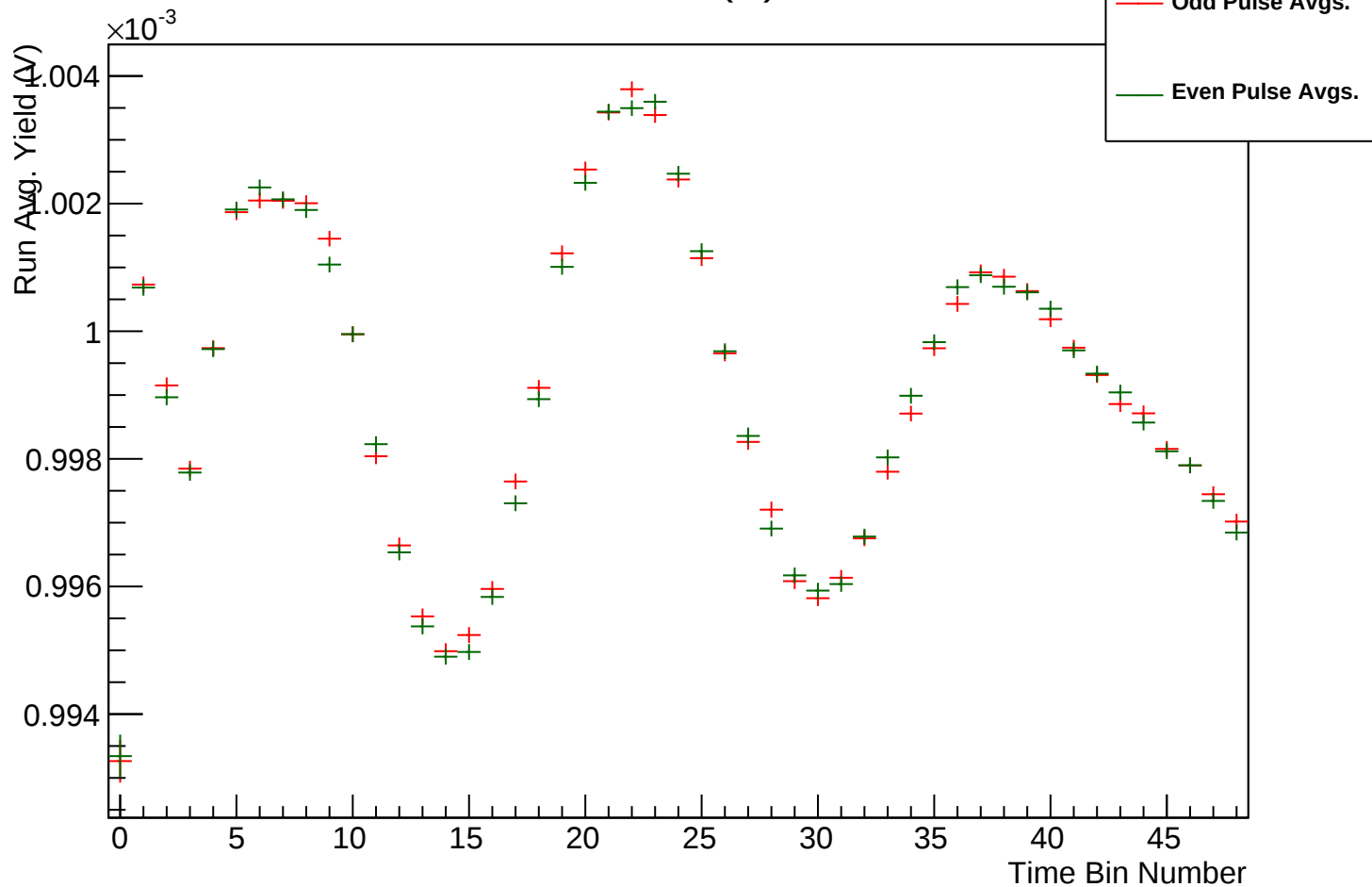
r17784-w140-Yield(V)-OddPulses



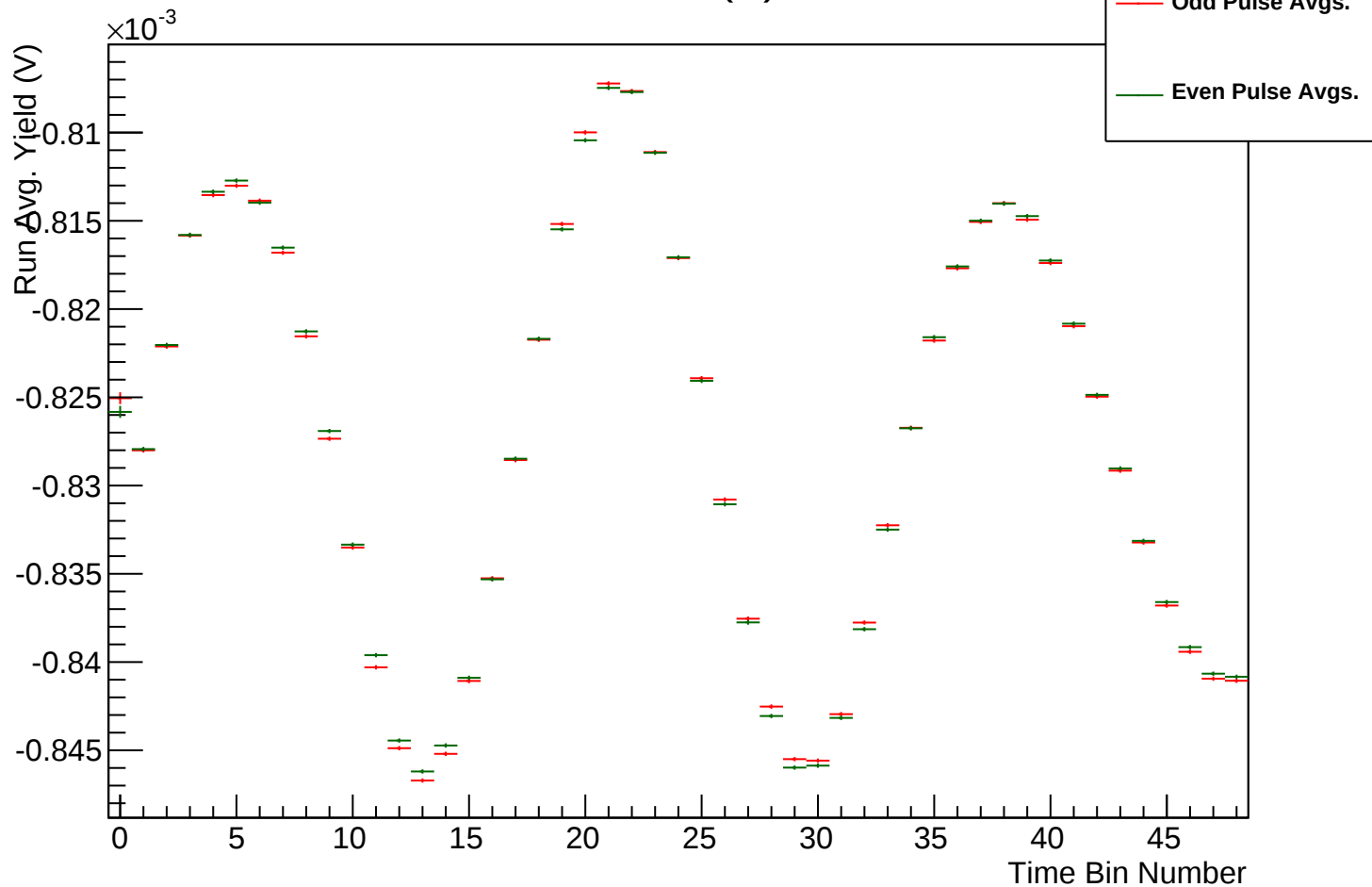
r17784-w141-Yield(V)-OddPulses



r17784-w142-Yield(V)-OddPulses



r17784-w143-Yield(V)-OddPulses



Create on Date: Wed Aug 23 17:38:54 2017

Created by: M. McCrea

Created from: TBinPlots-WireYields.C

Date Source: TTreeRaw(17784)

Data Format Info:

this file contains the run average wire yield

for all time bins of all 144 wires for even odd and.

other pulse combinations.