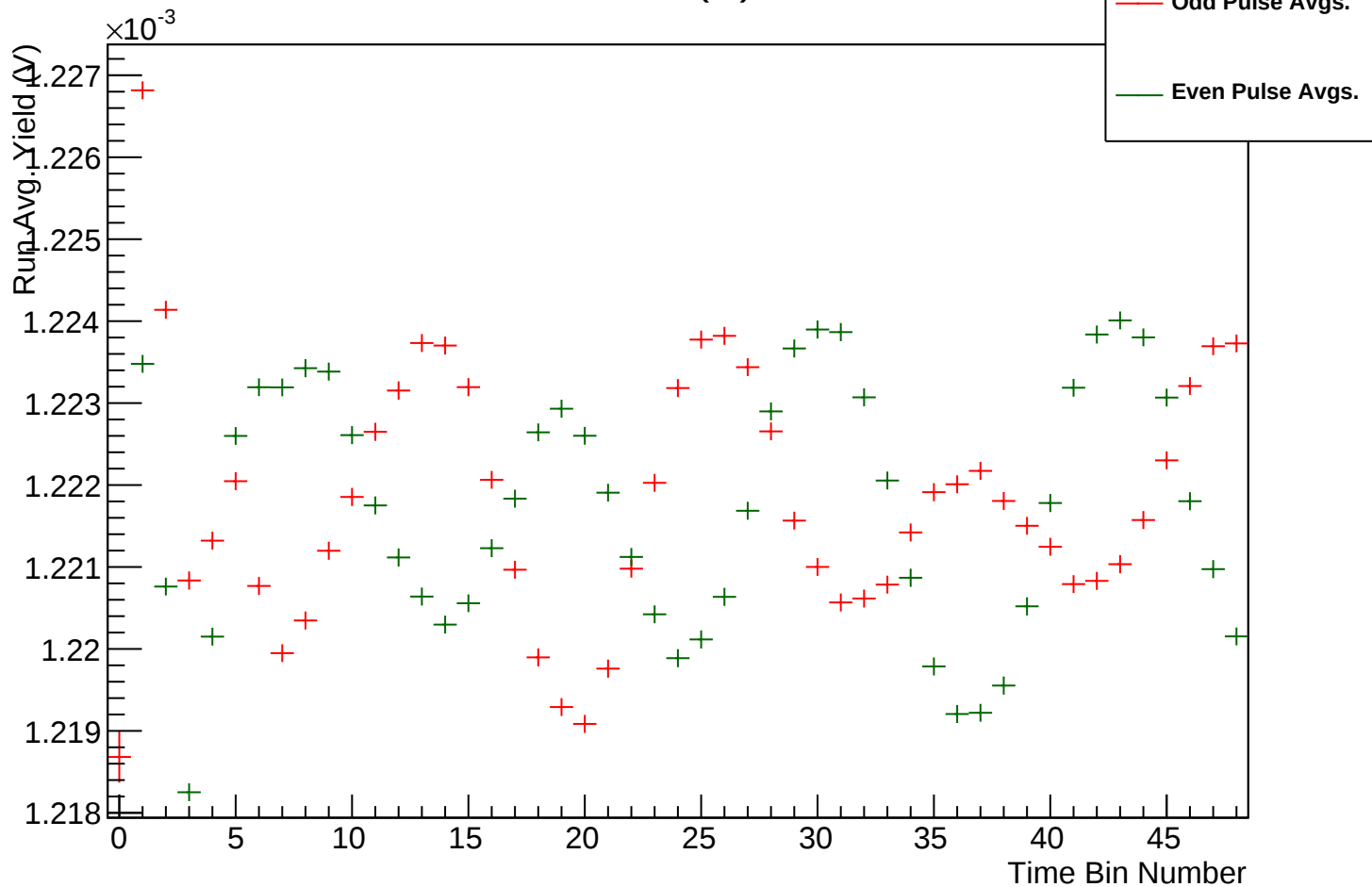
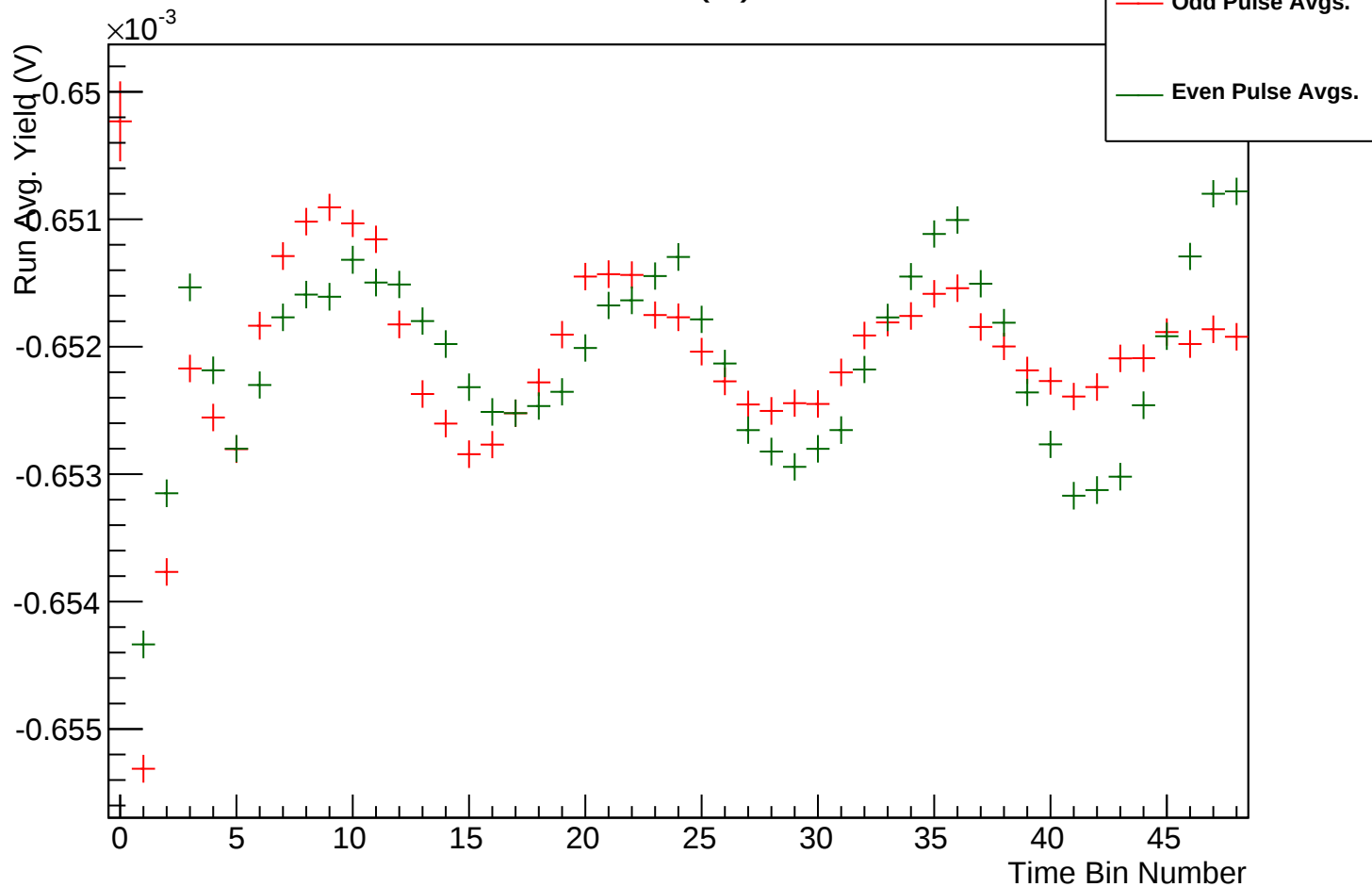


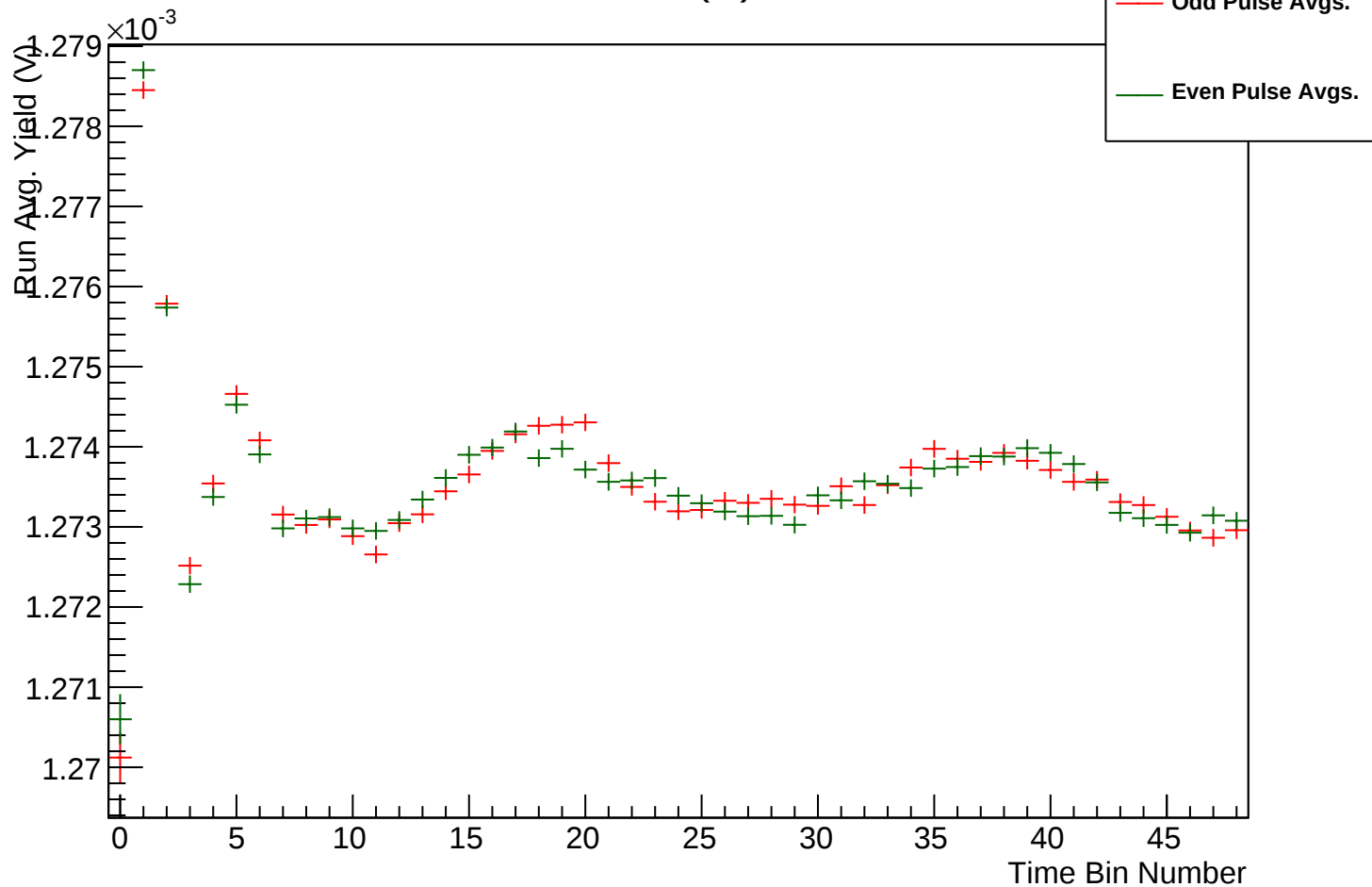
r38314-w0-Yield(V)-OddPulses



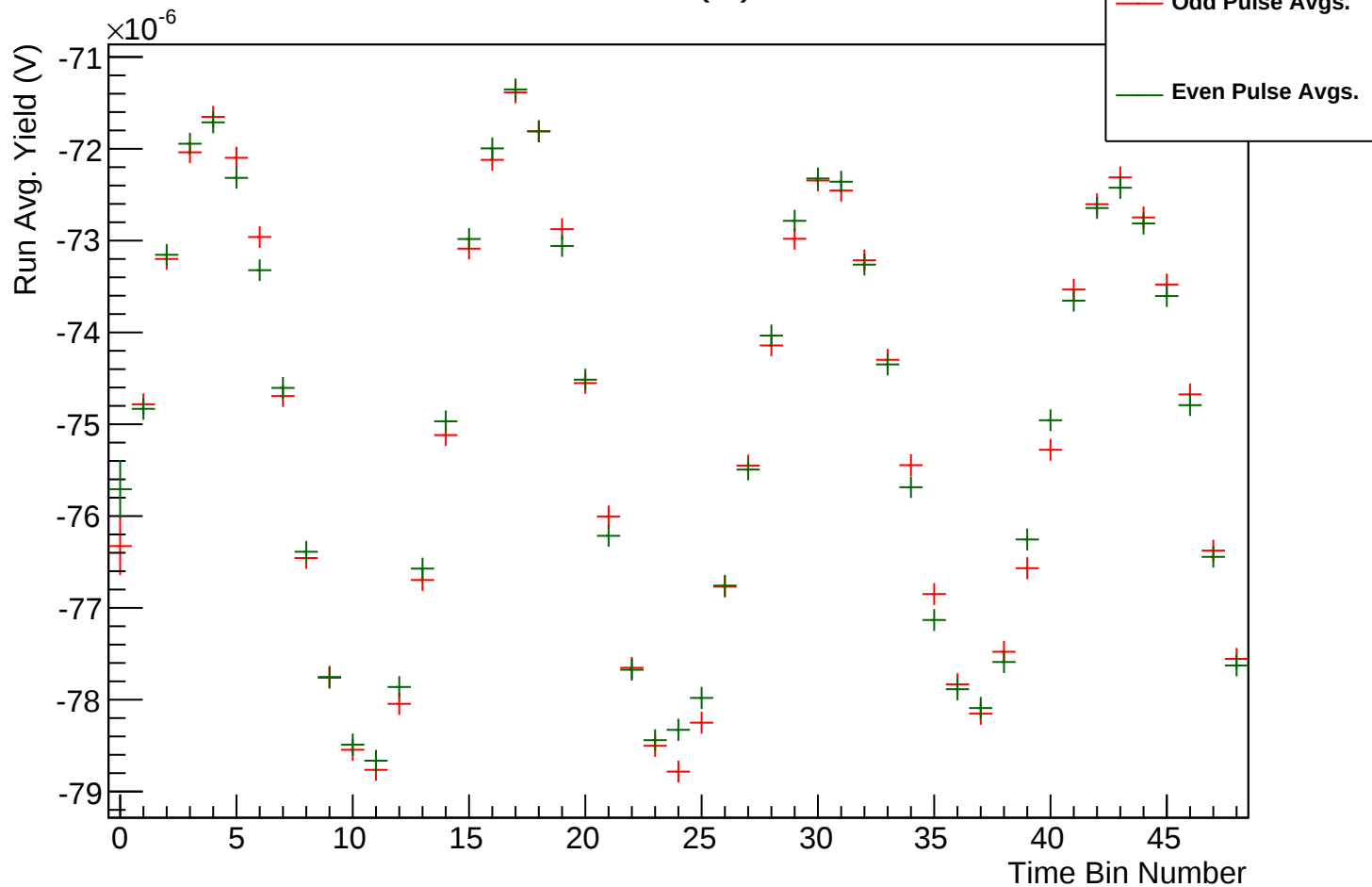
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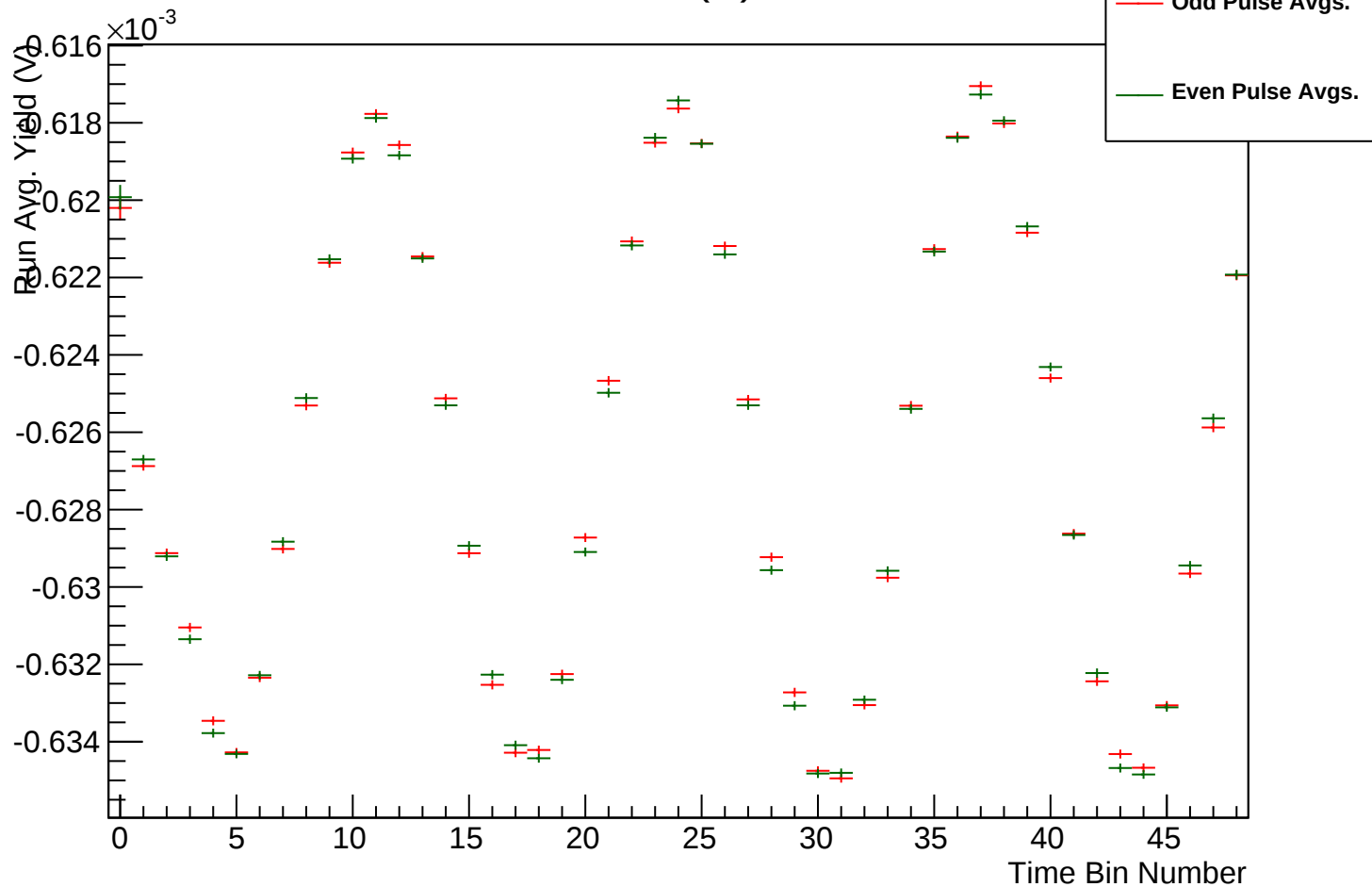
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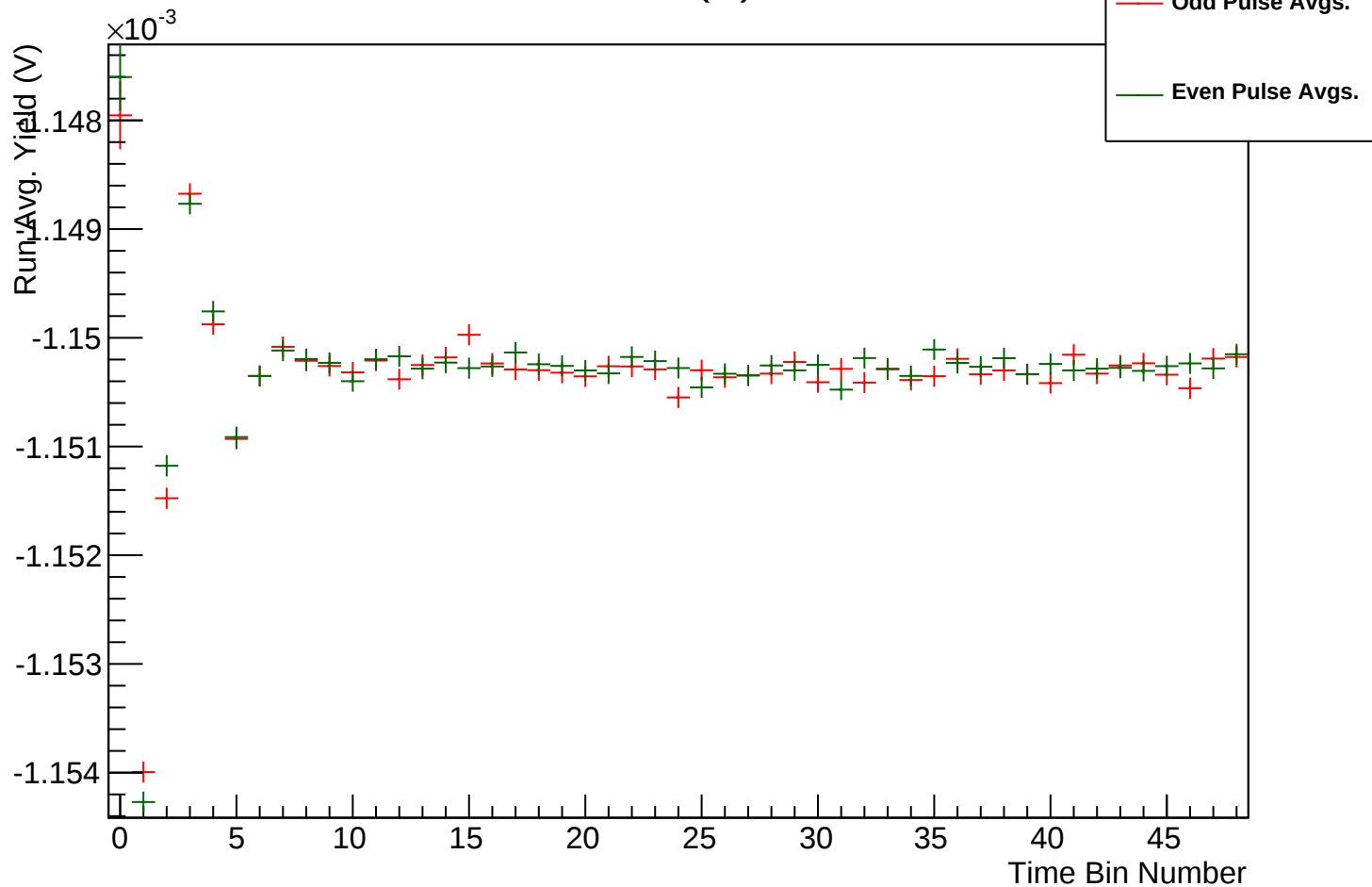
r38314-w3-Yield(V)-OddPulses



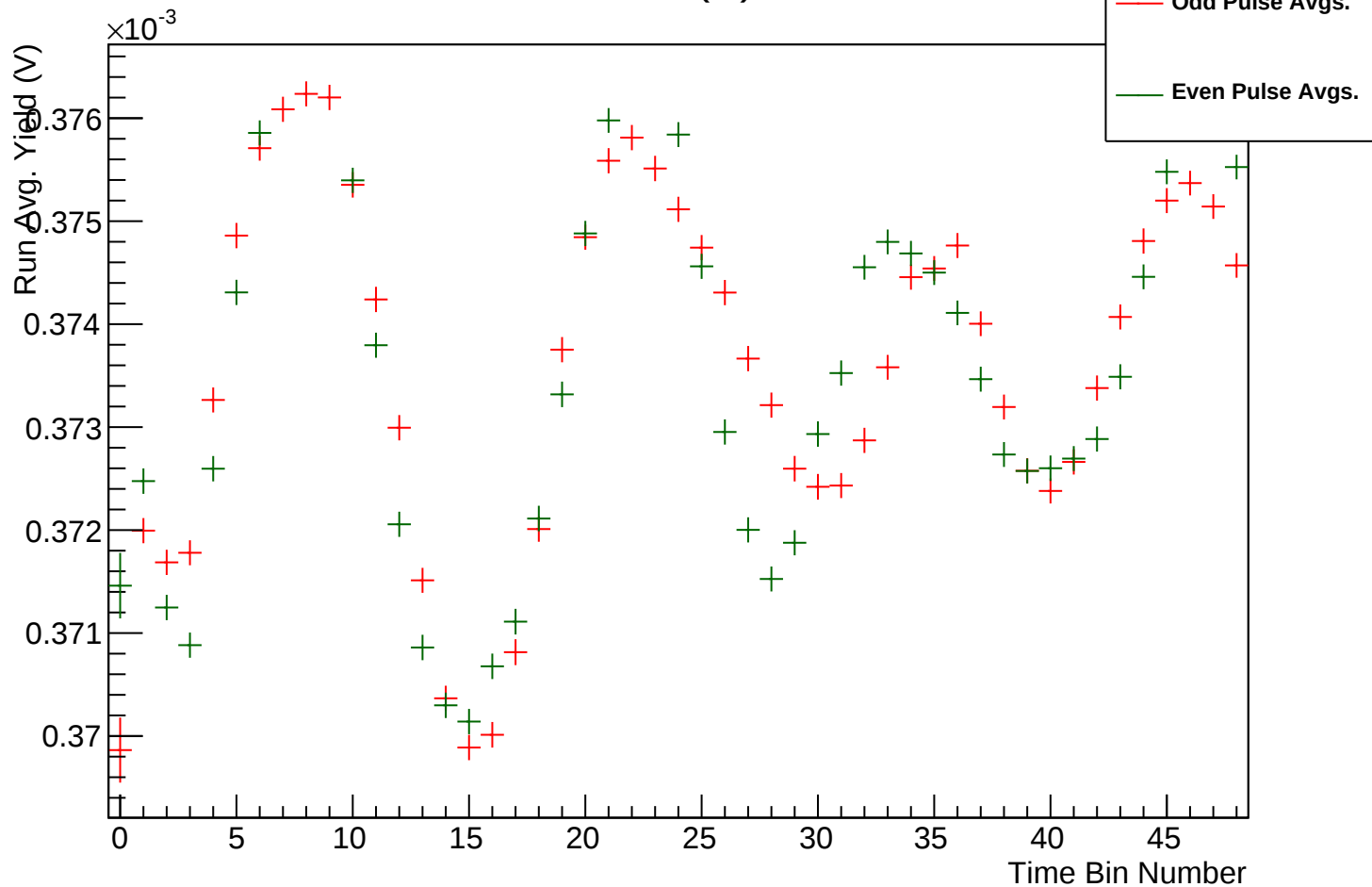
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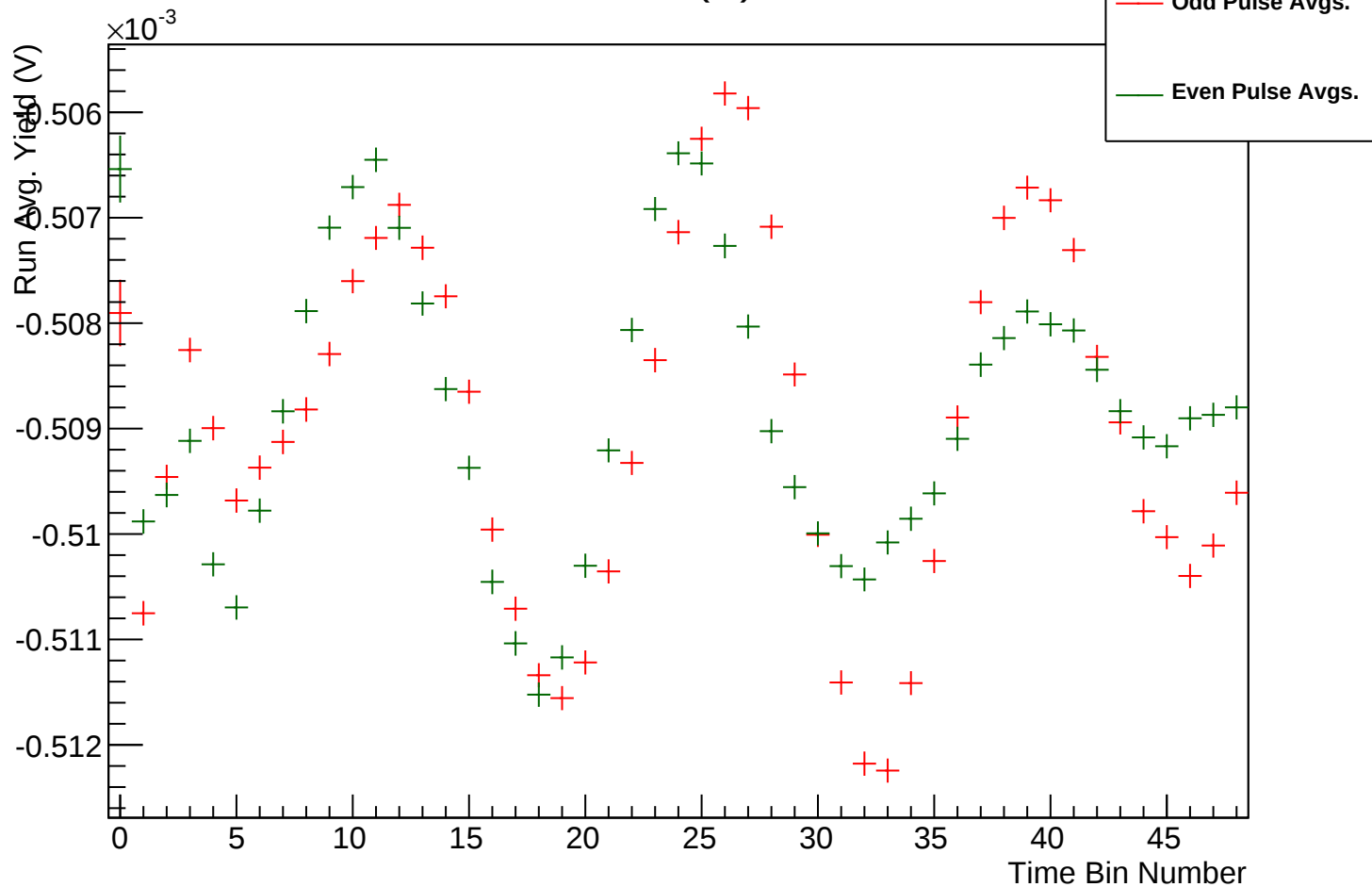
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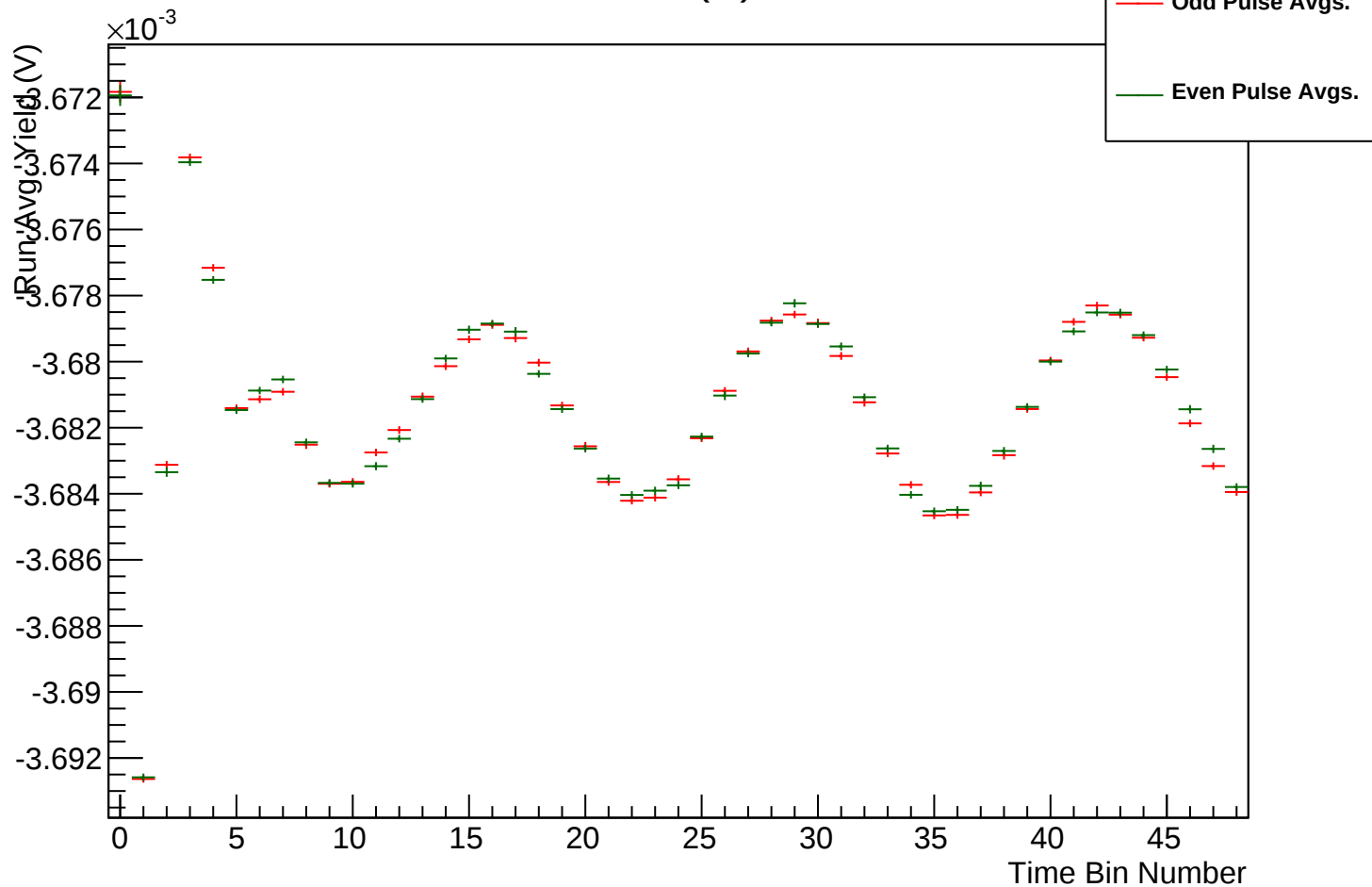
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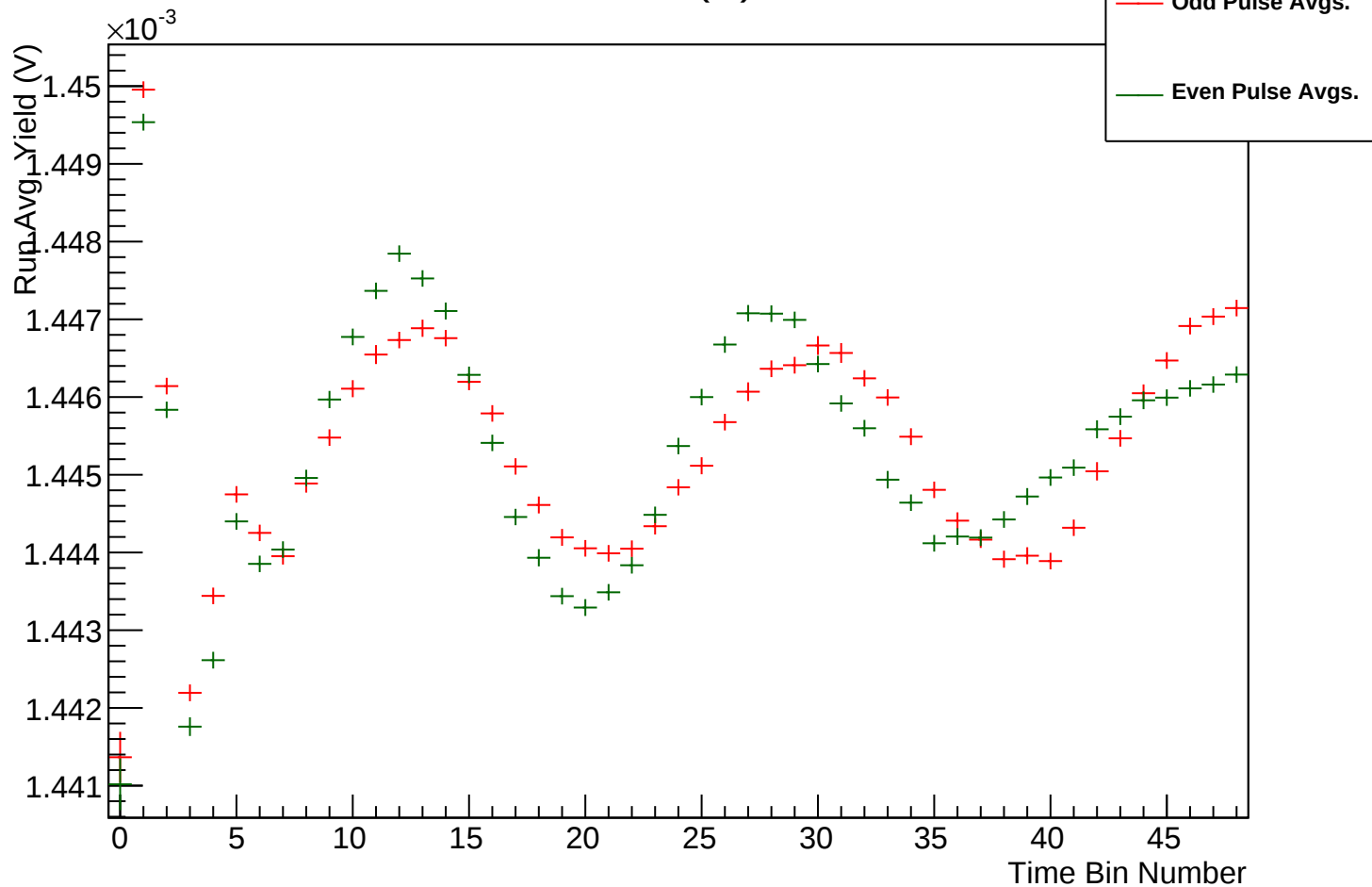
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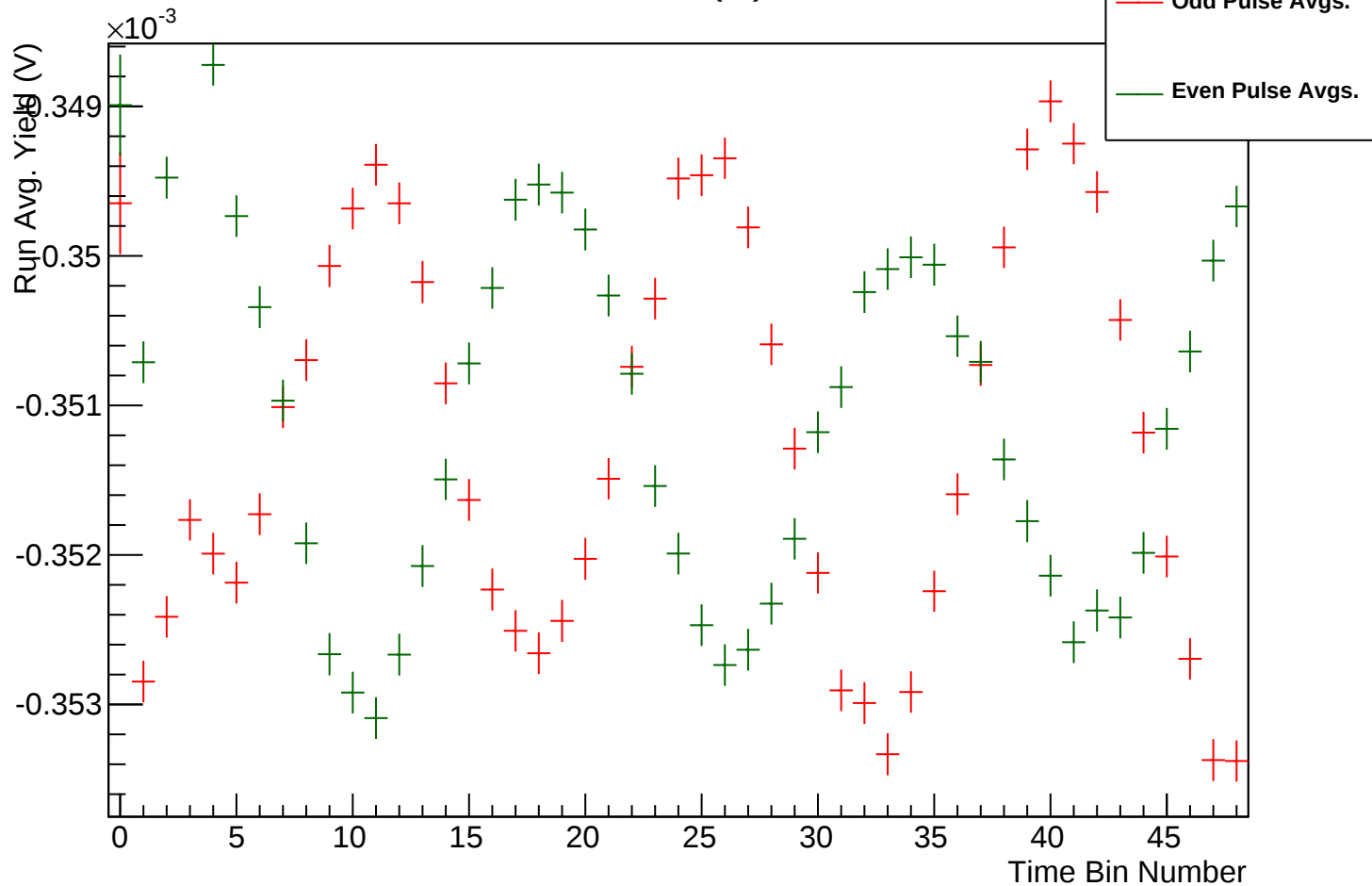
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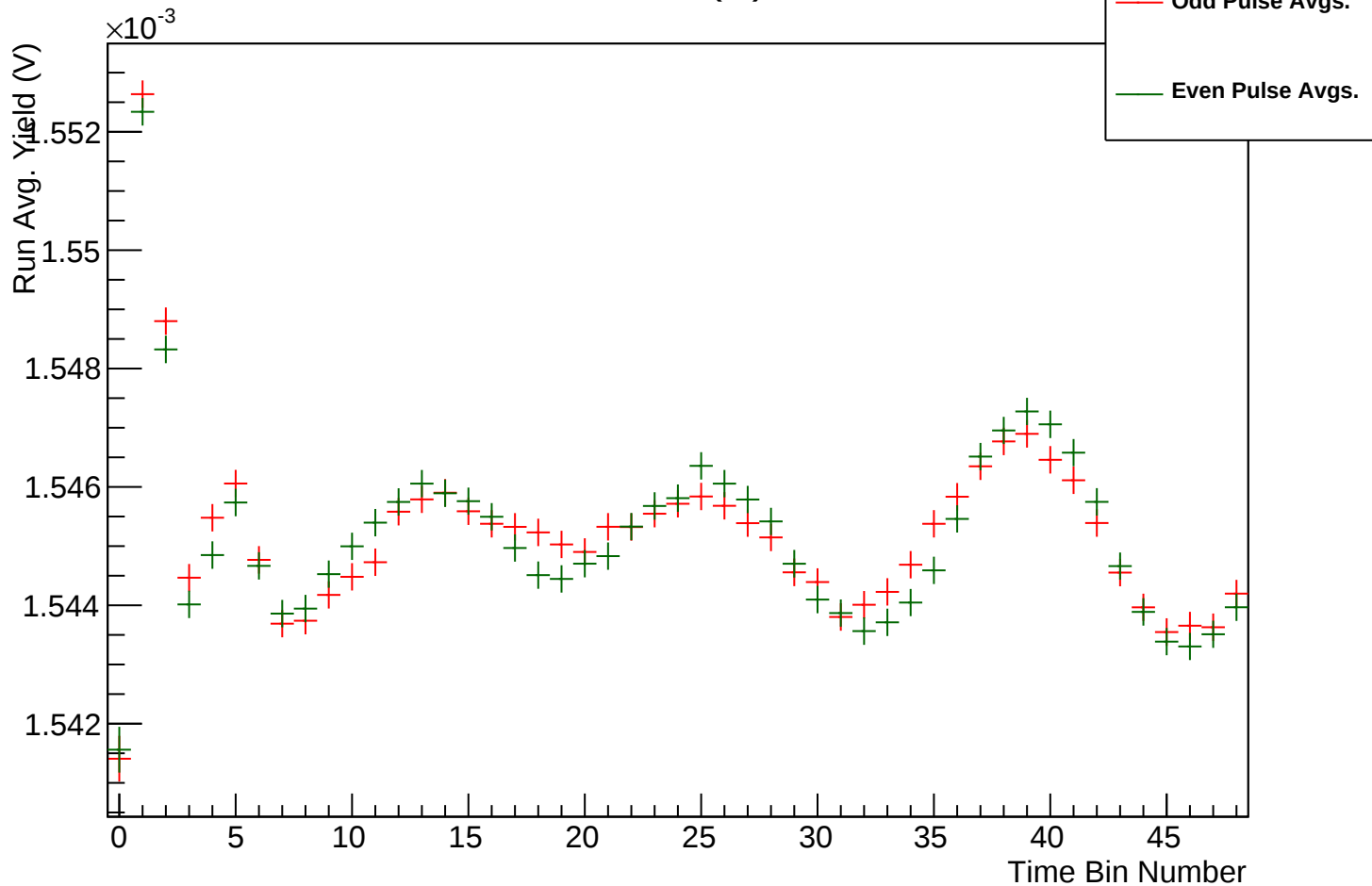
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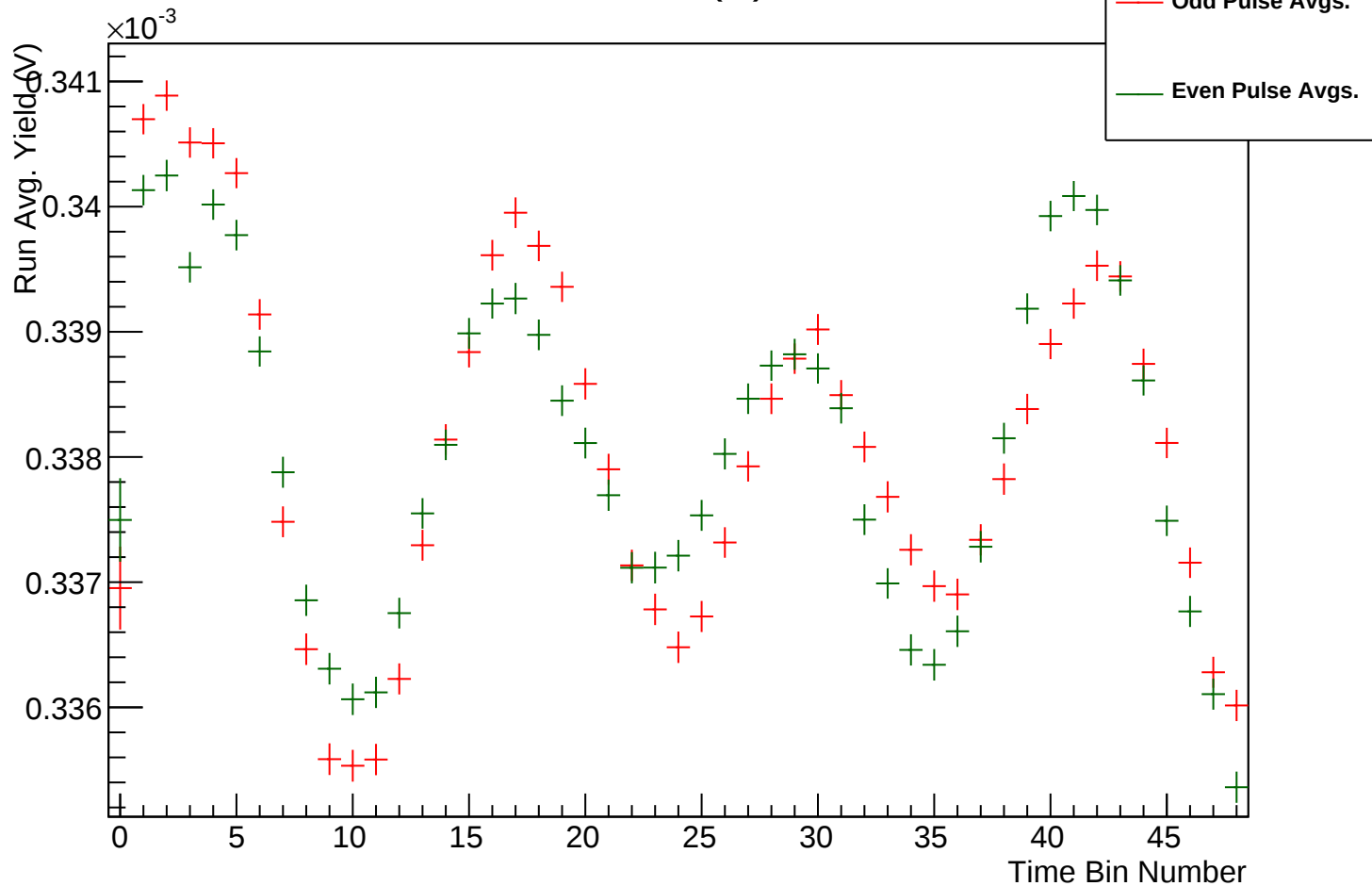
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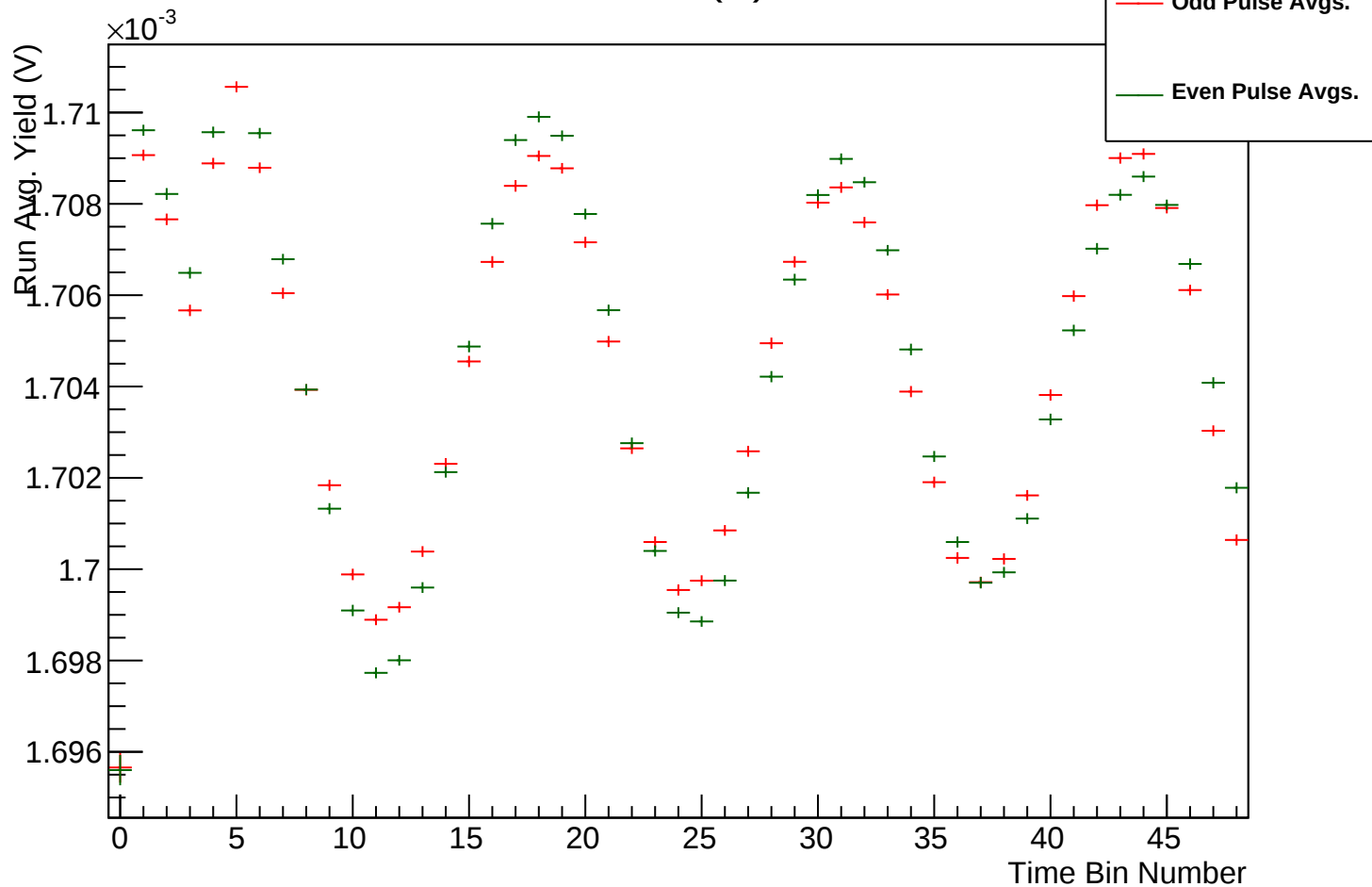
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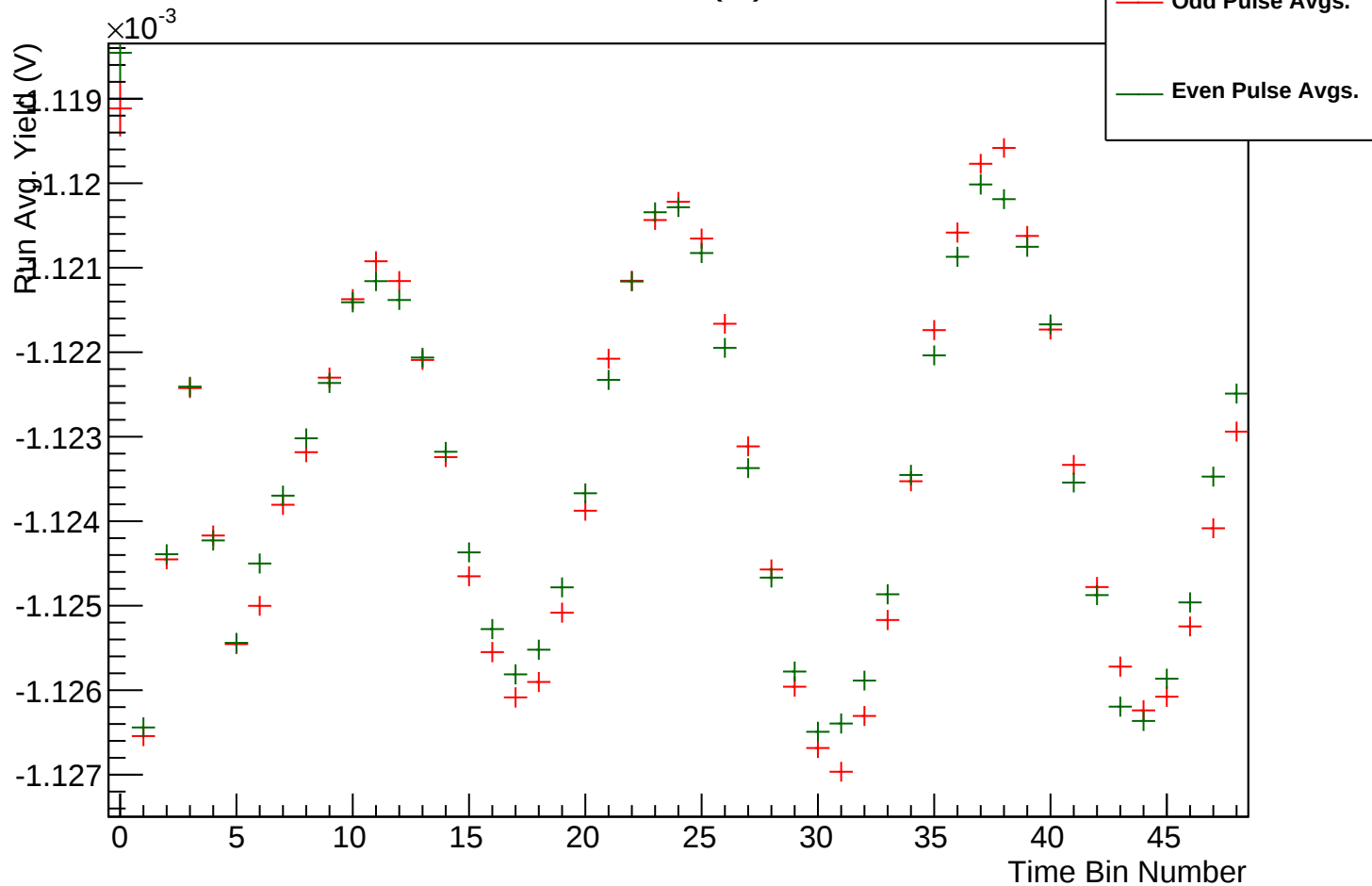
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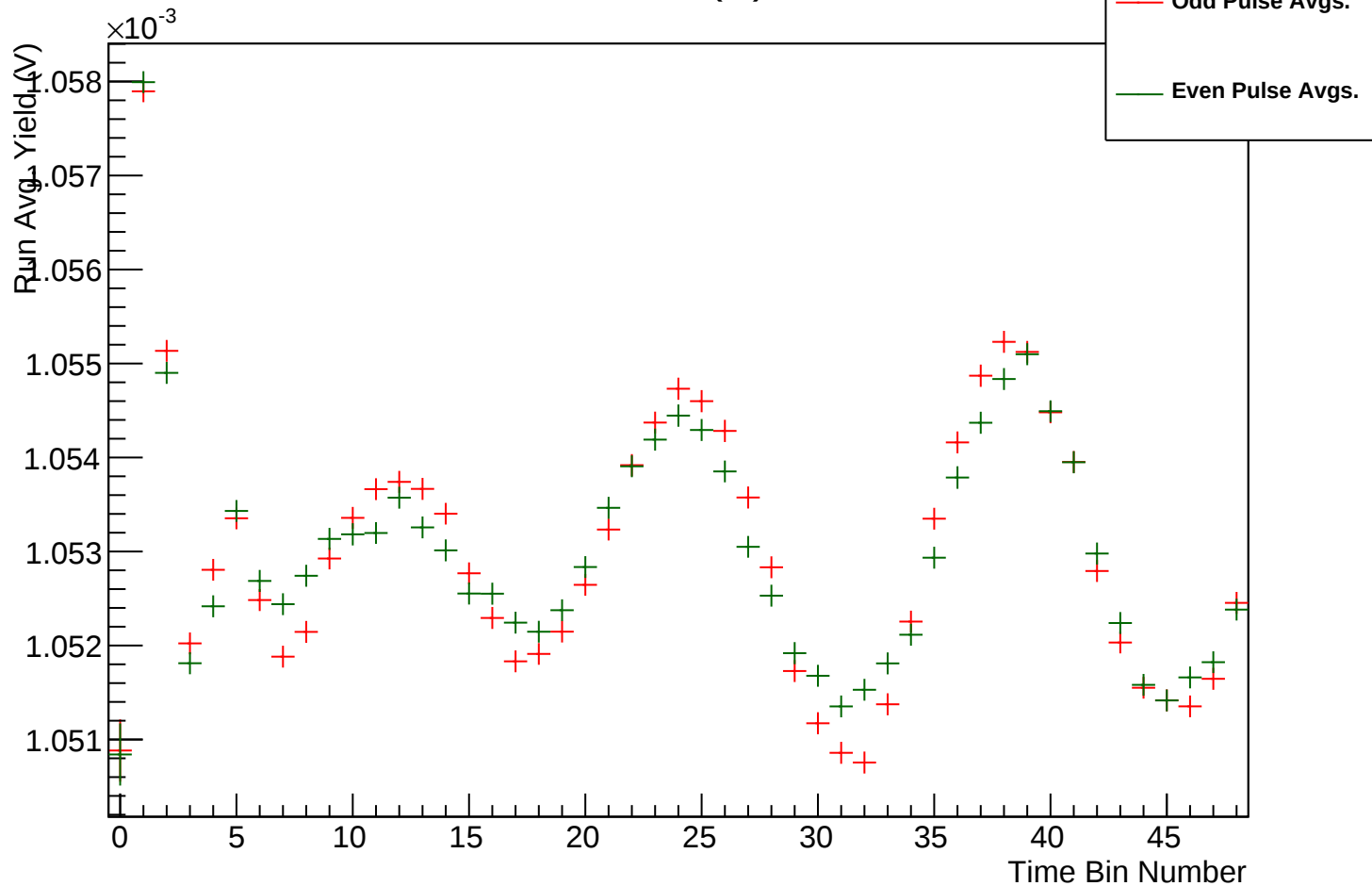
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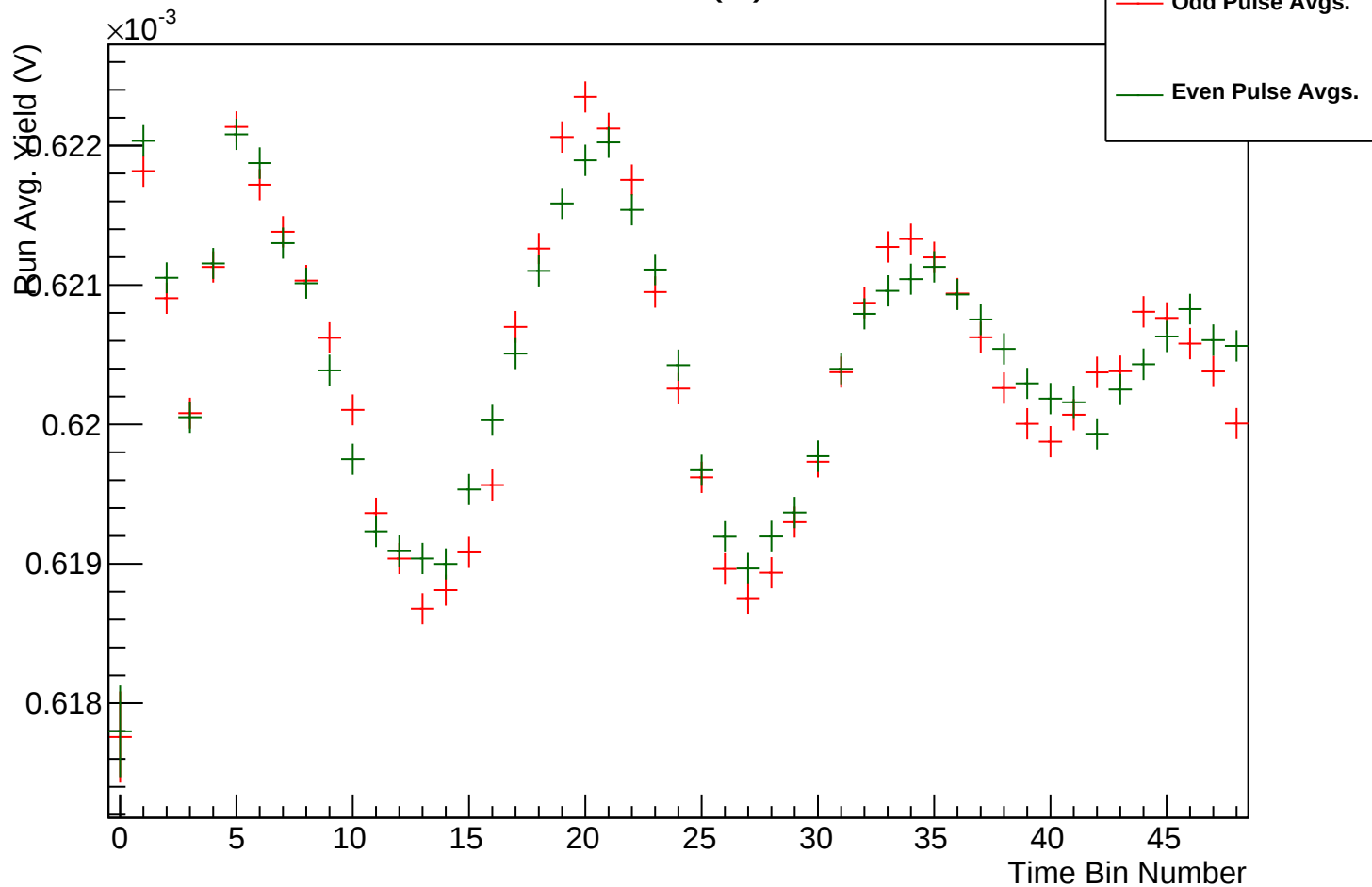
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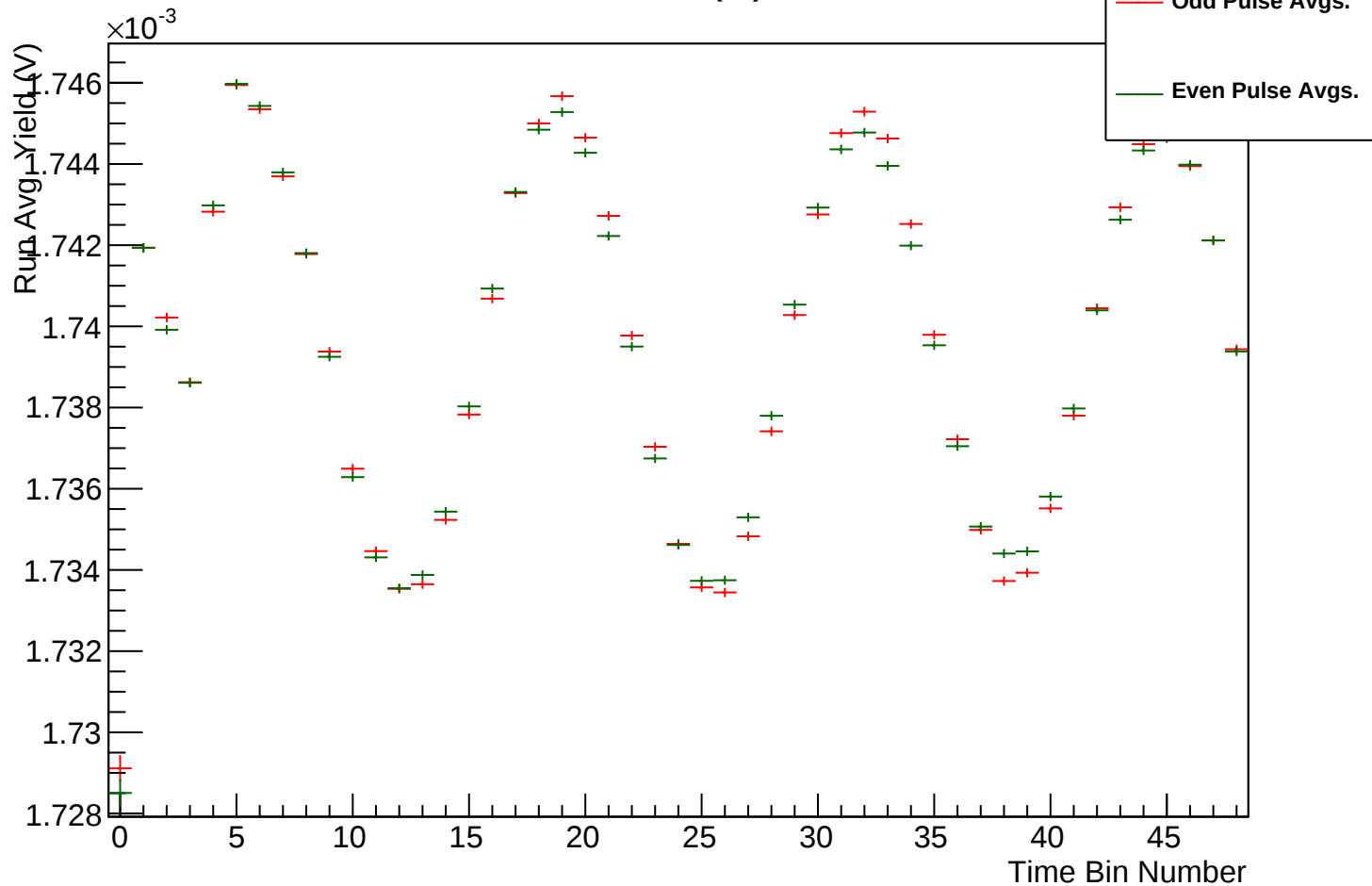
r38314-w15-Yield(V)-OddPulses



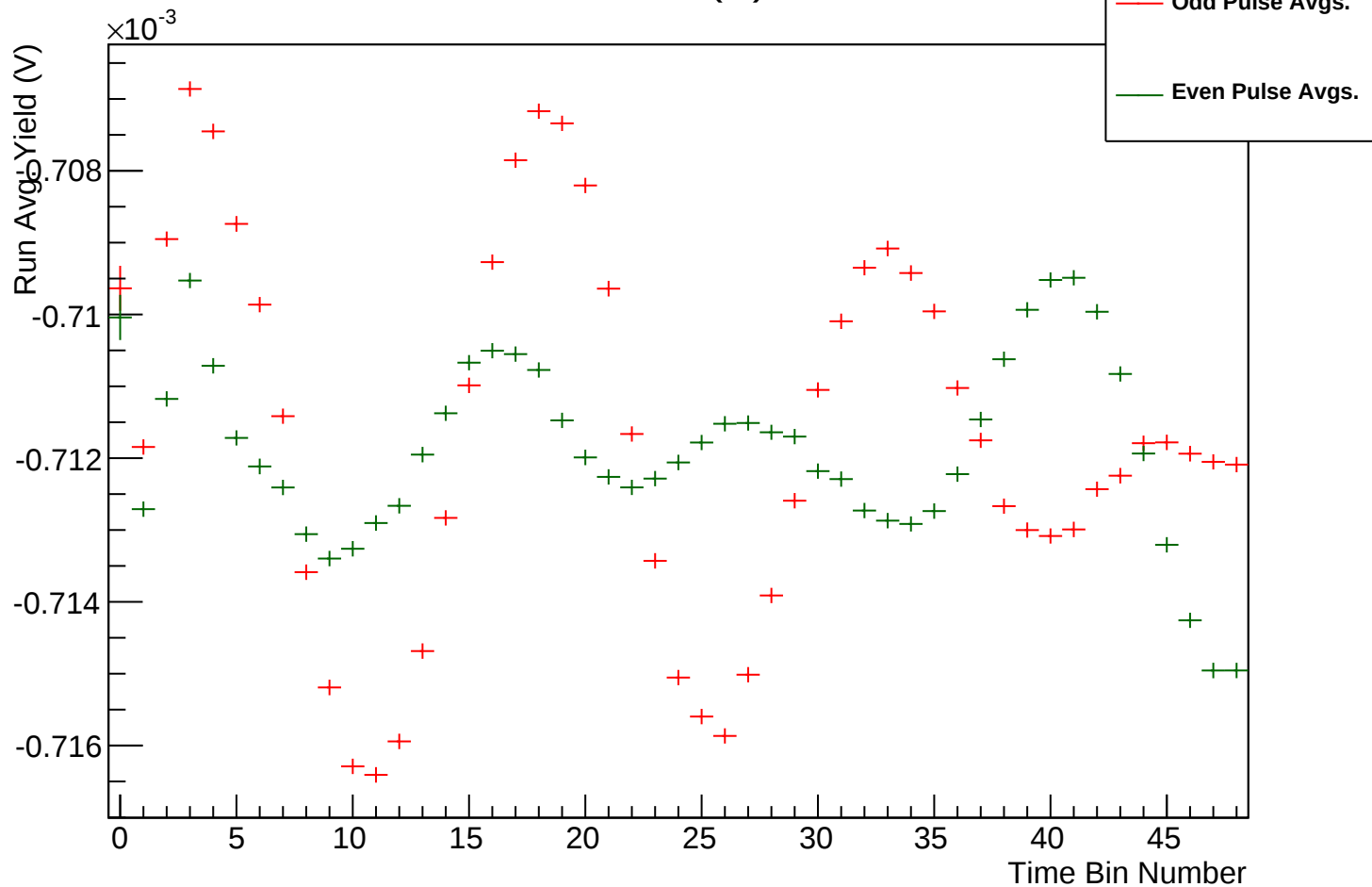
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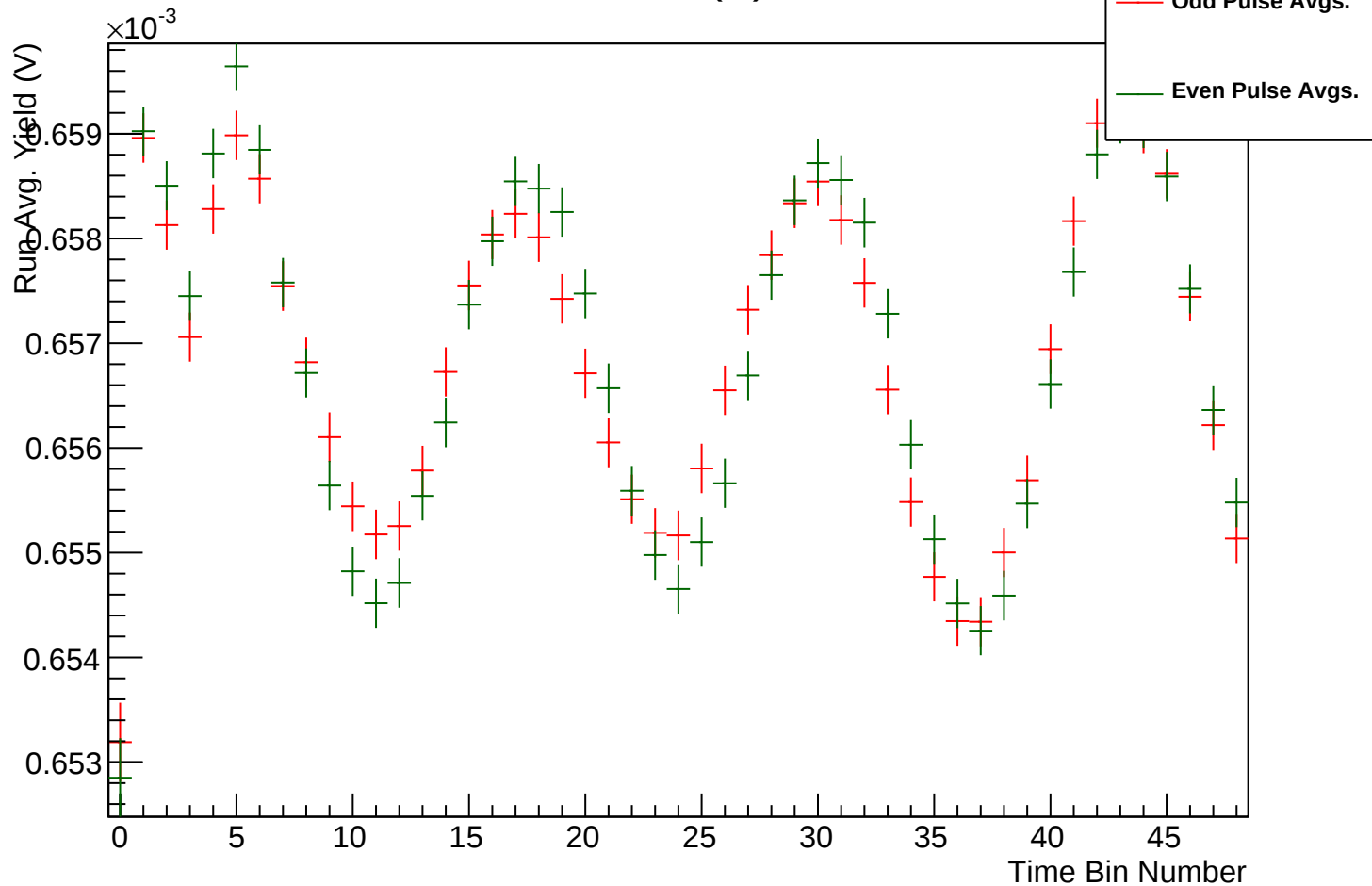
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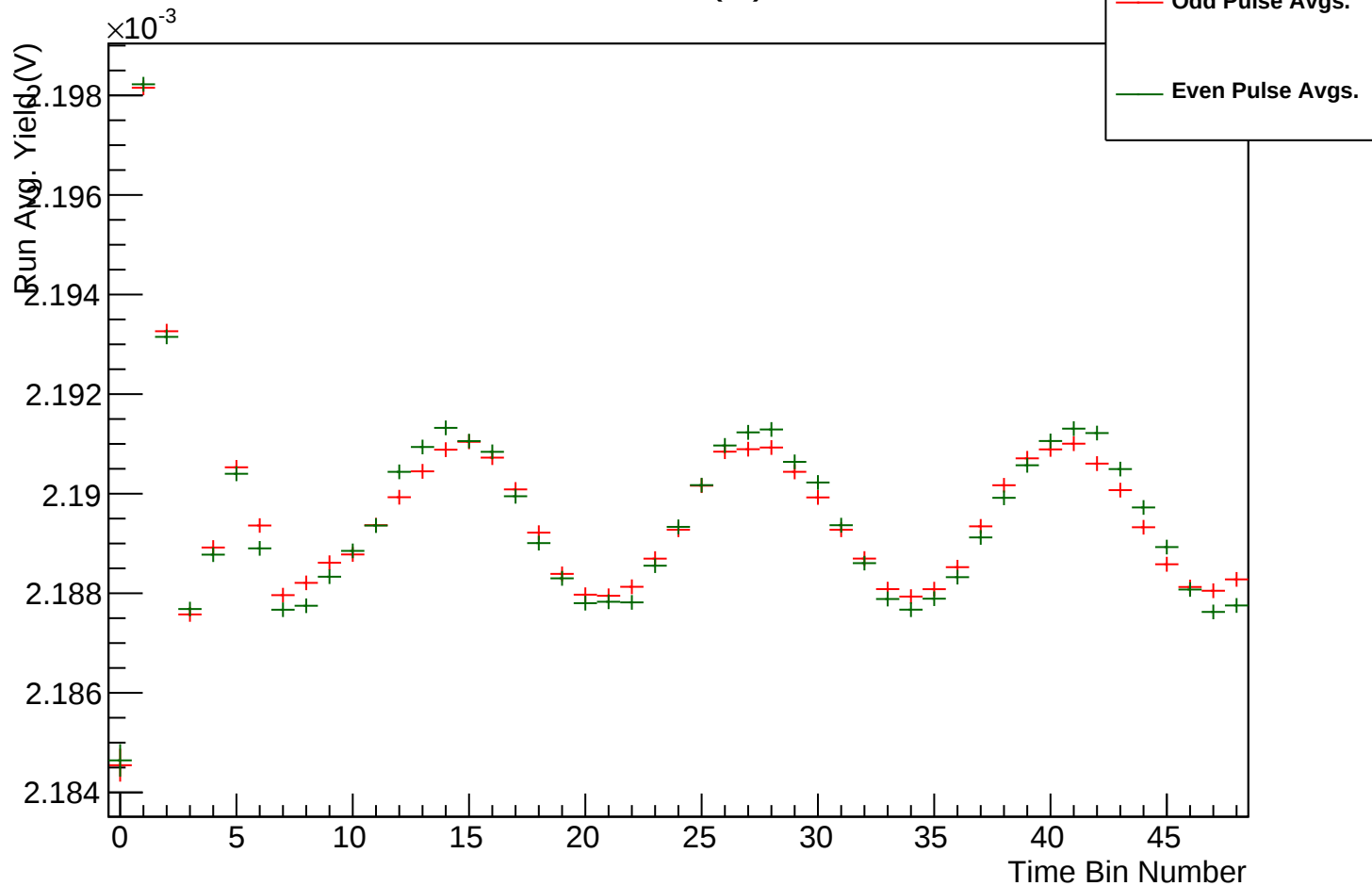
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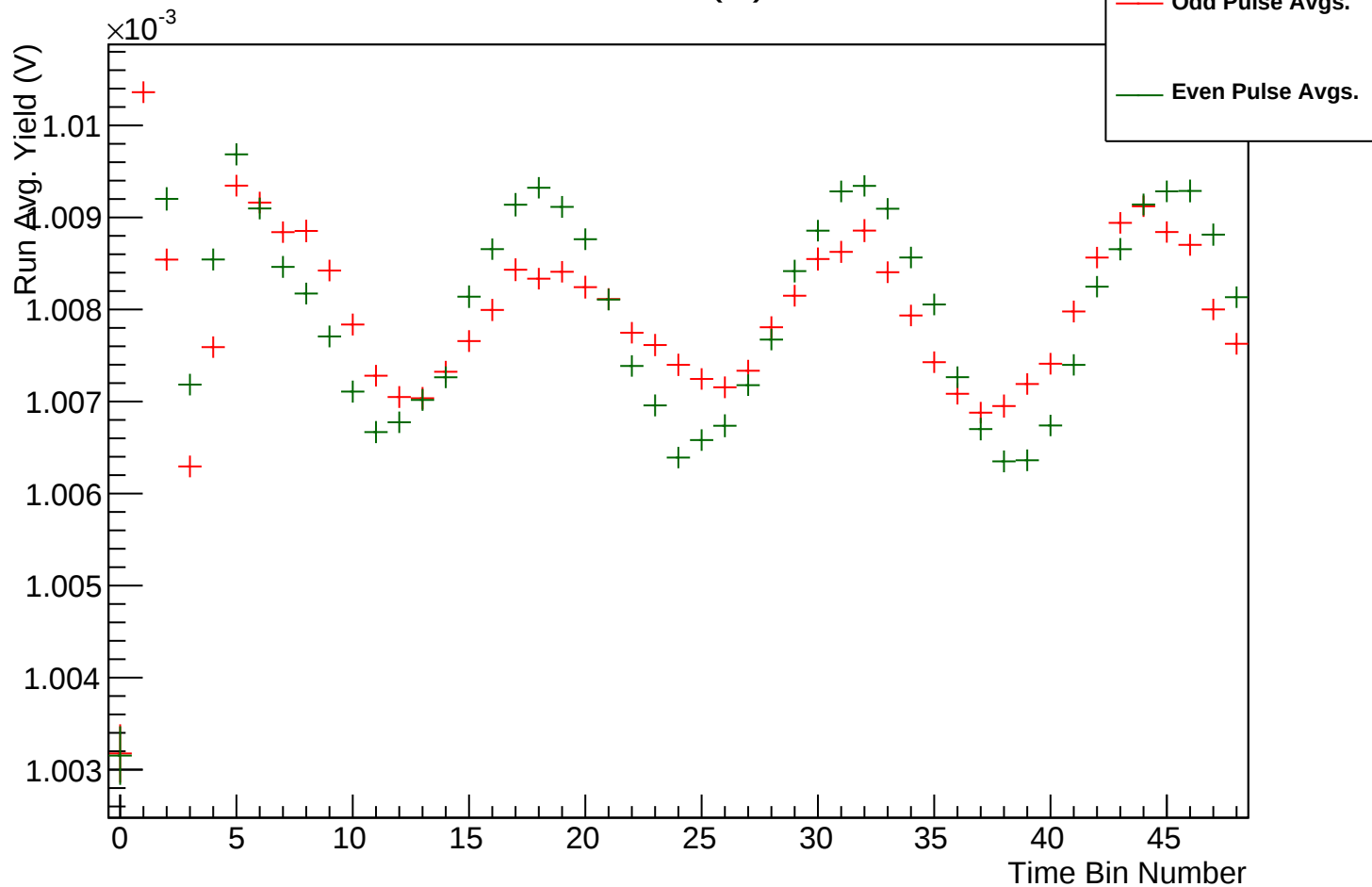
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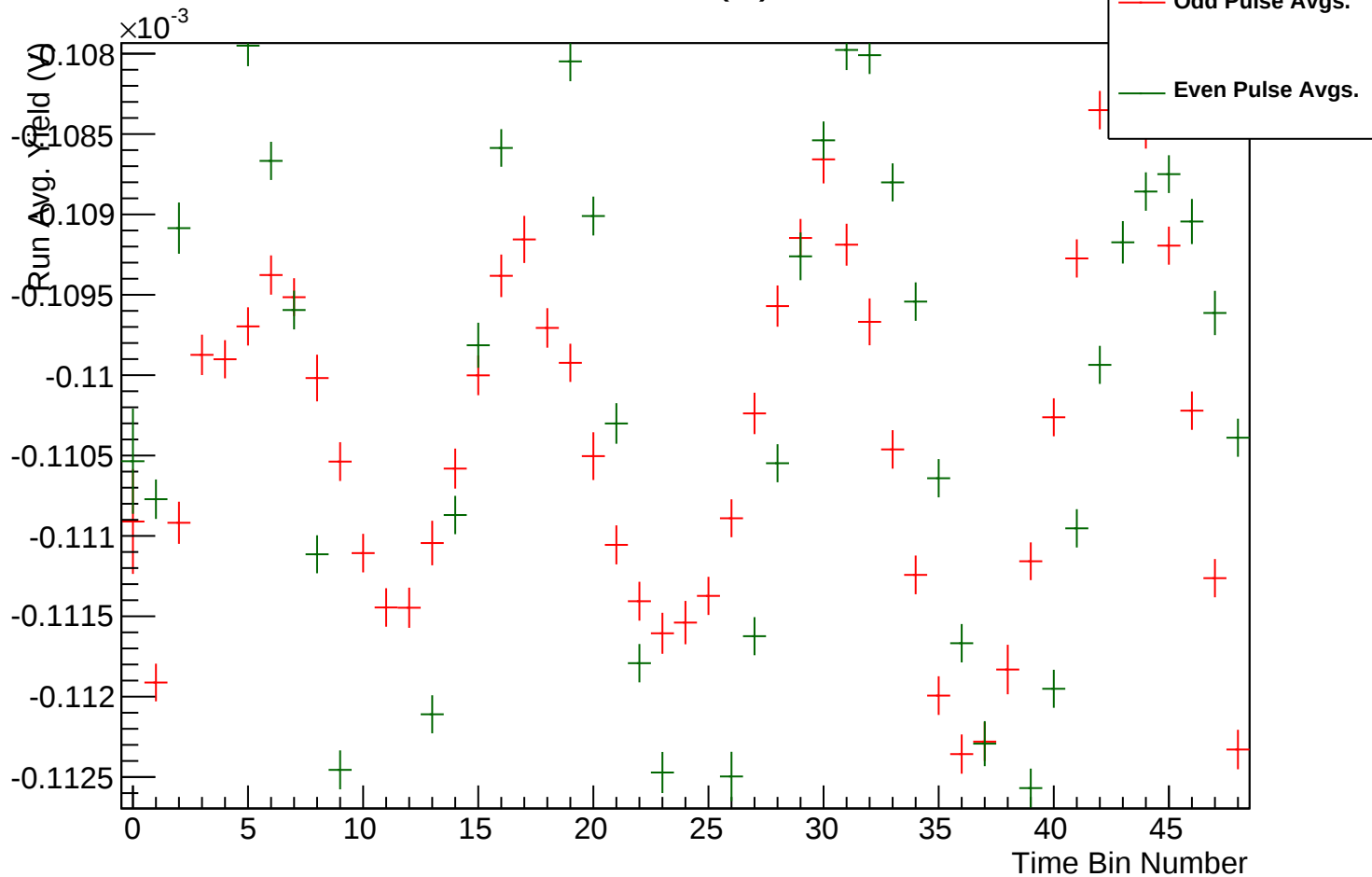
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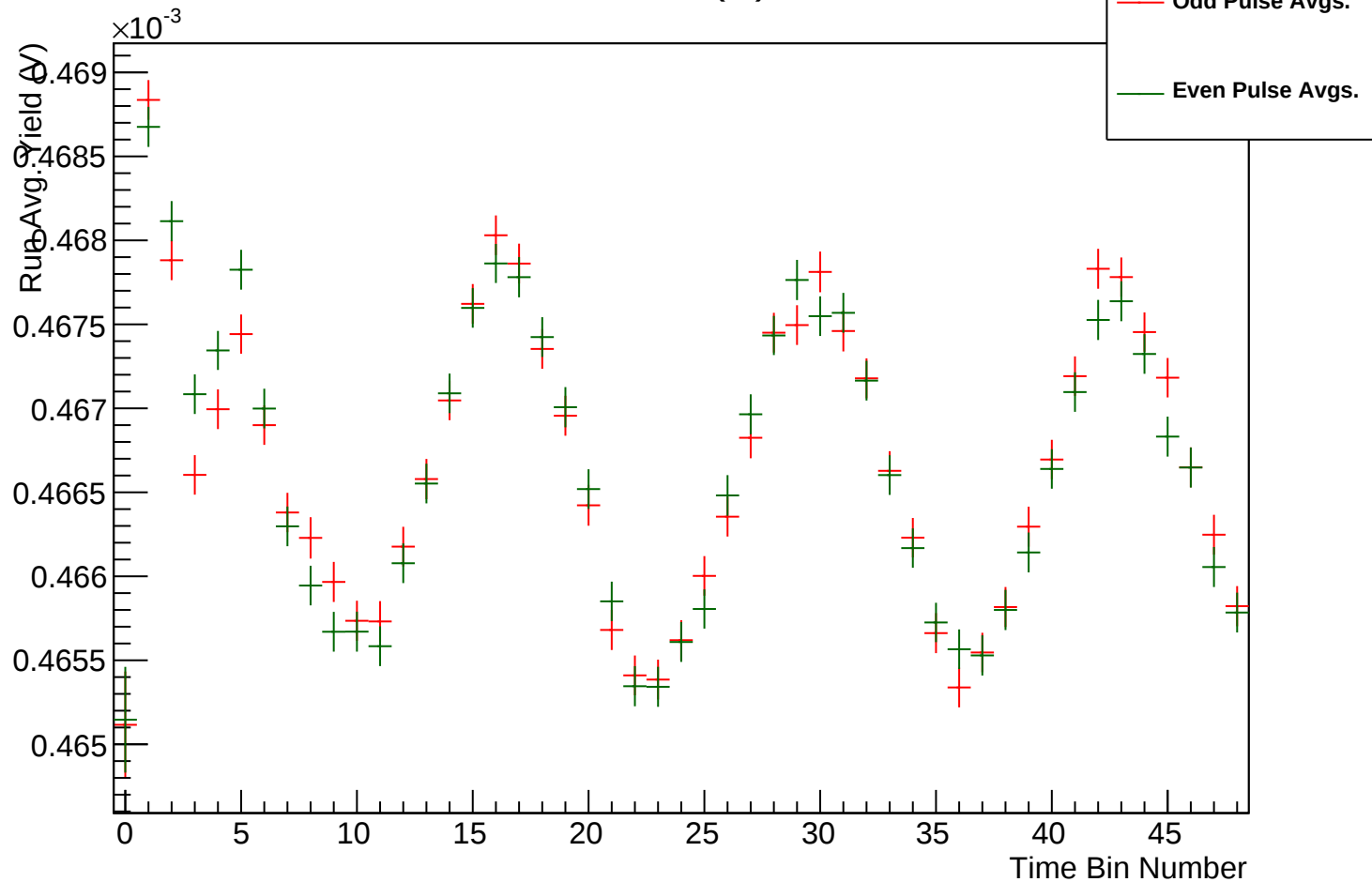
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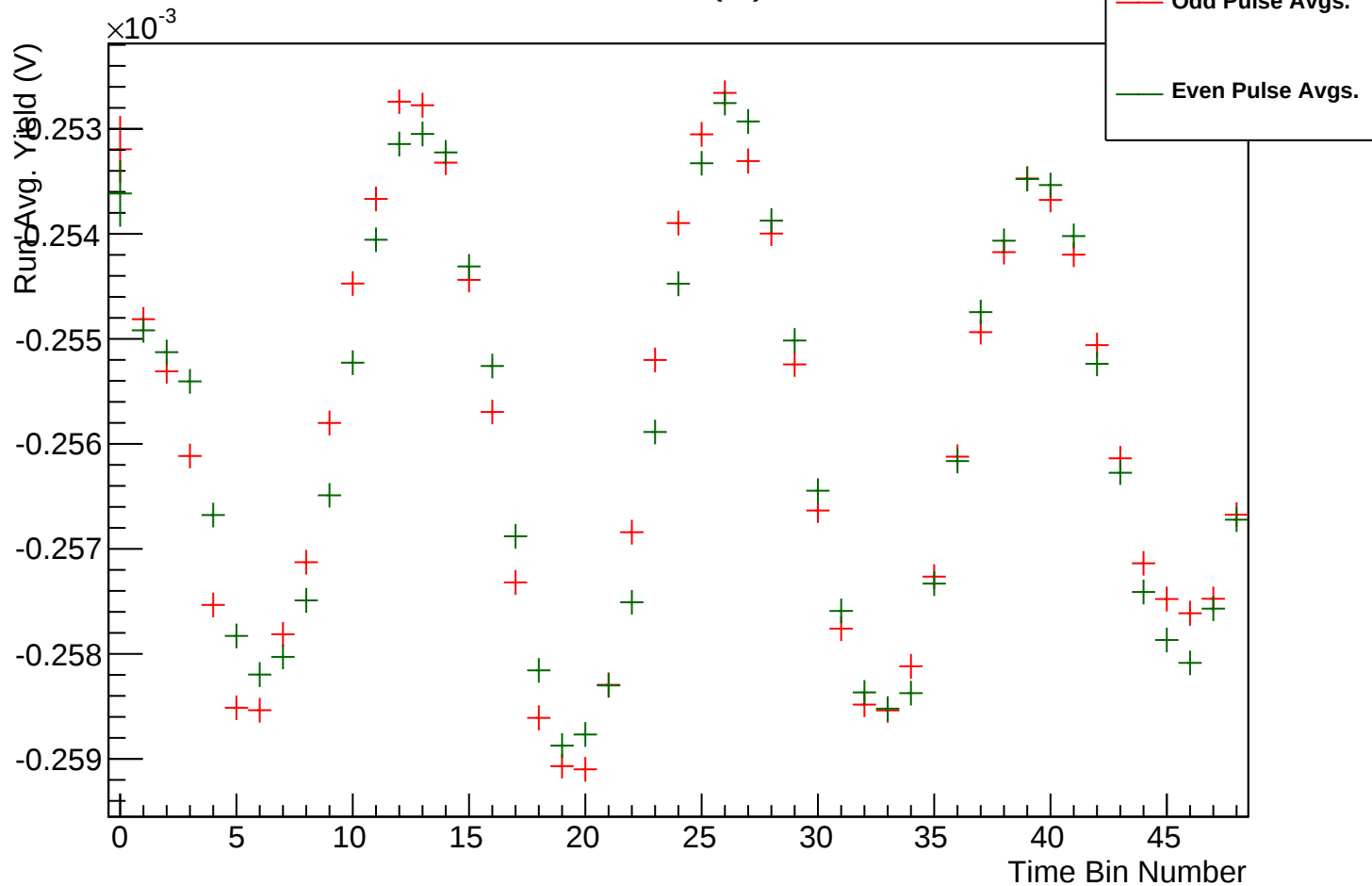
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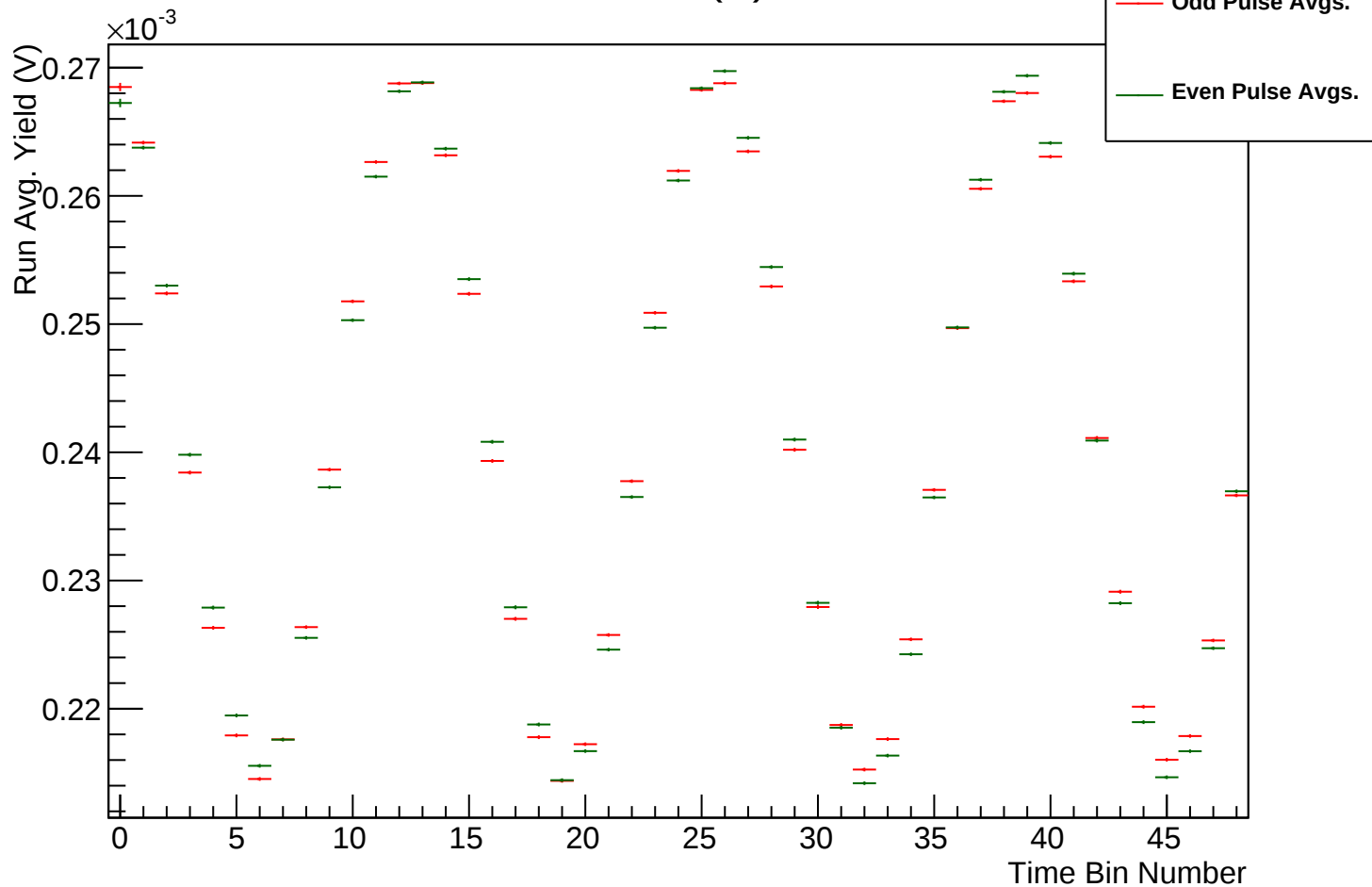
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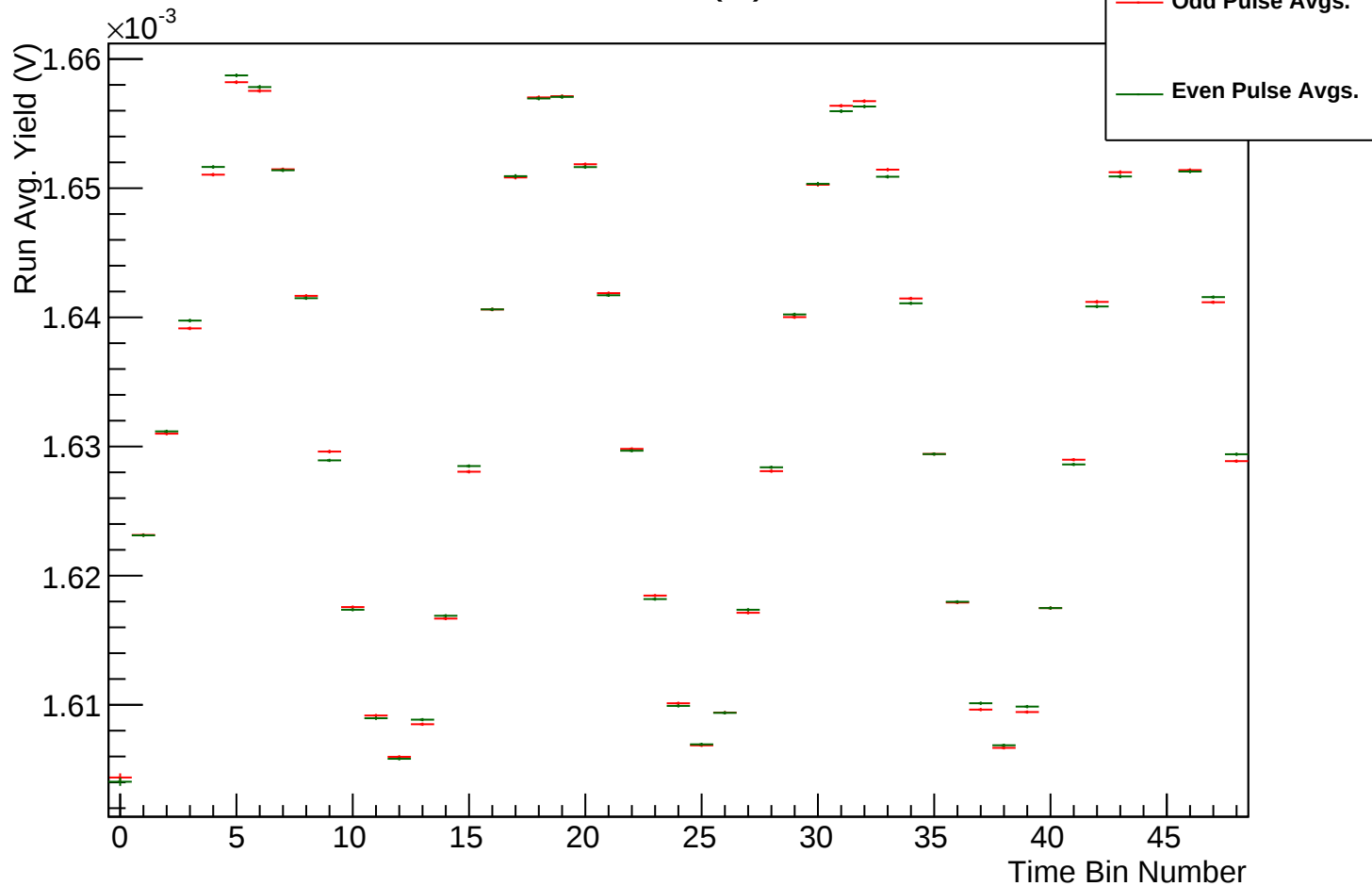
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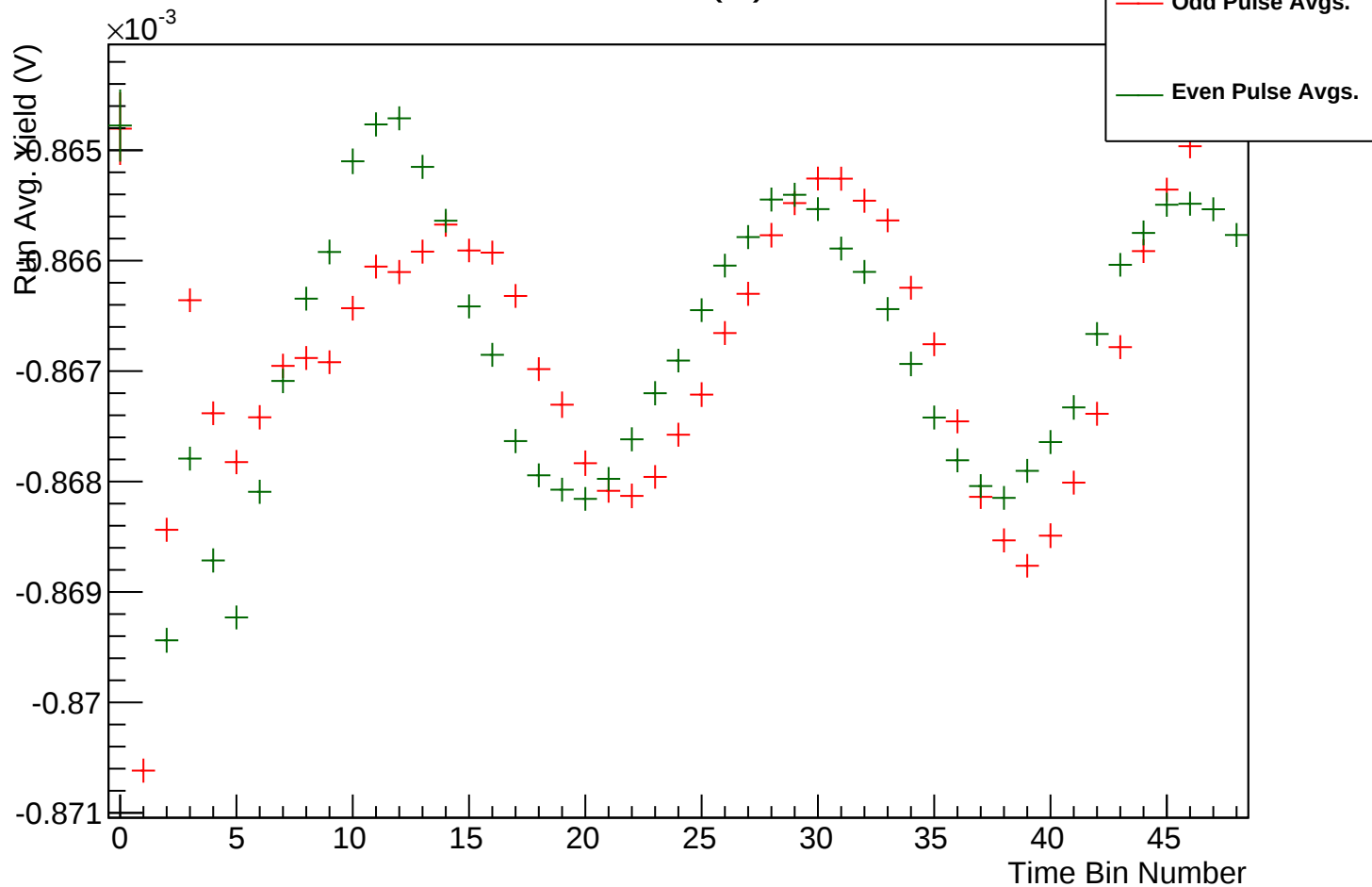
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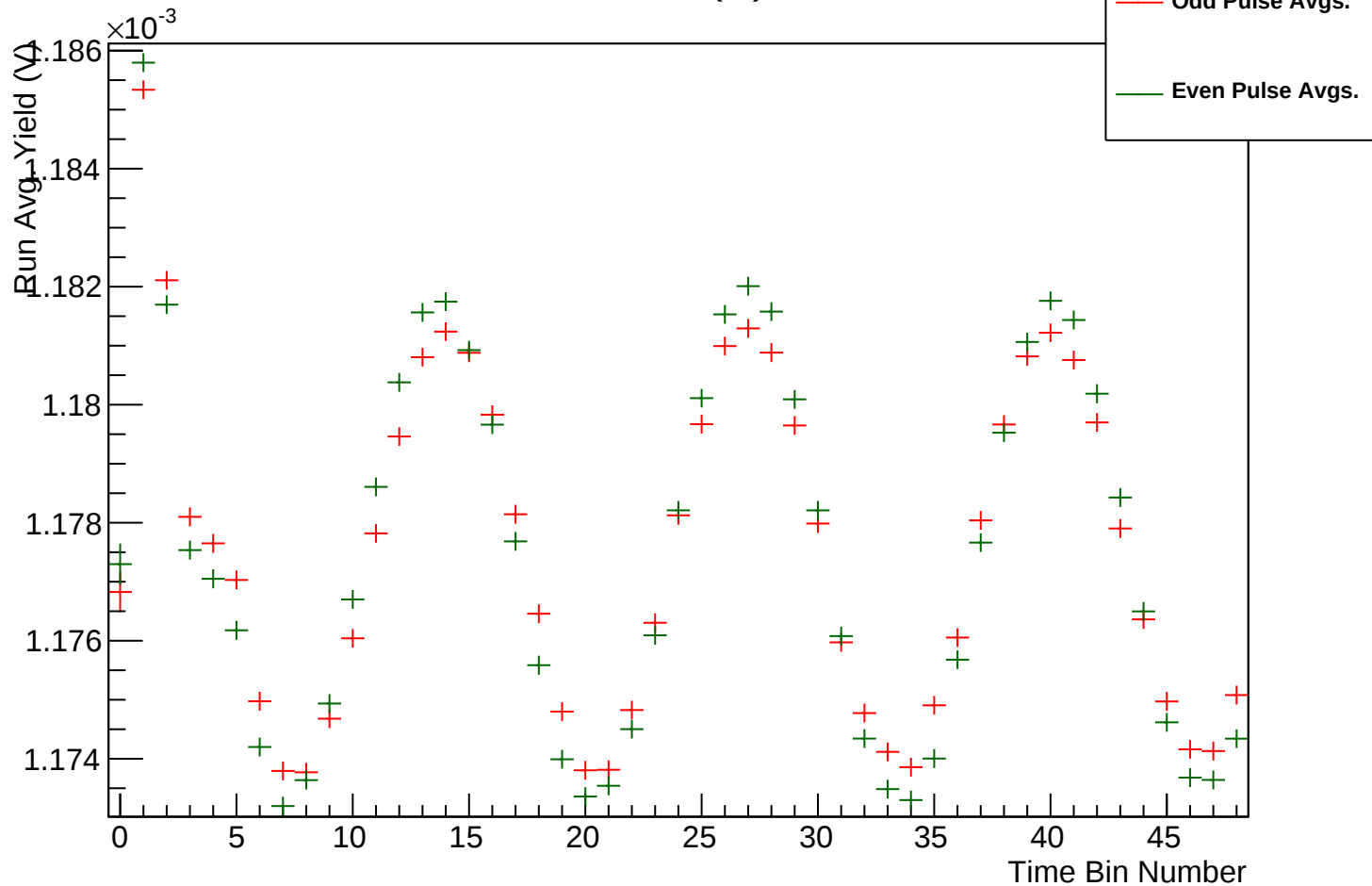
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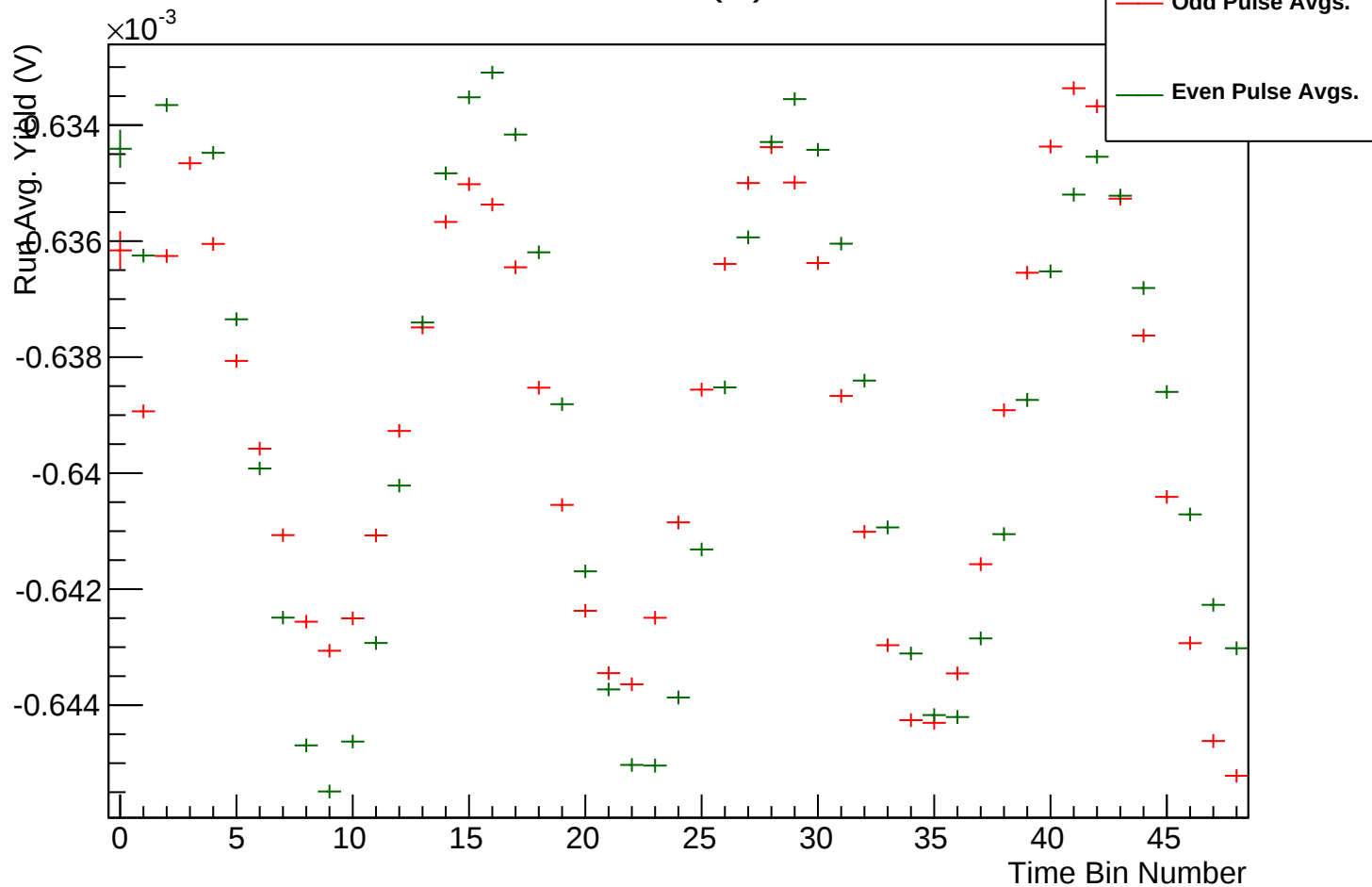
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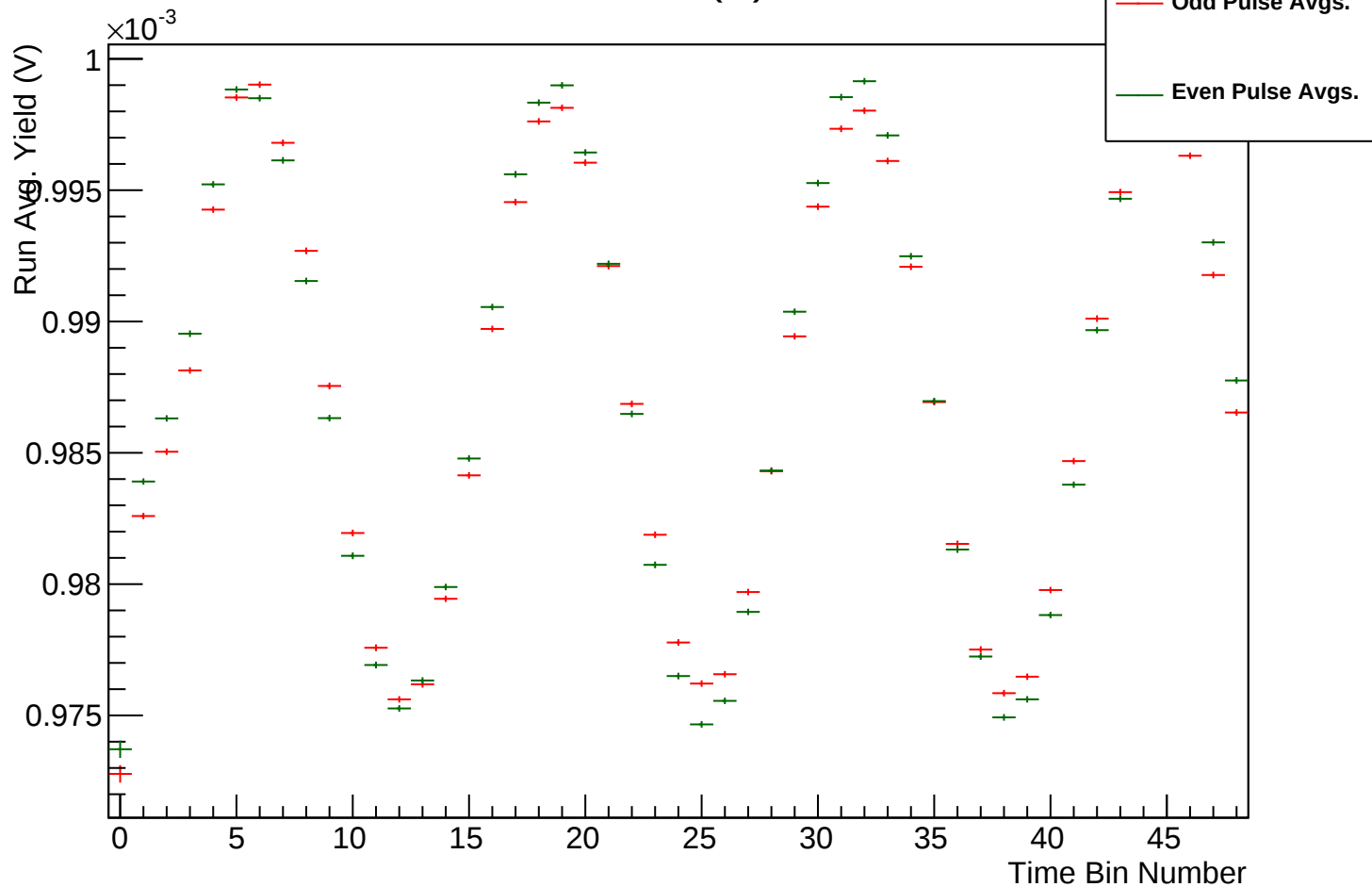
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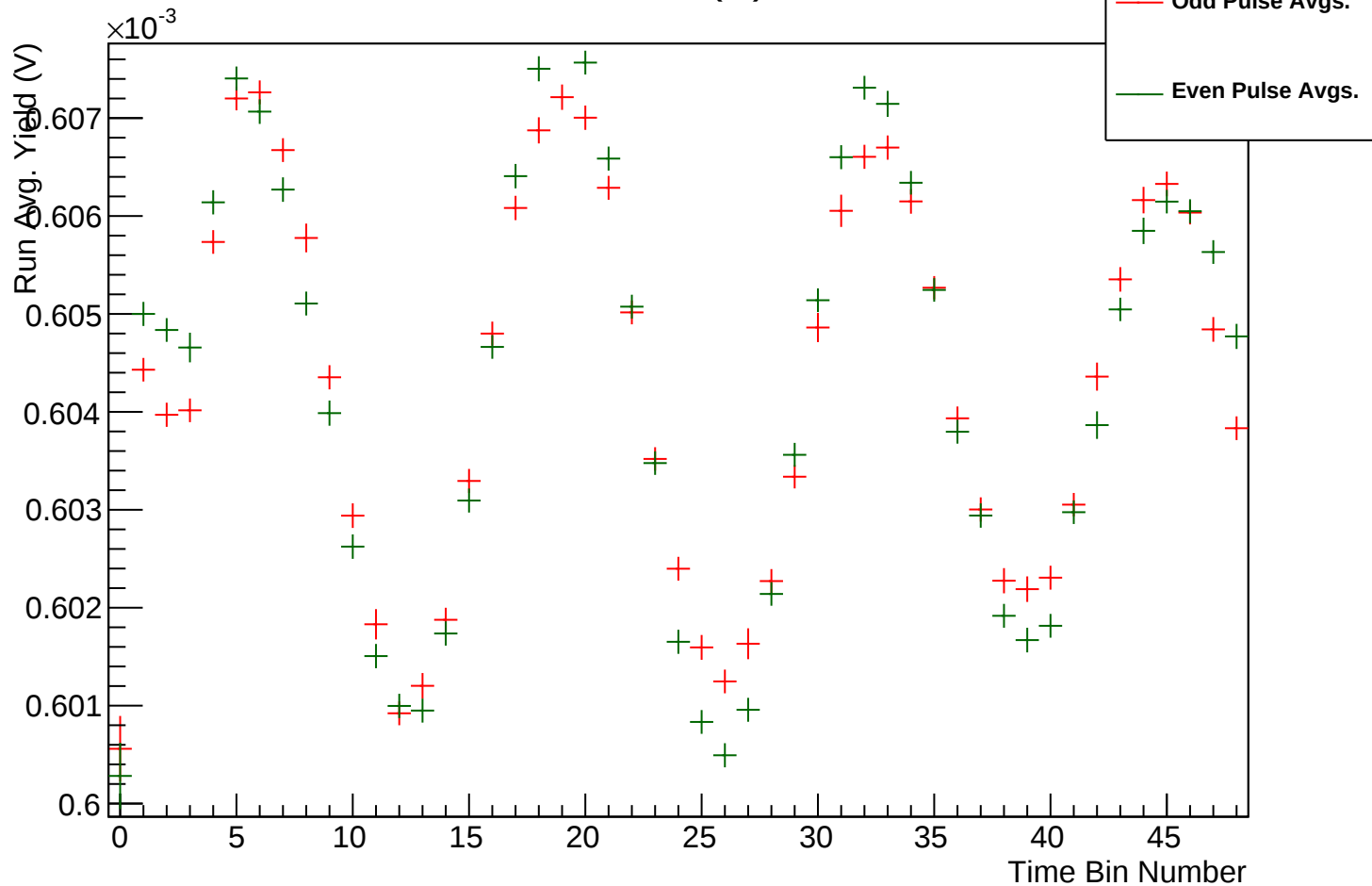
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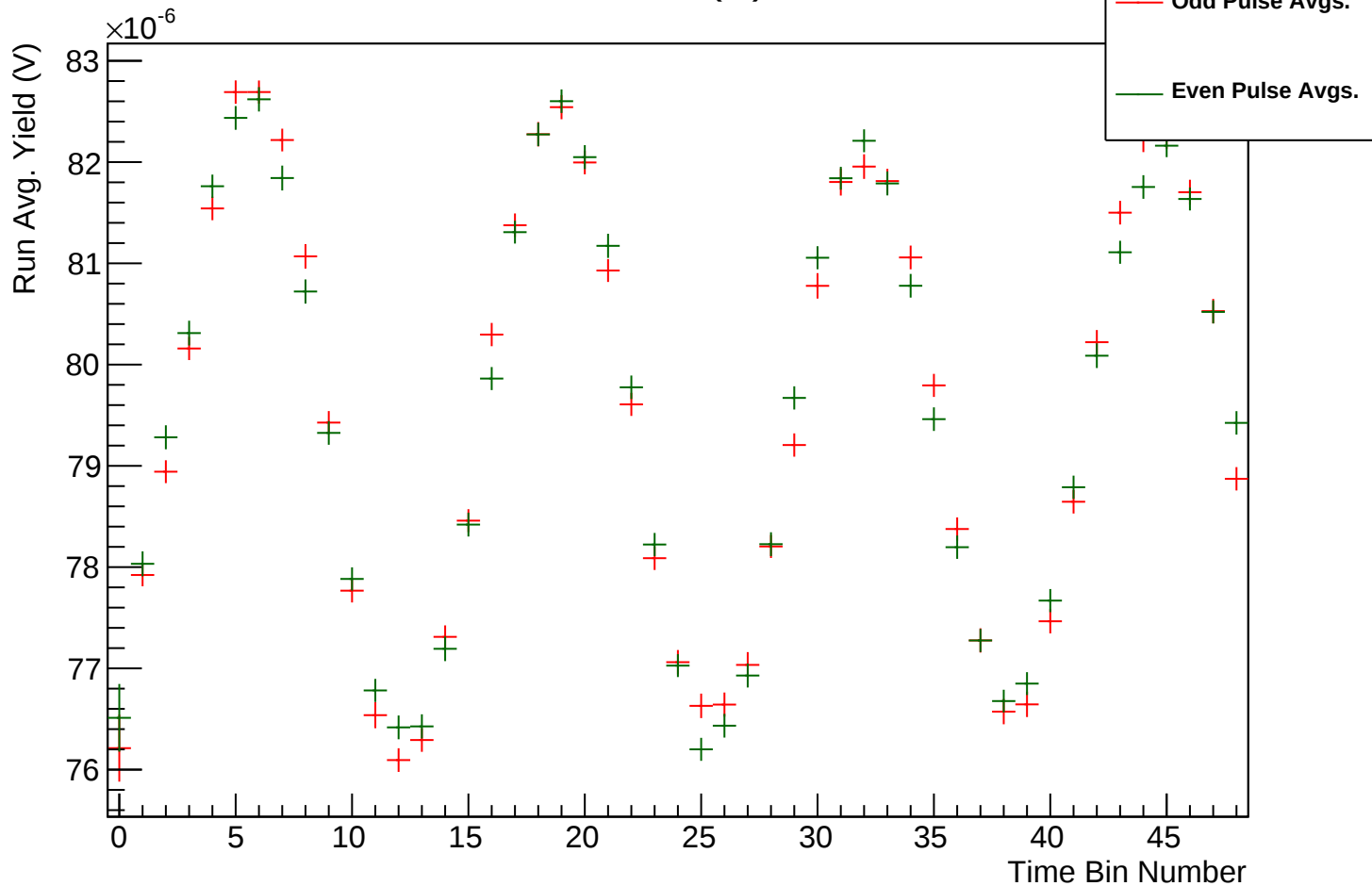
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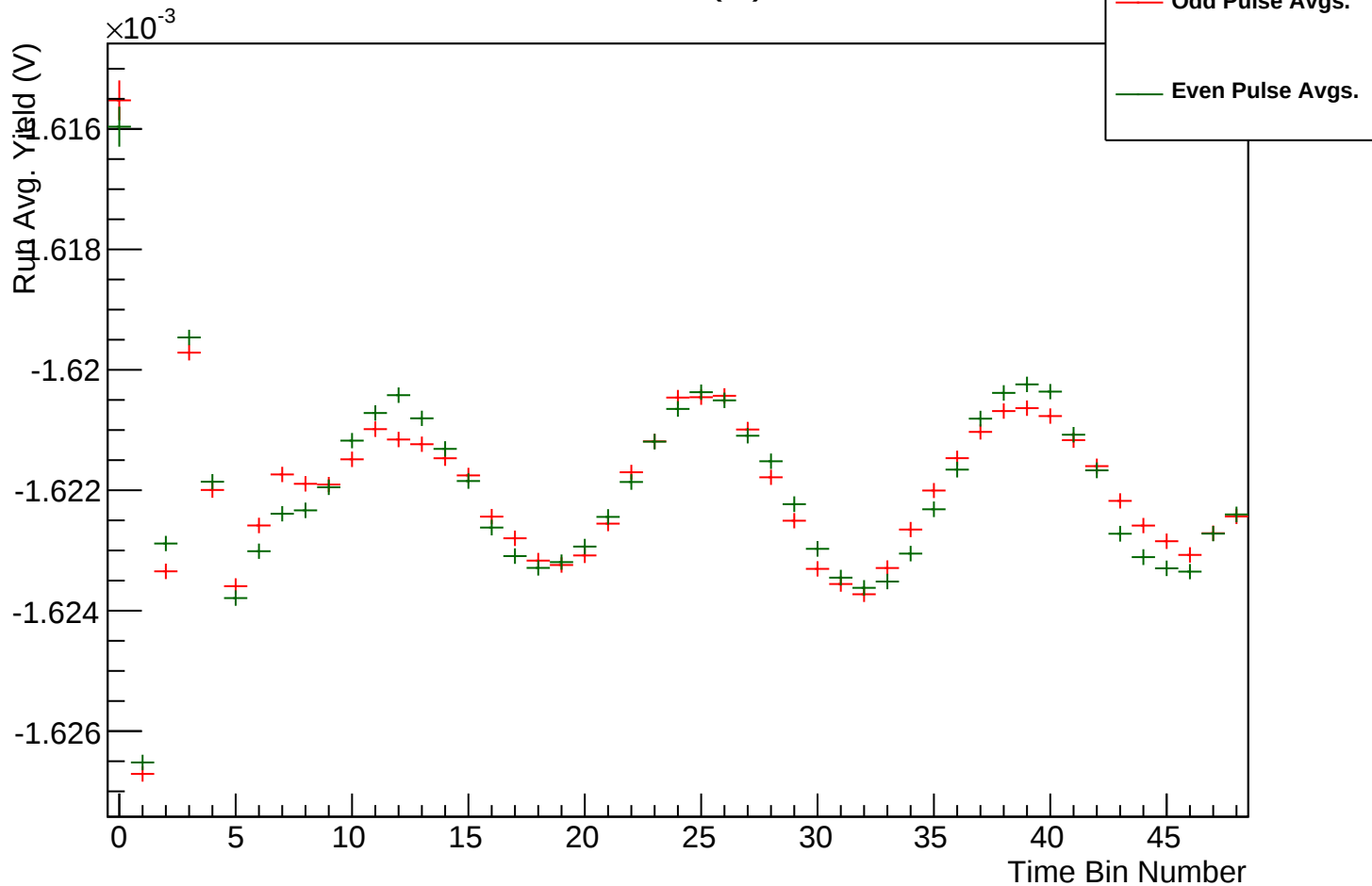
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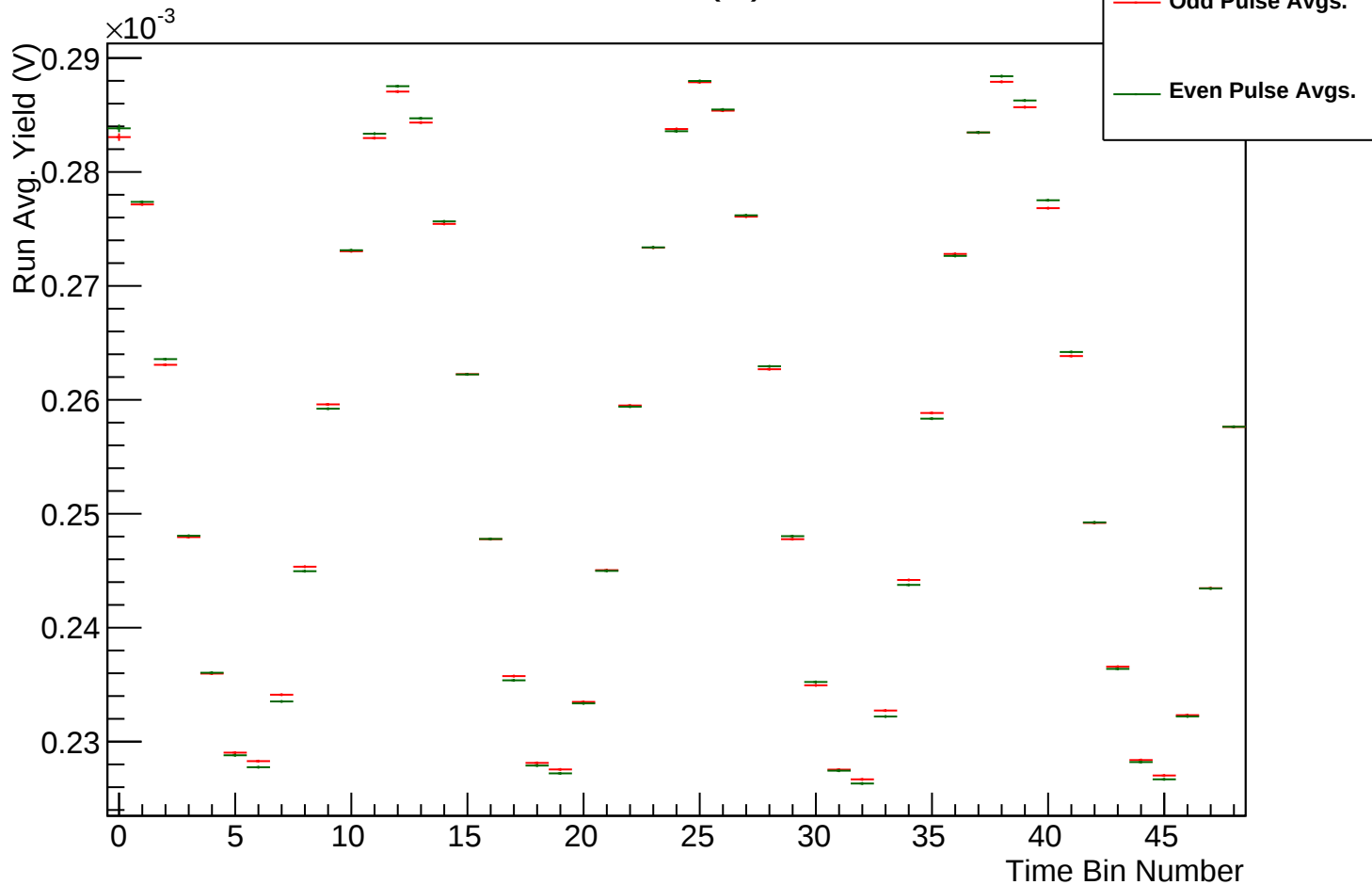
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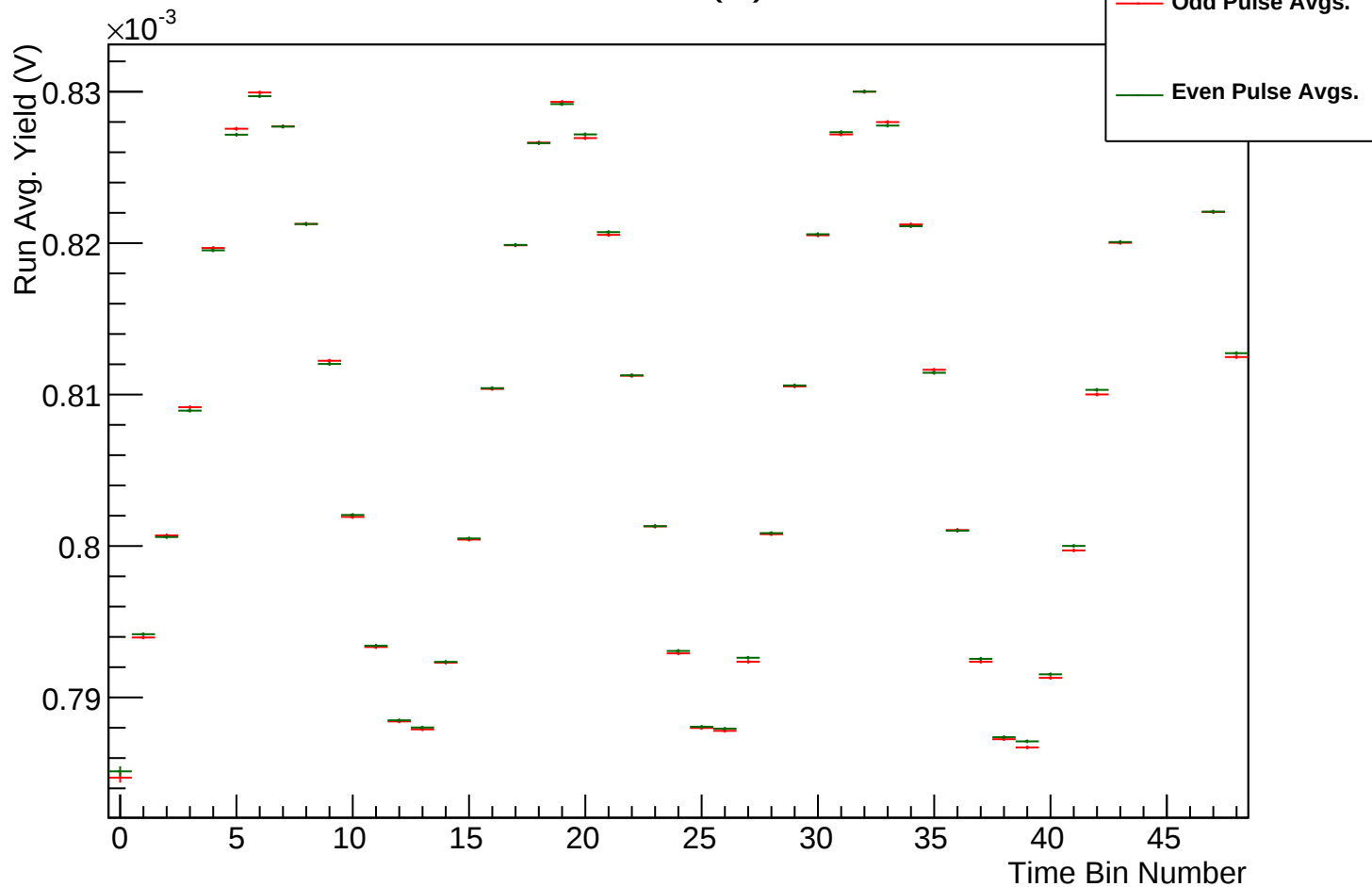
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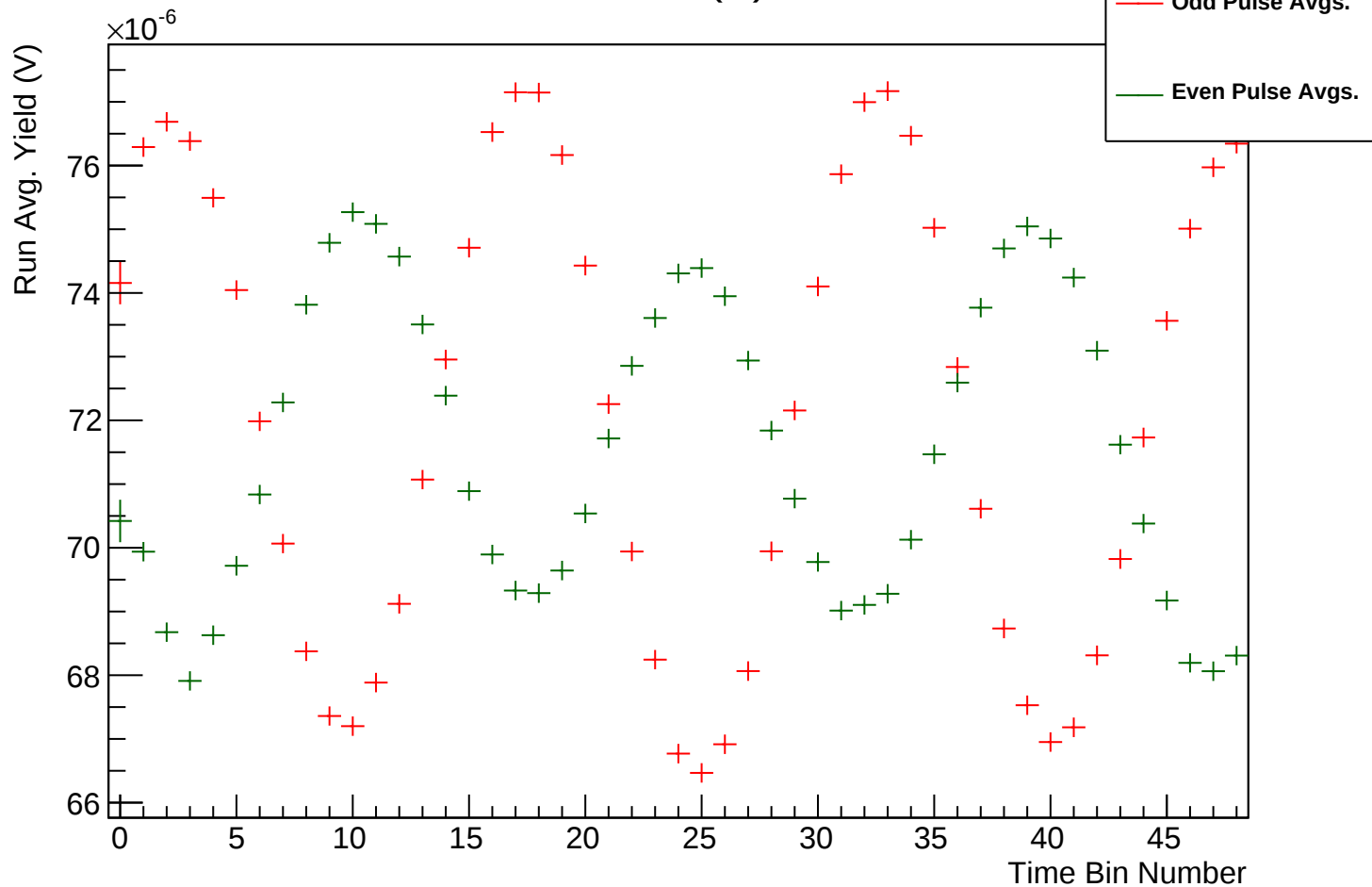
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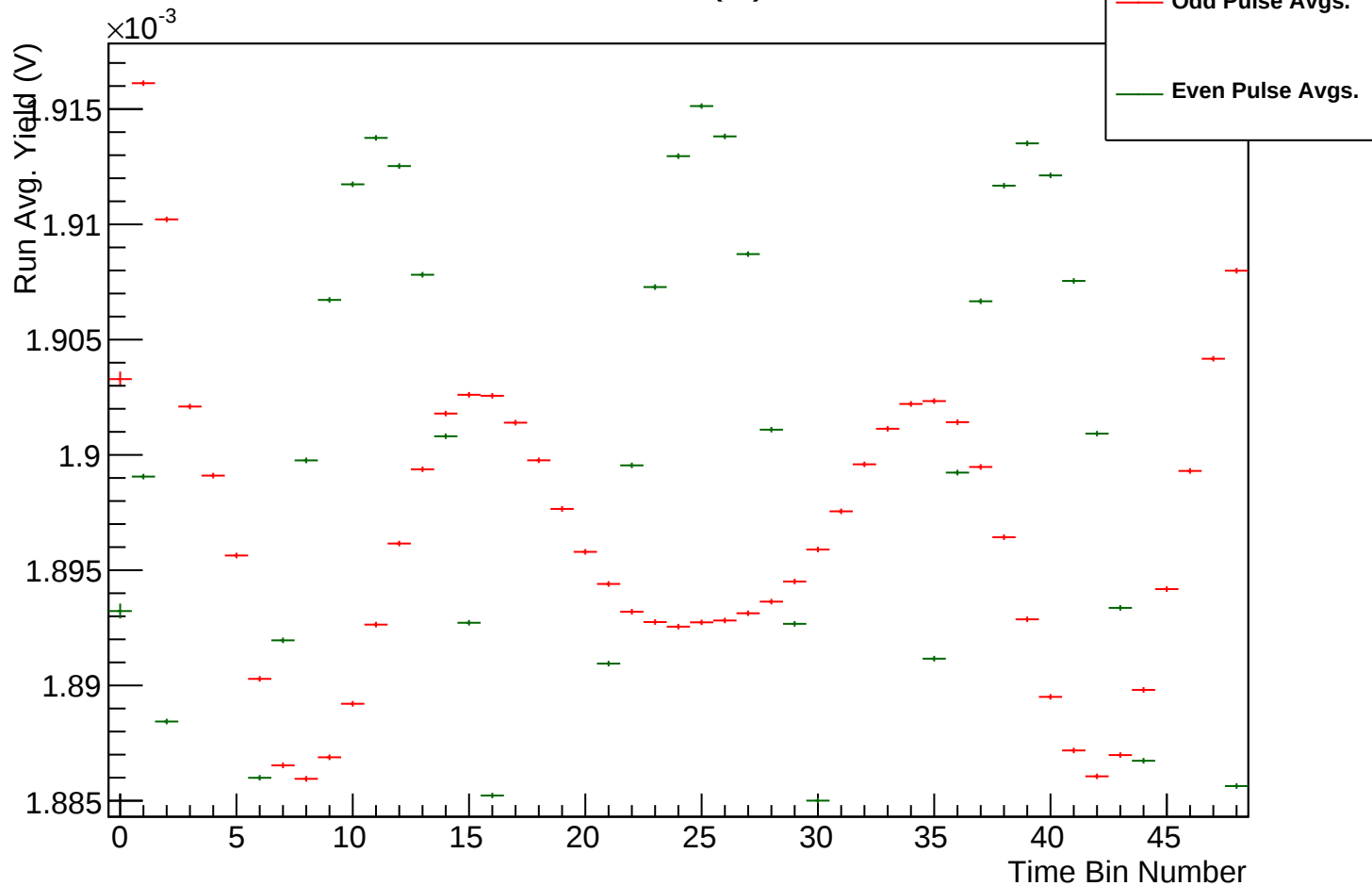
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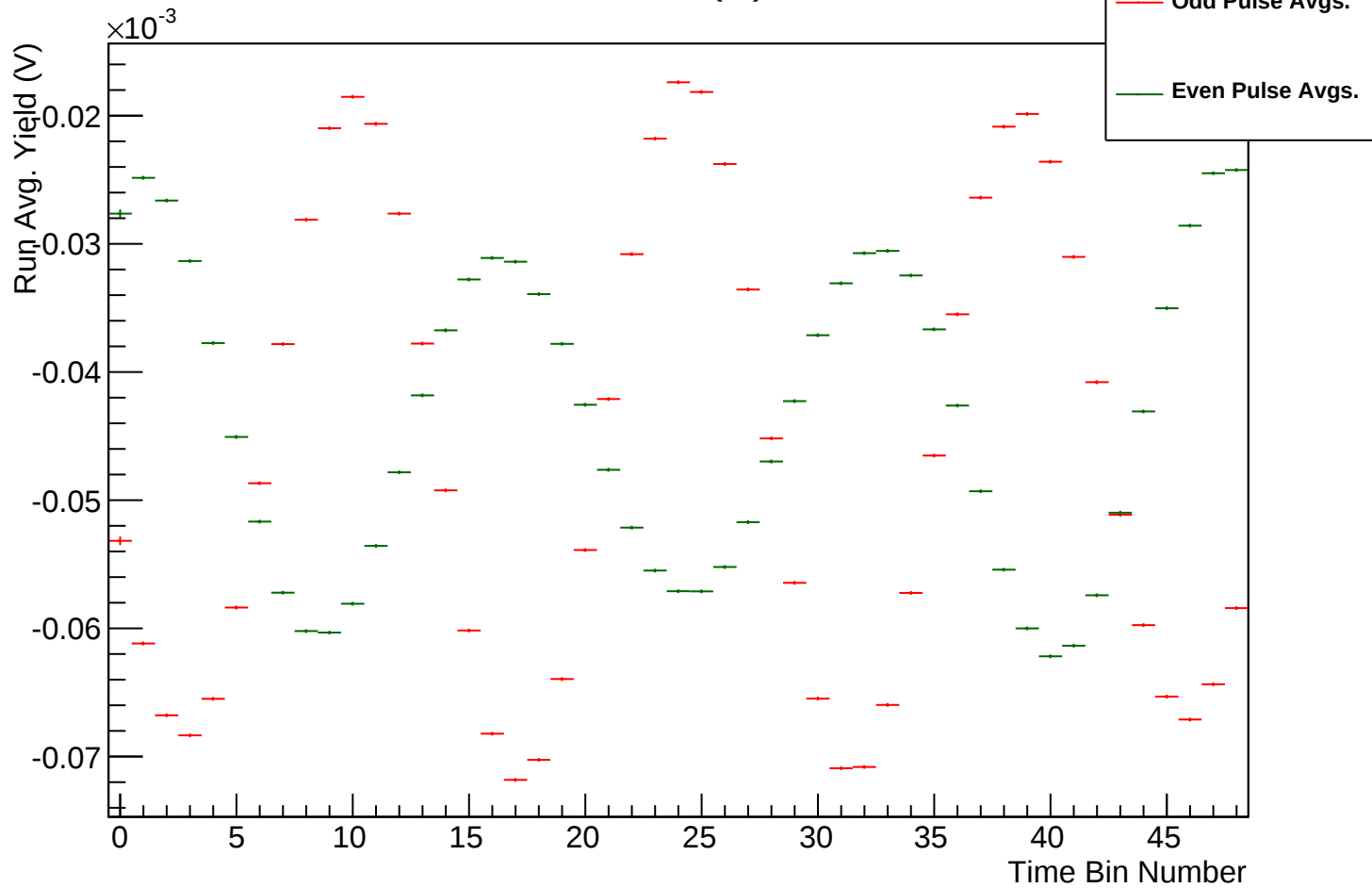
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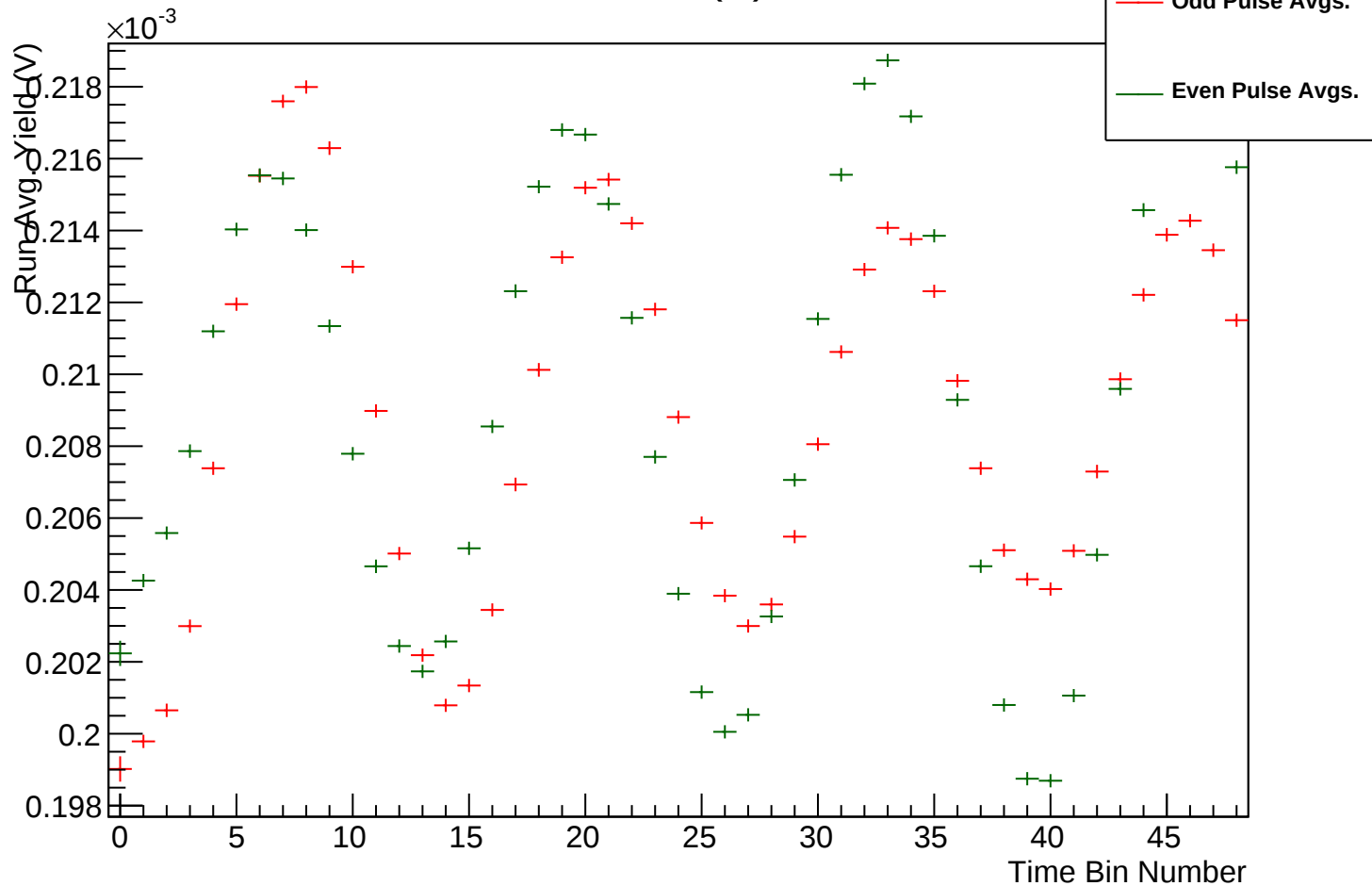
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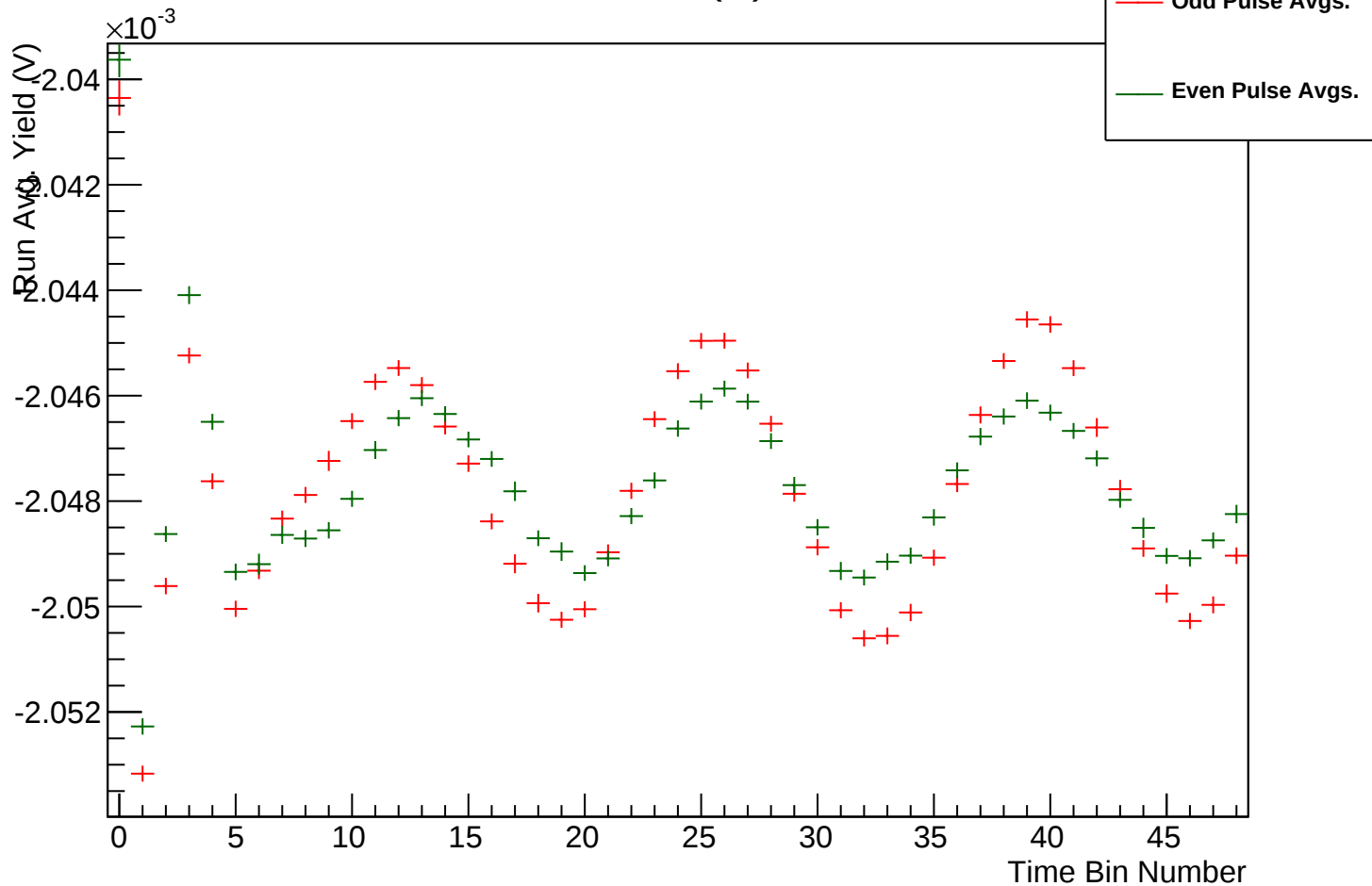
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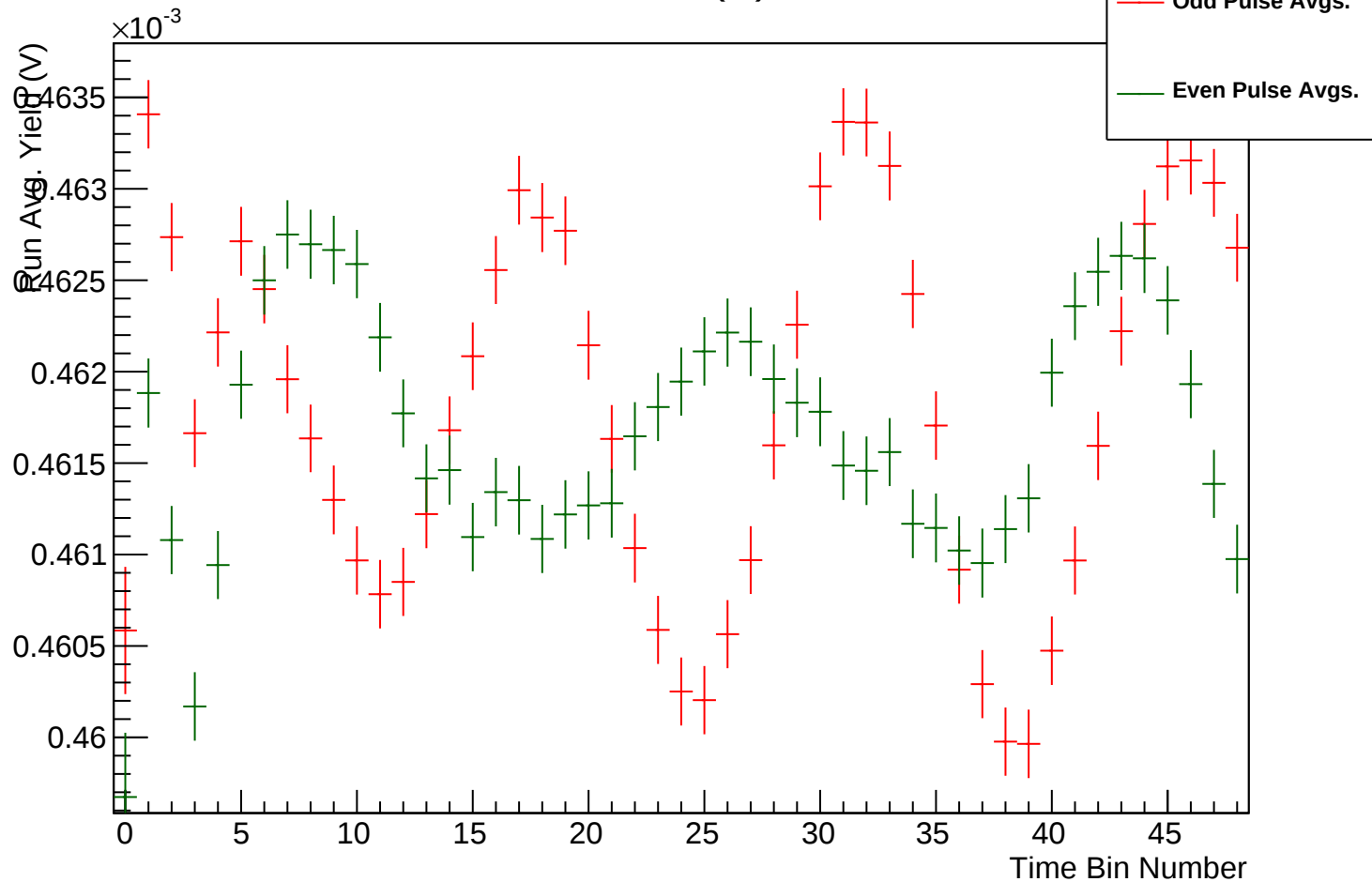
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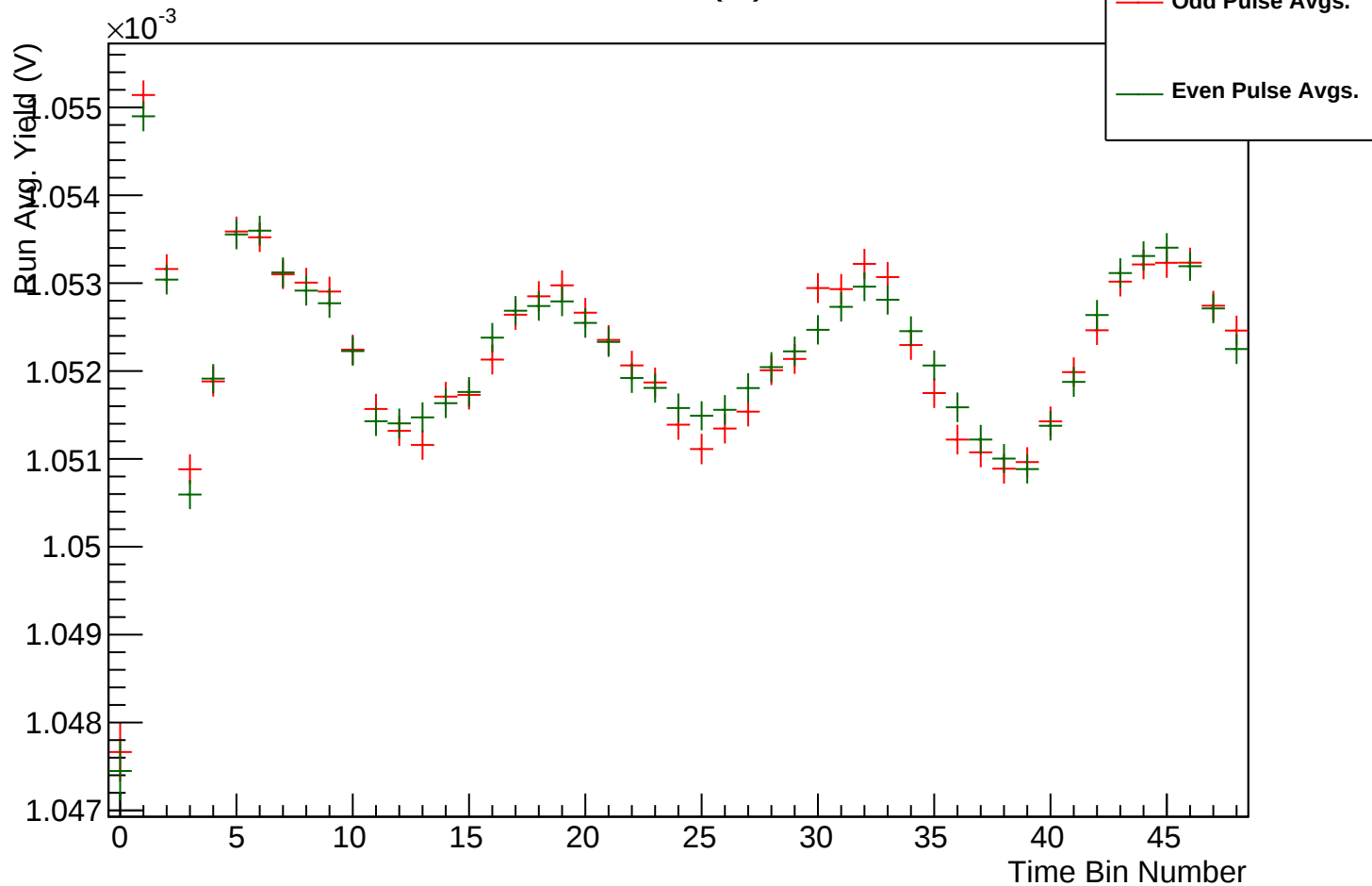
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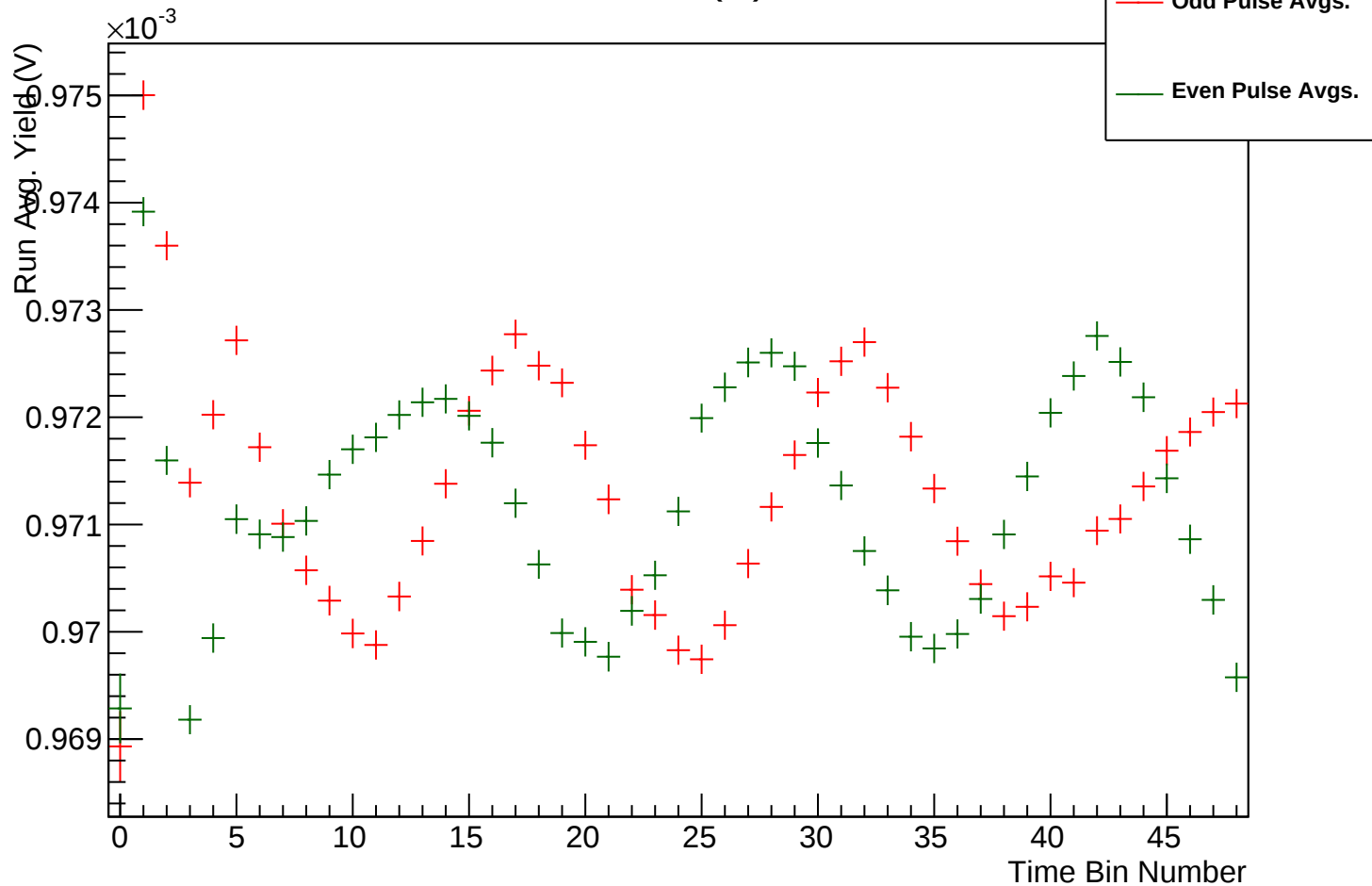
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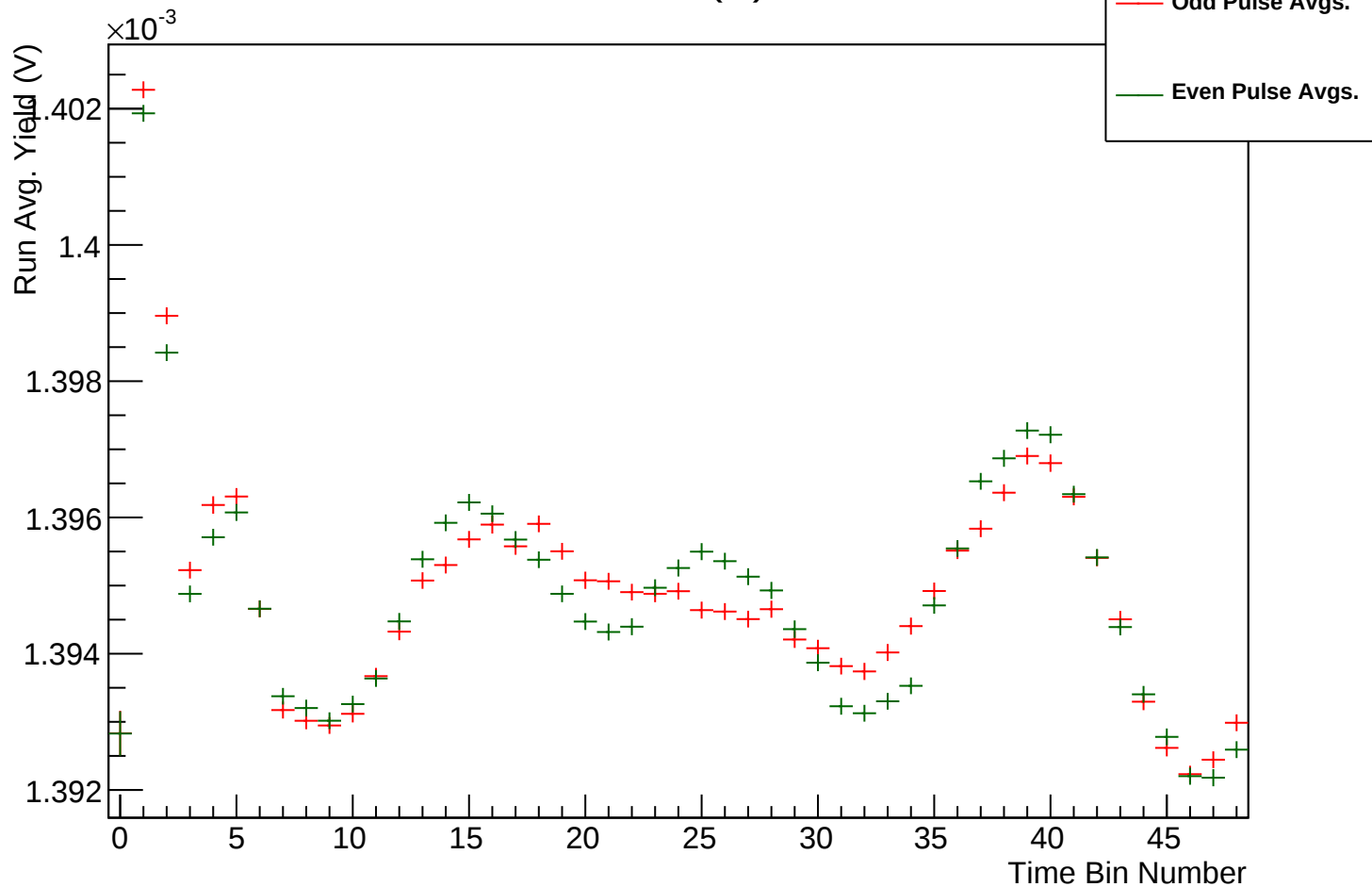
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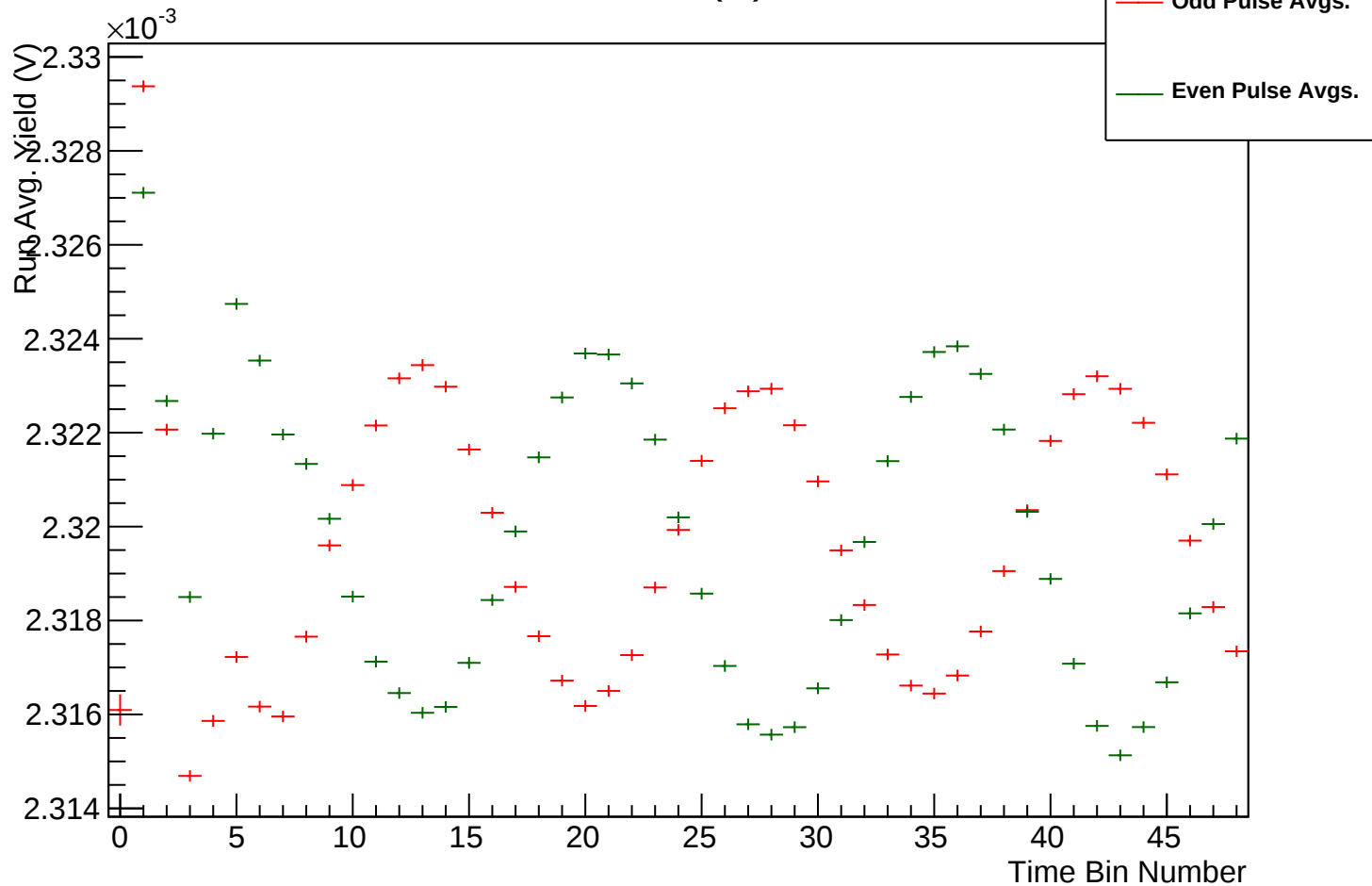
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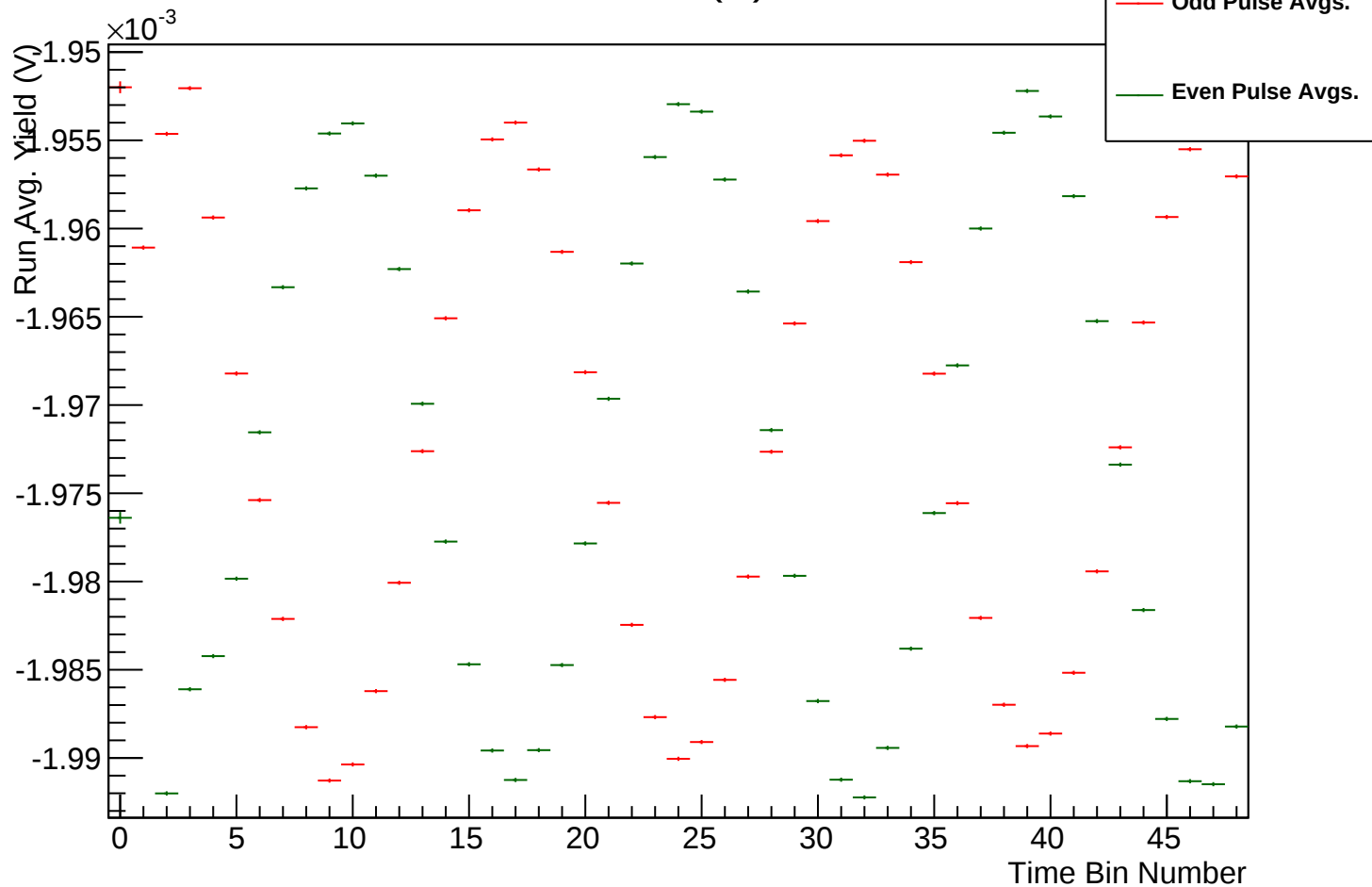
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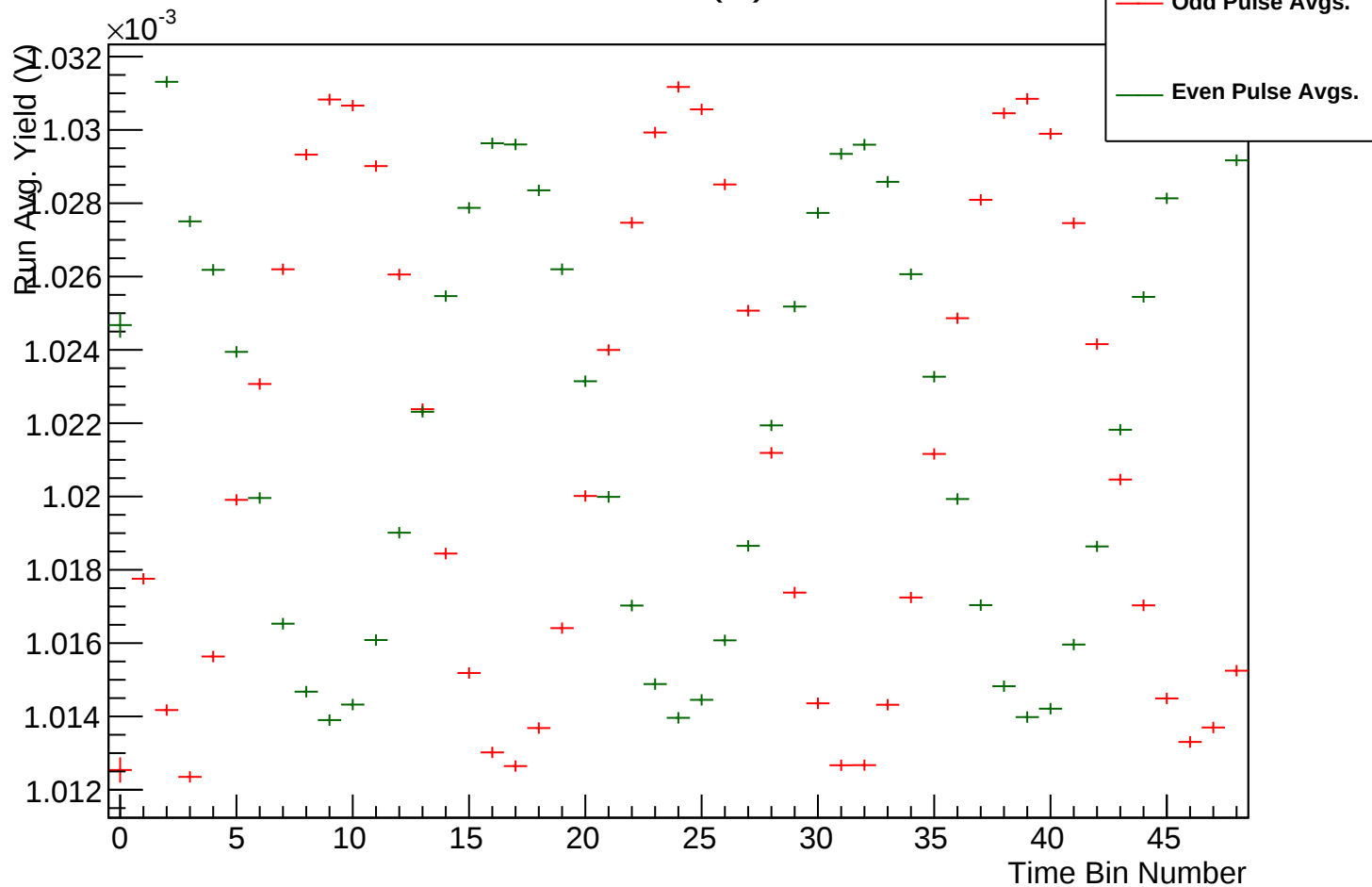
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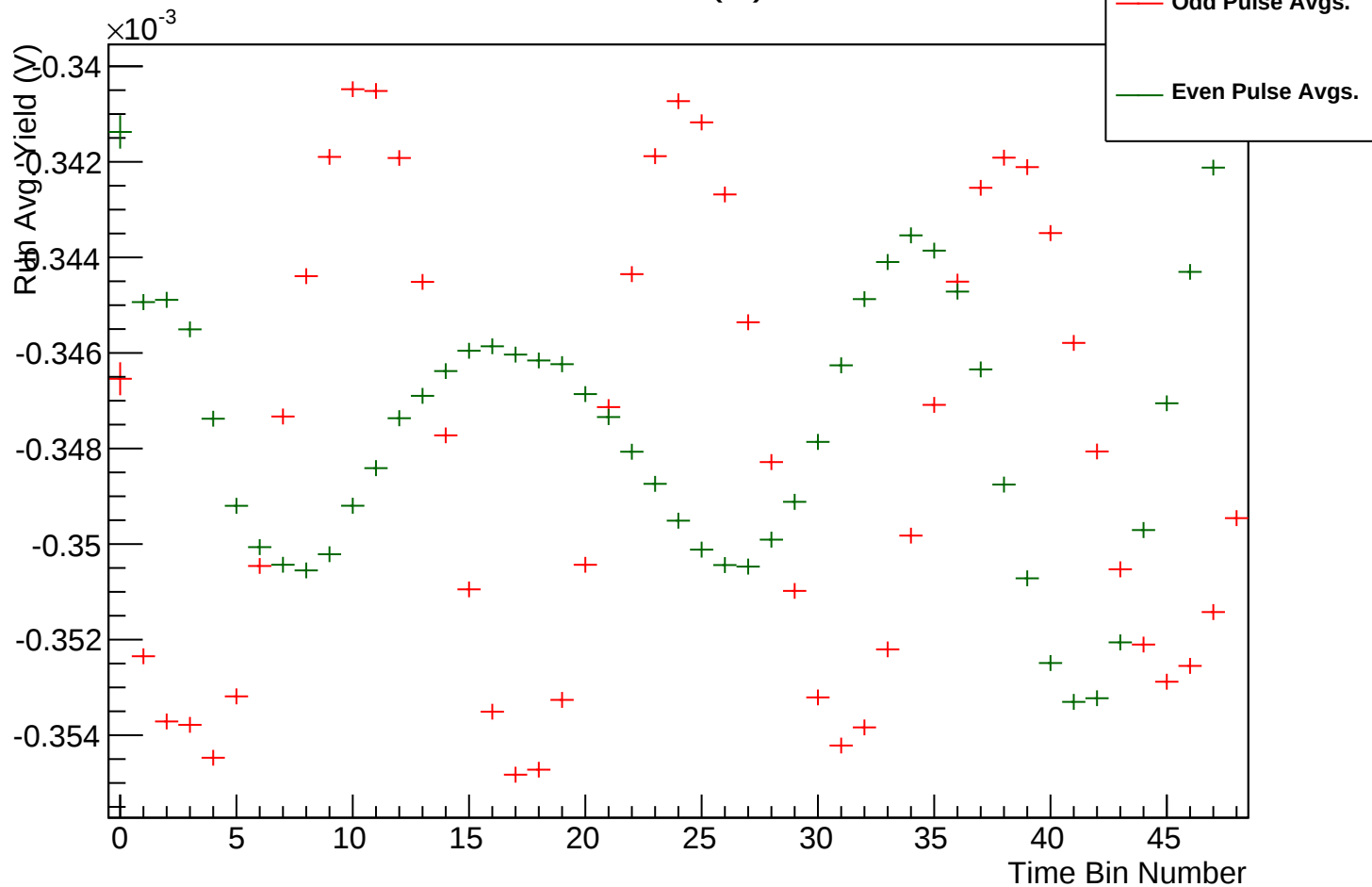
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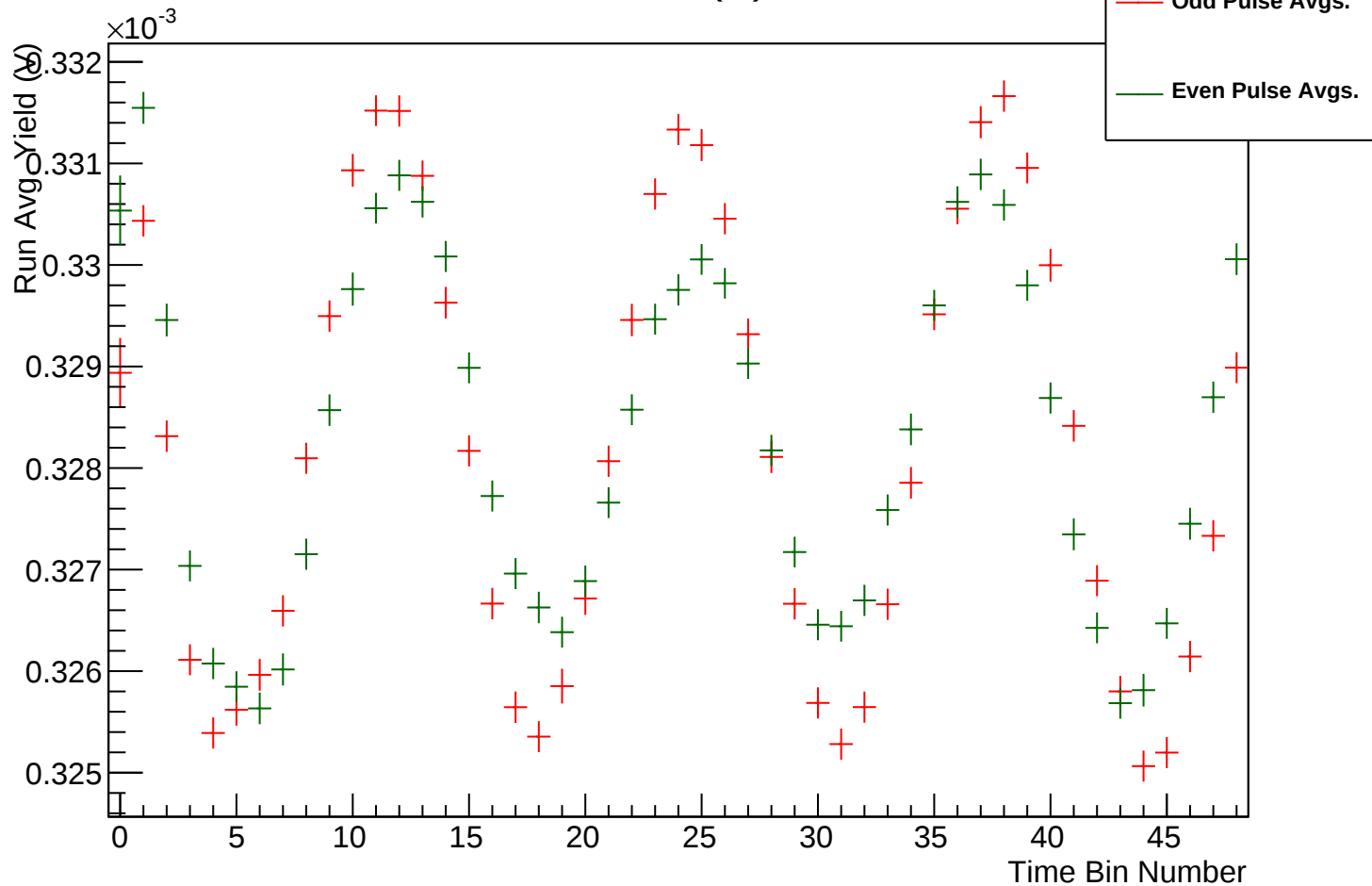
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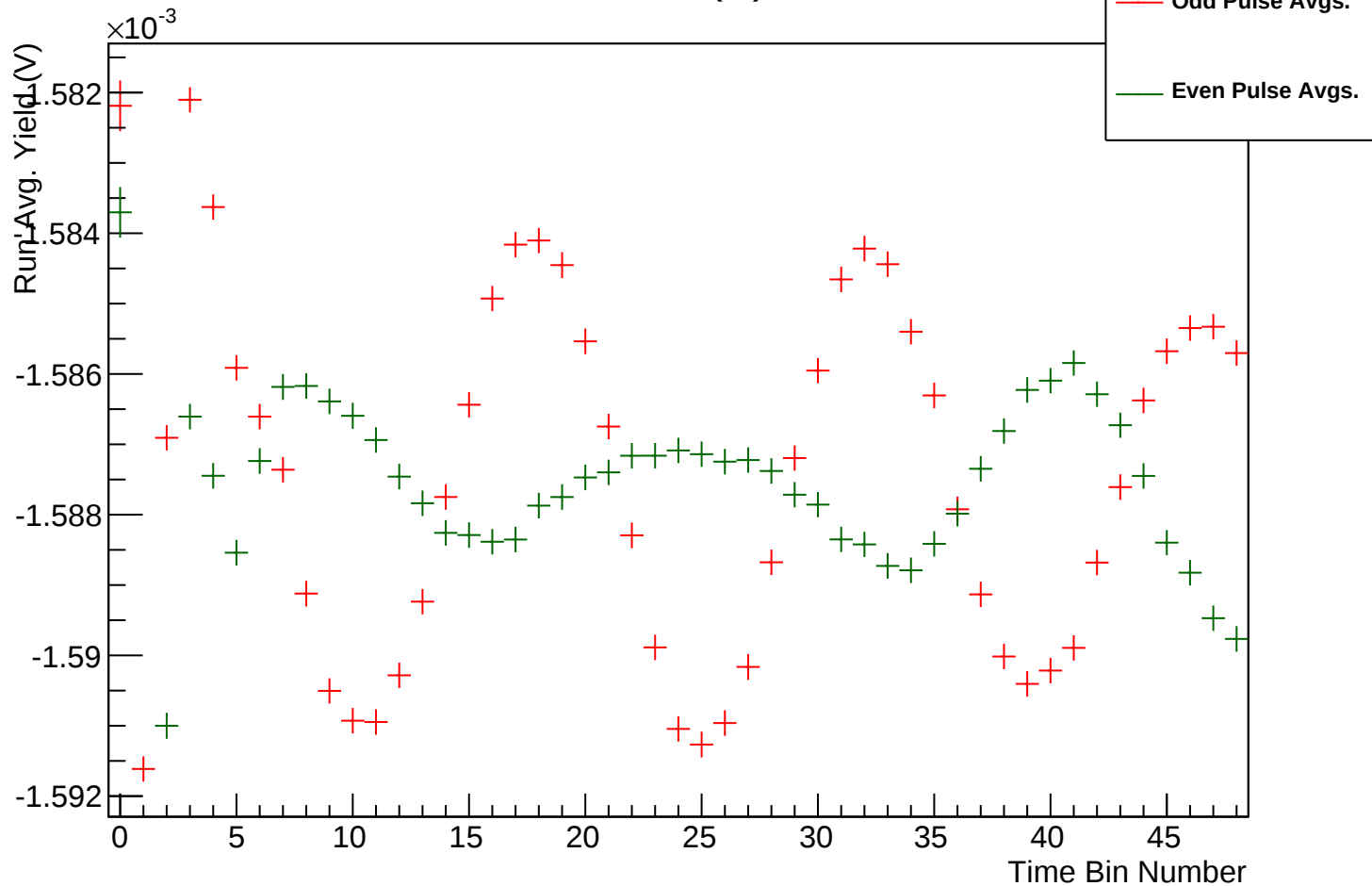
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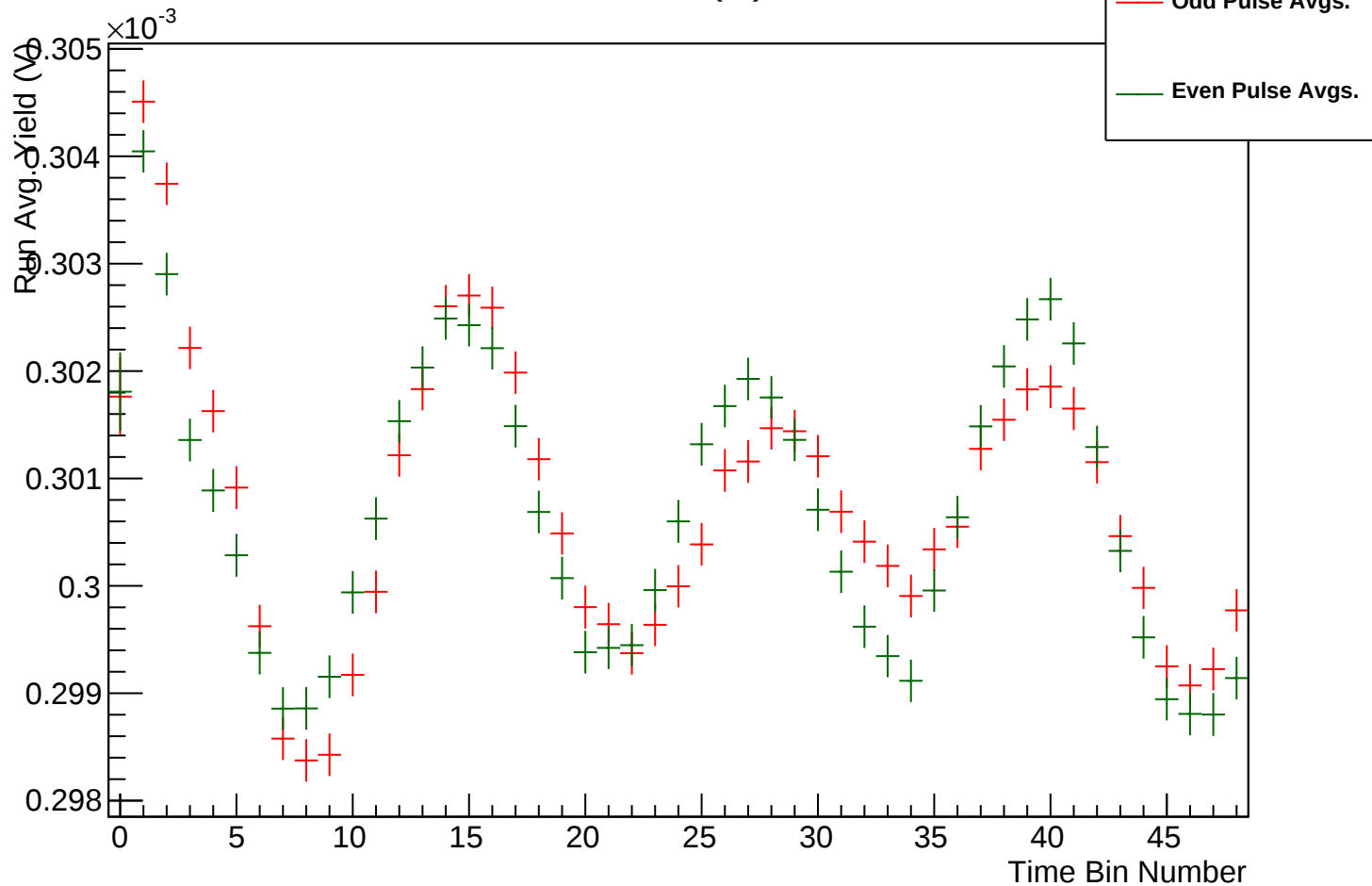
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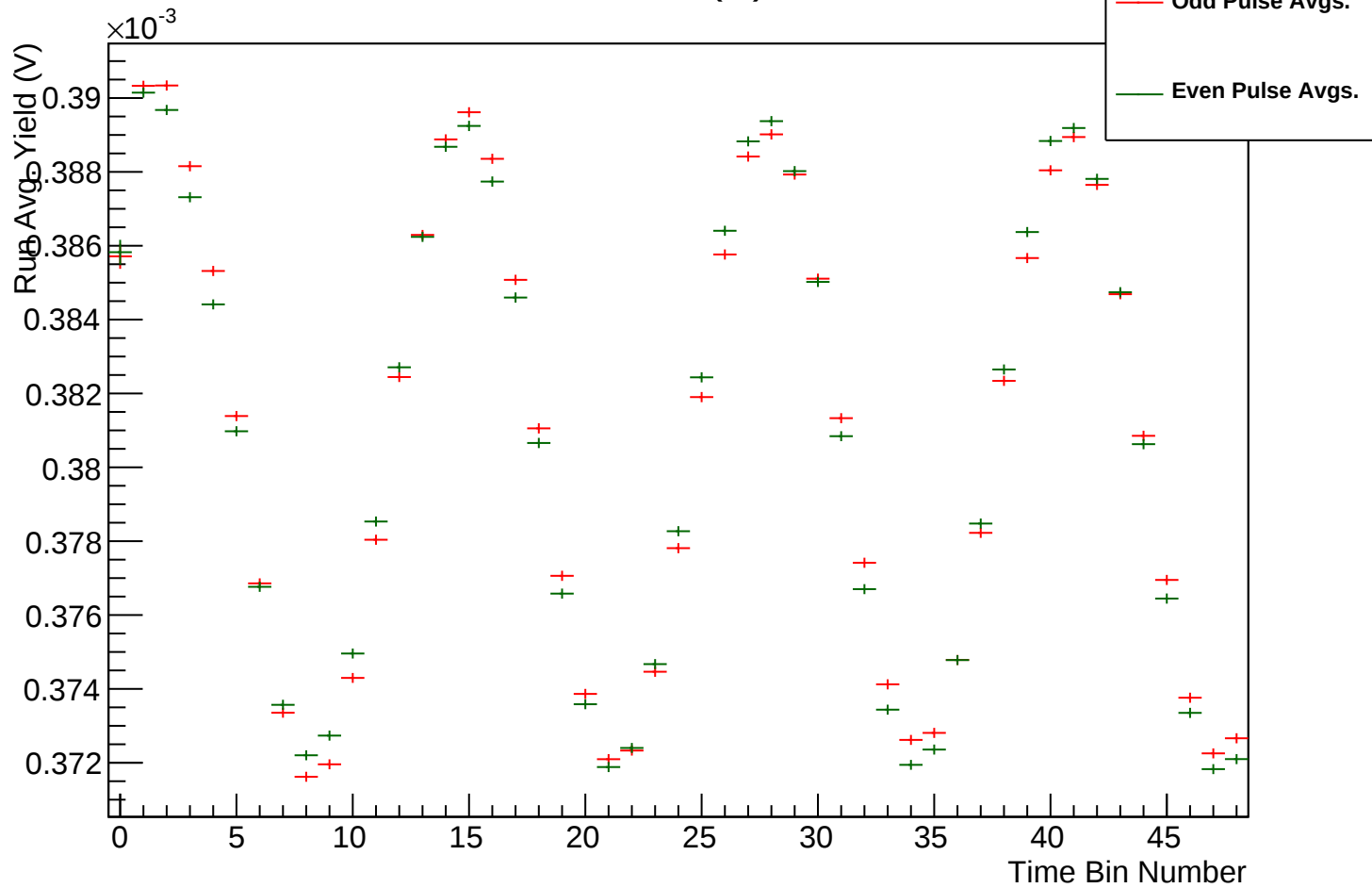
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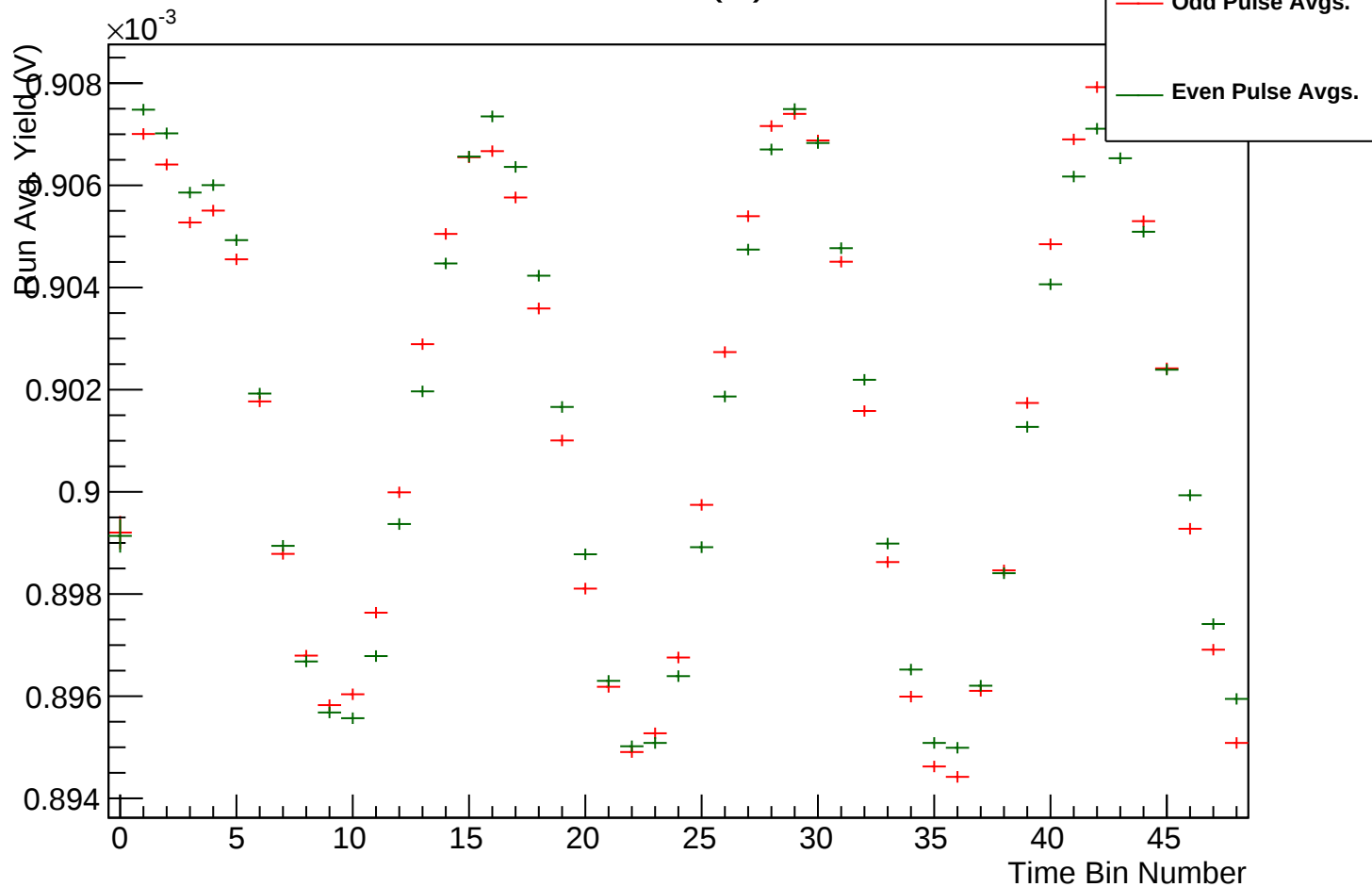
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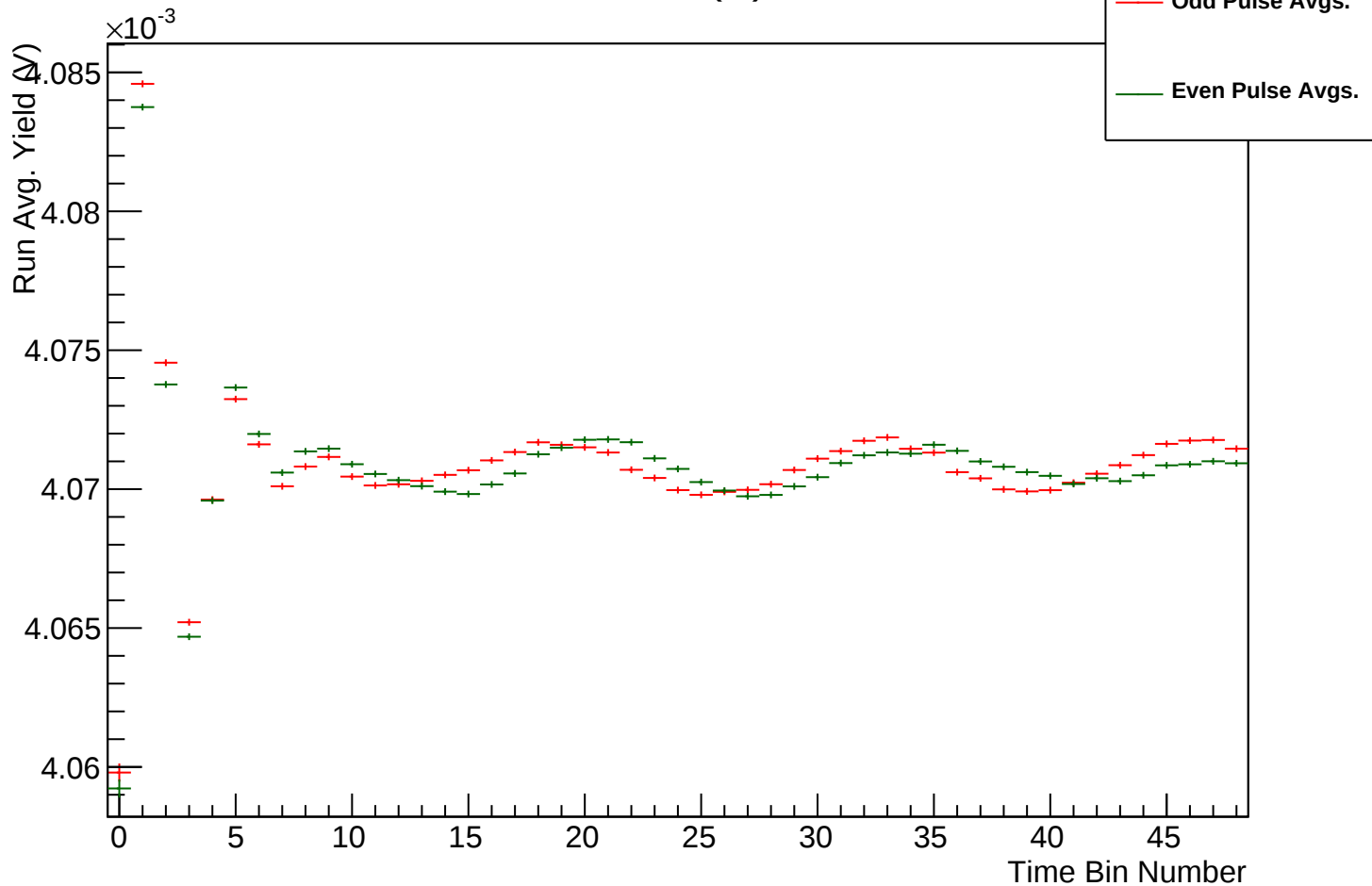
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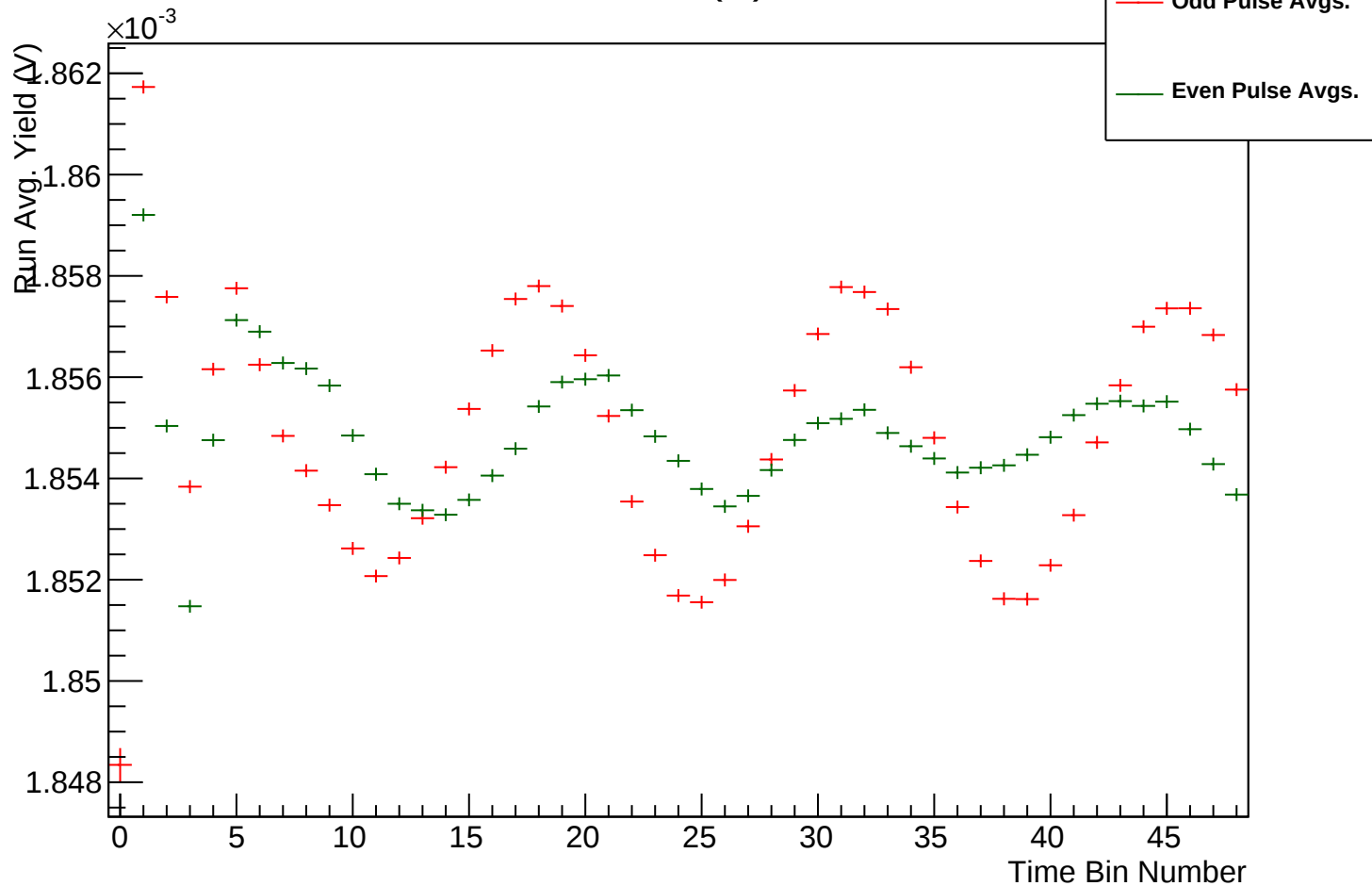
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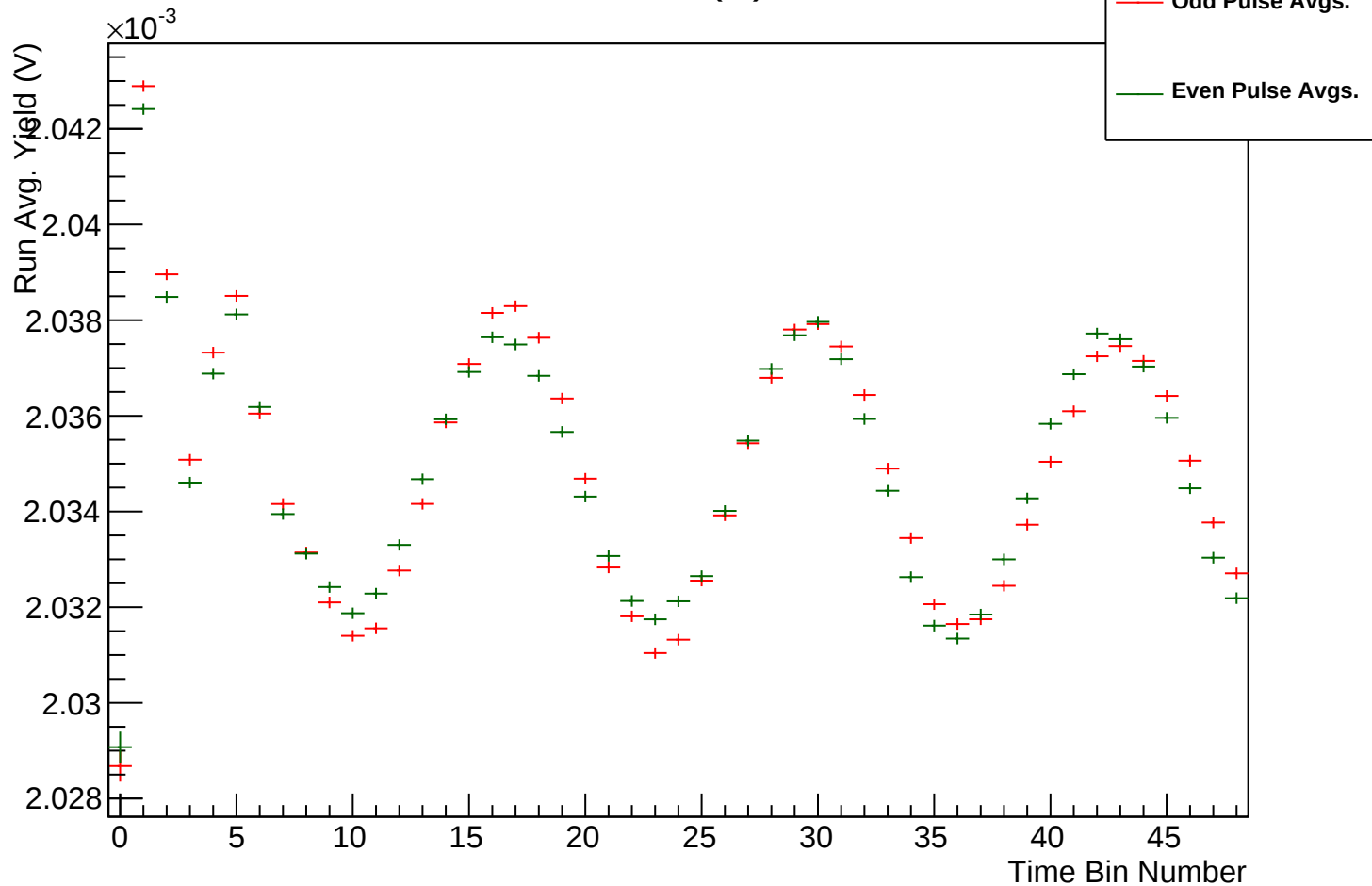
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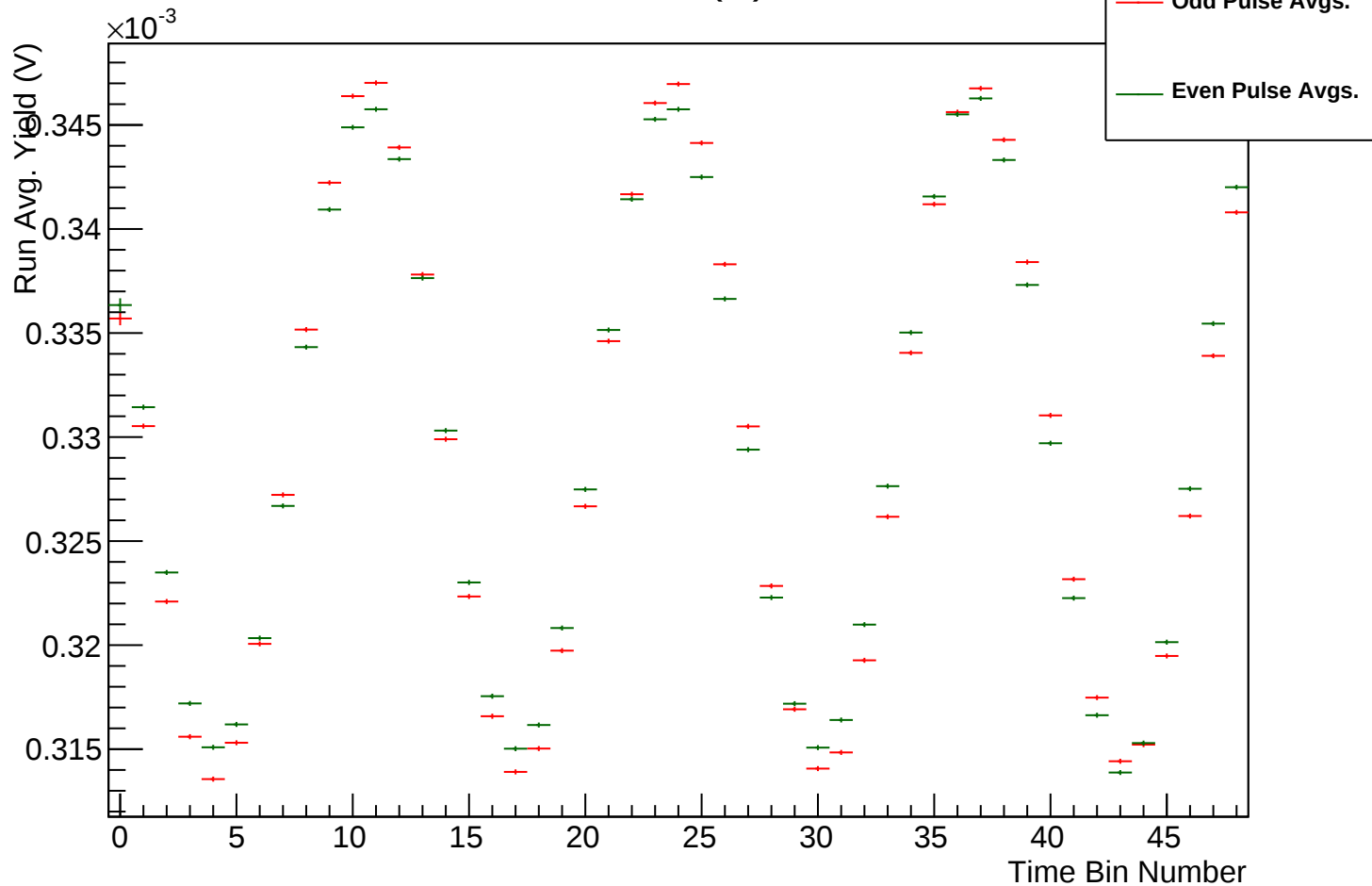
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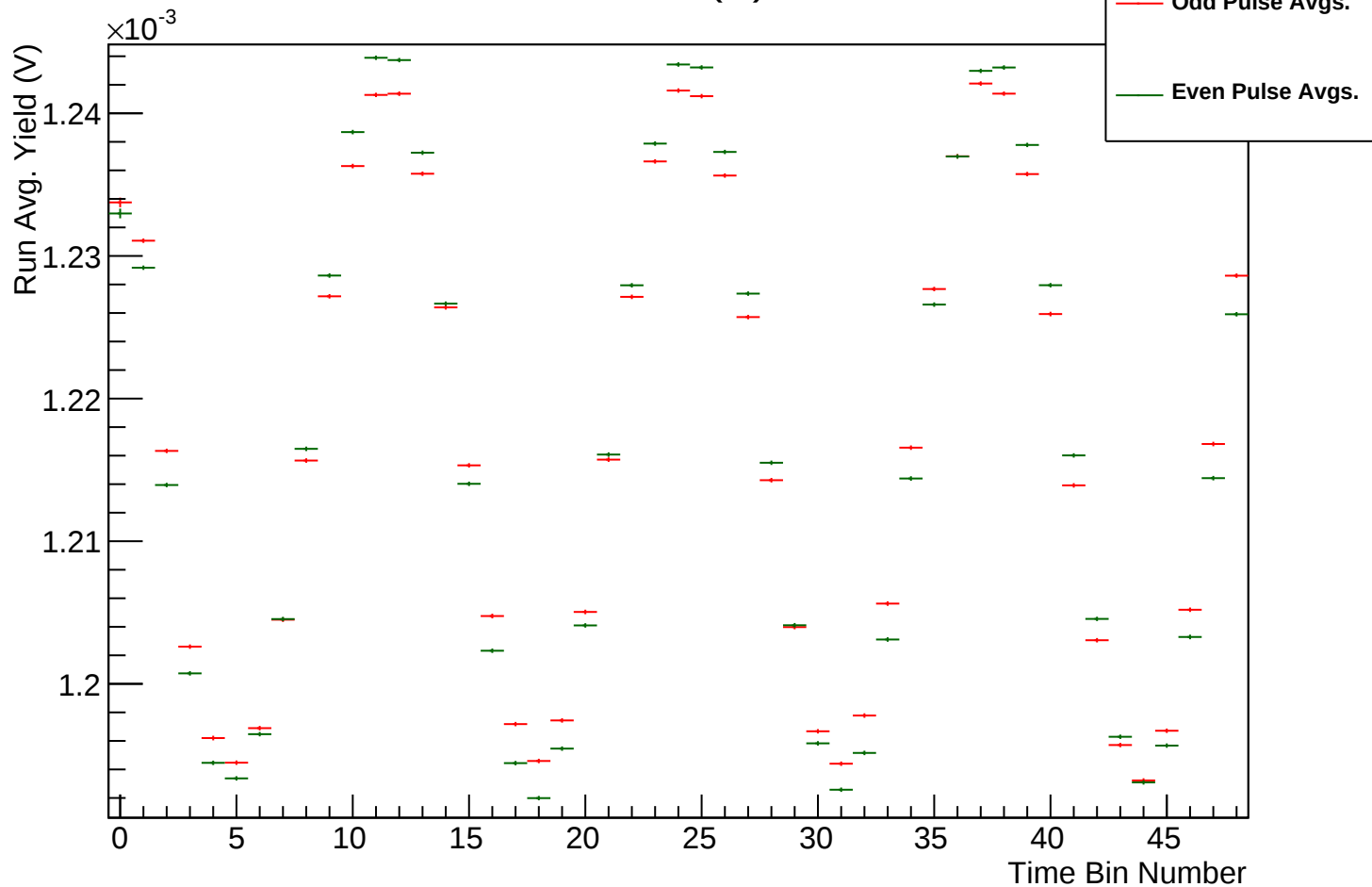
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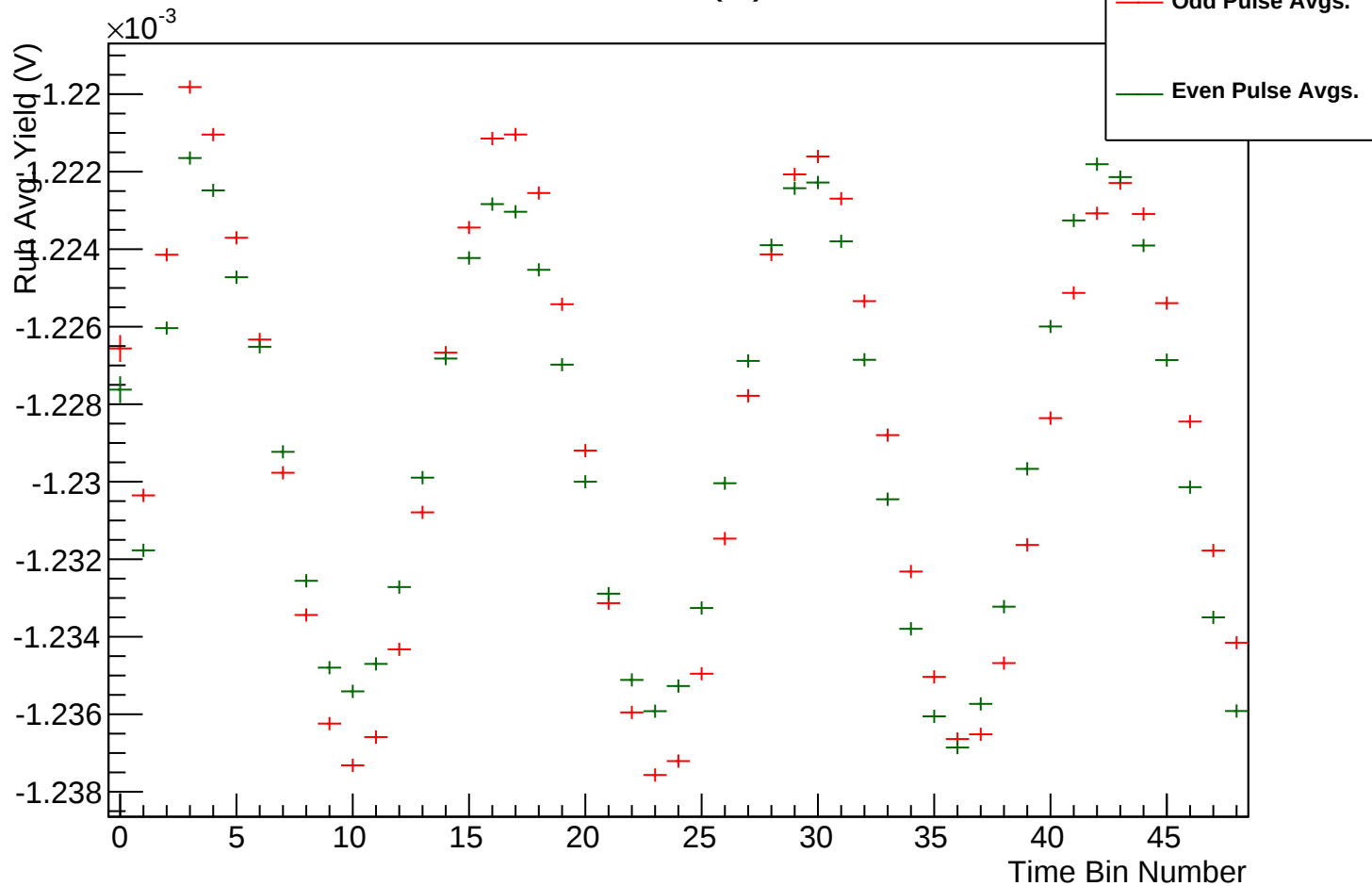
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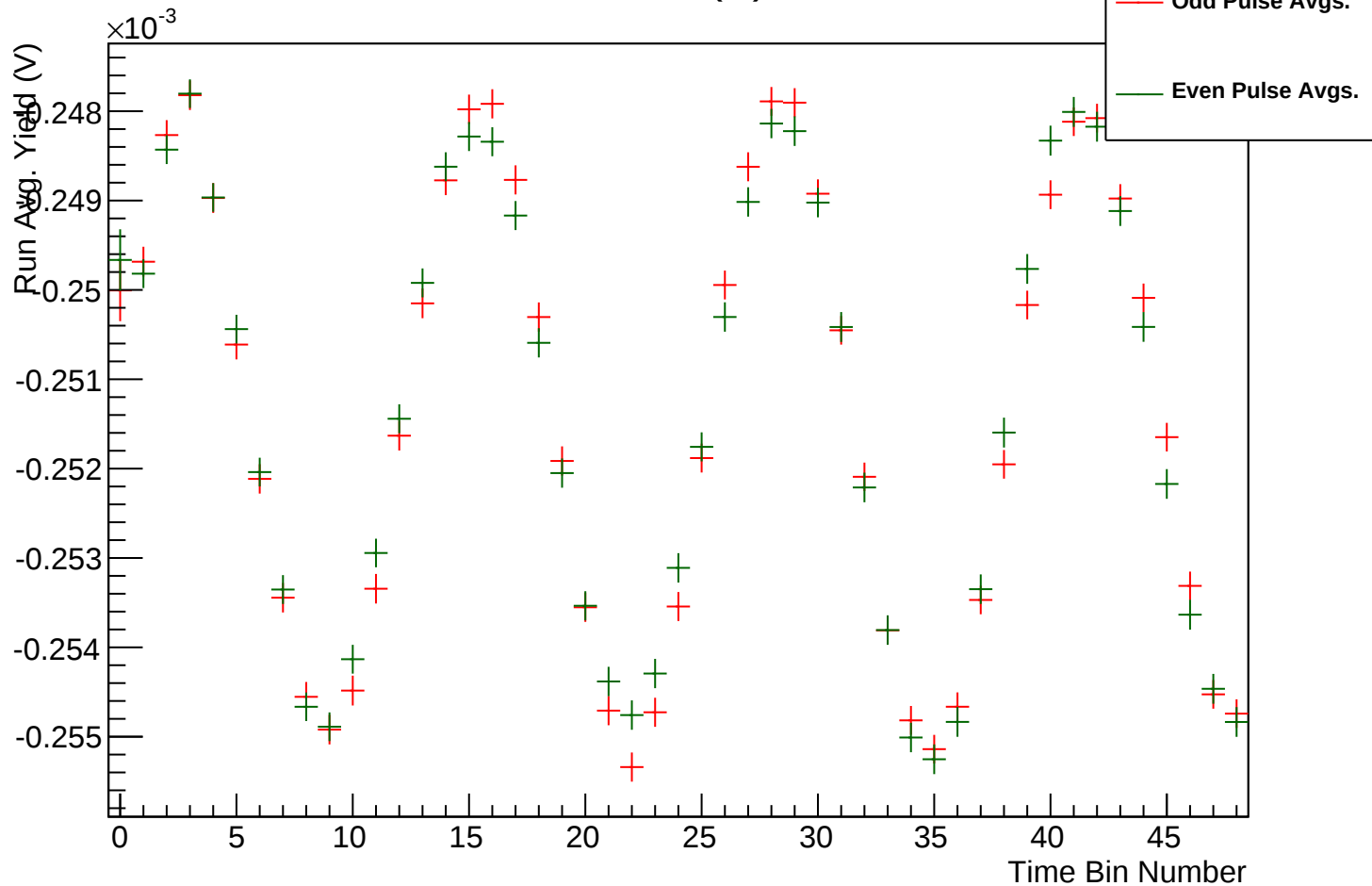
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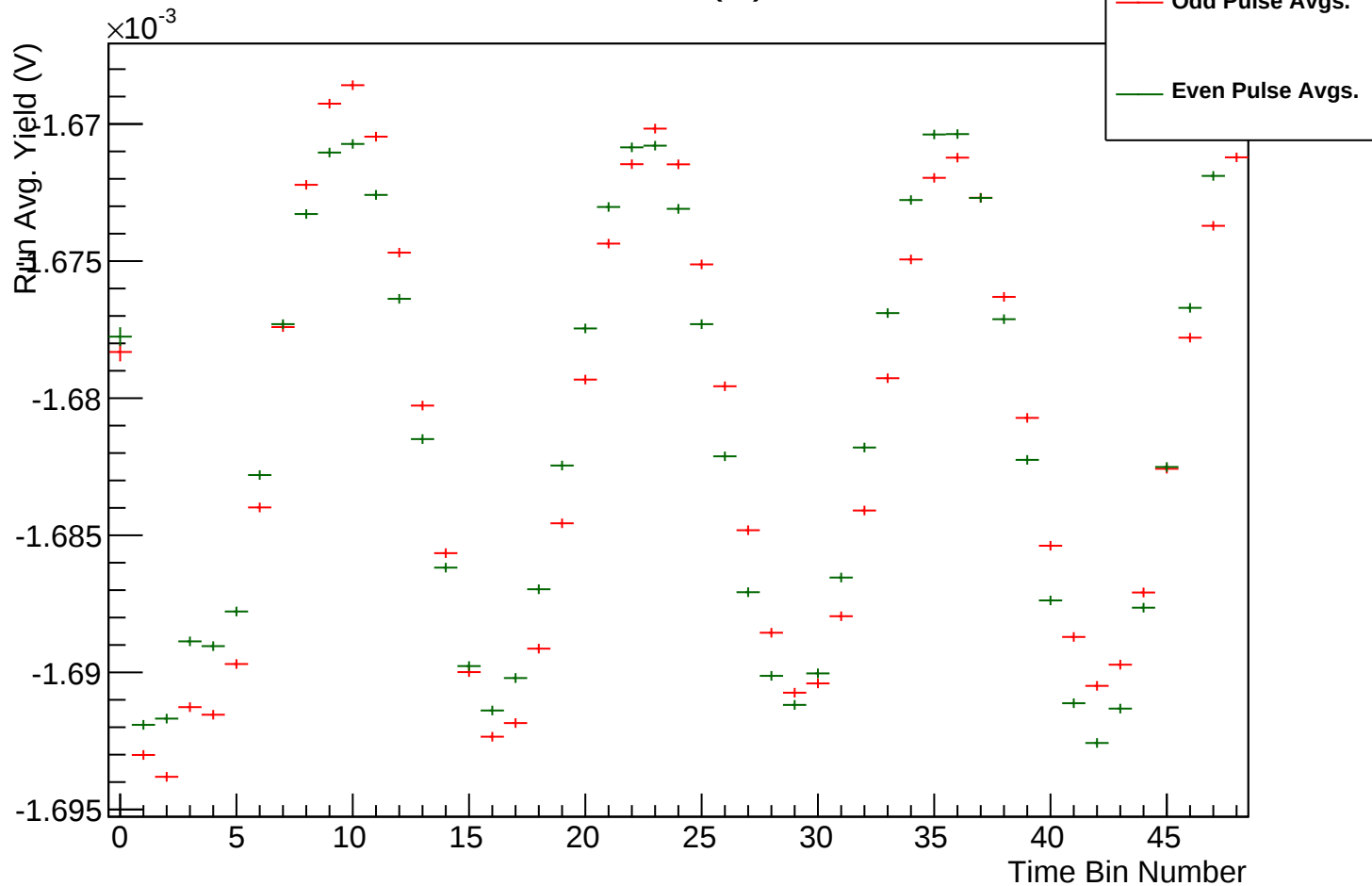
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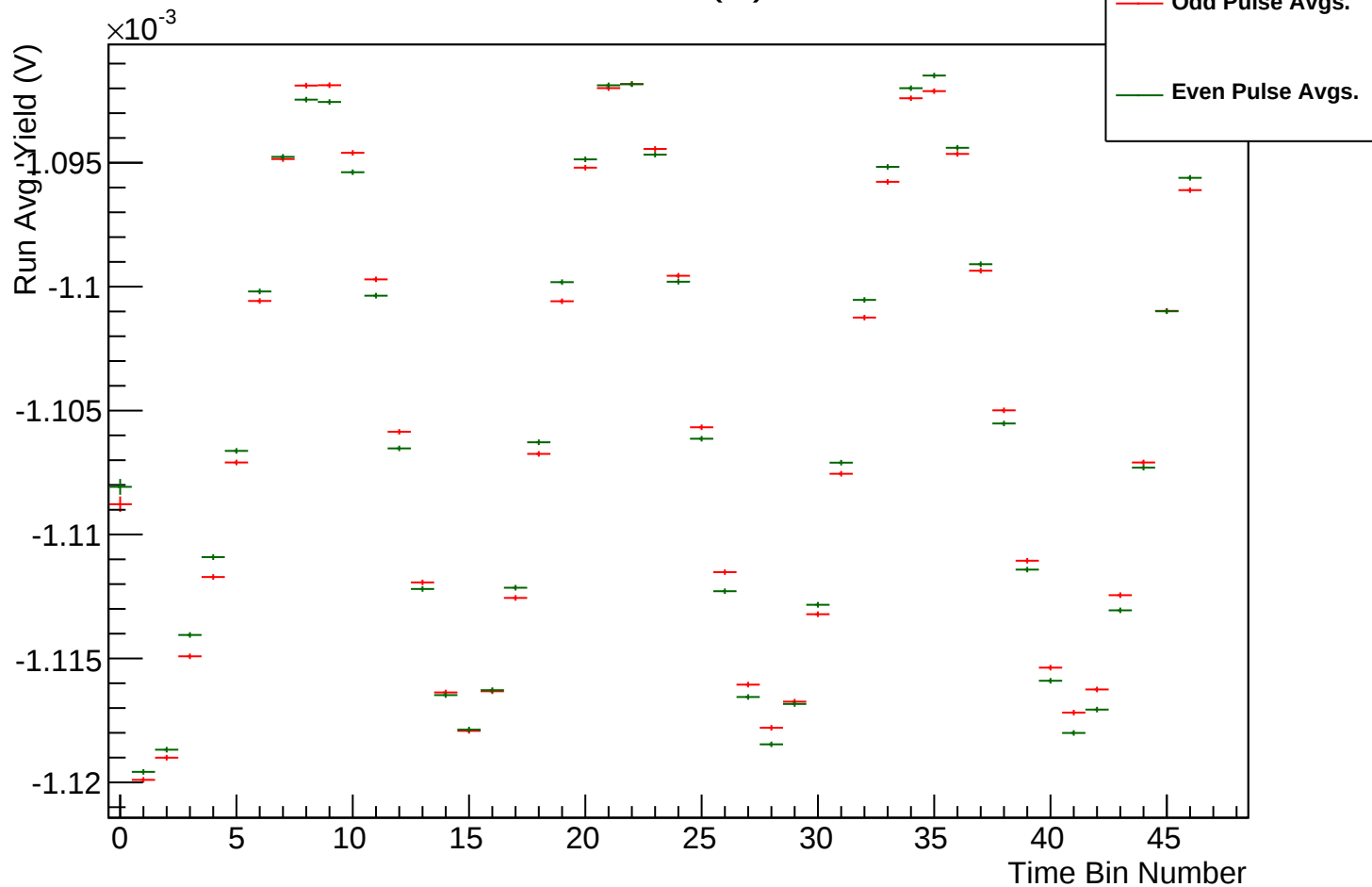
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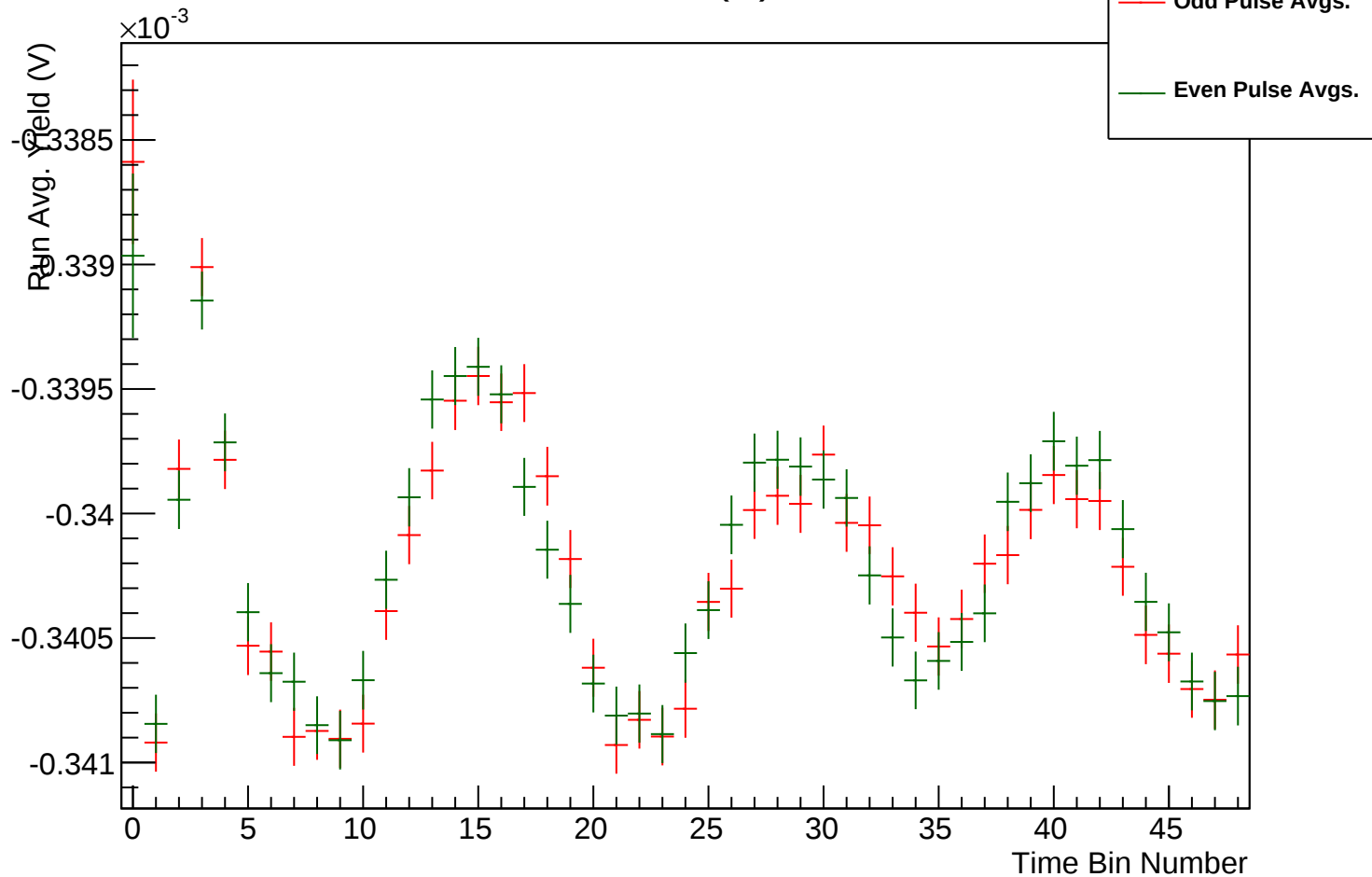
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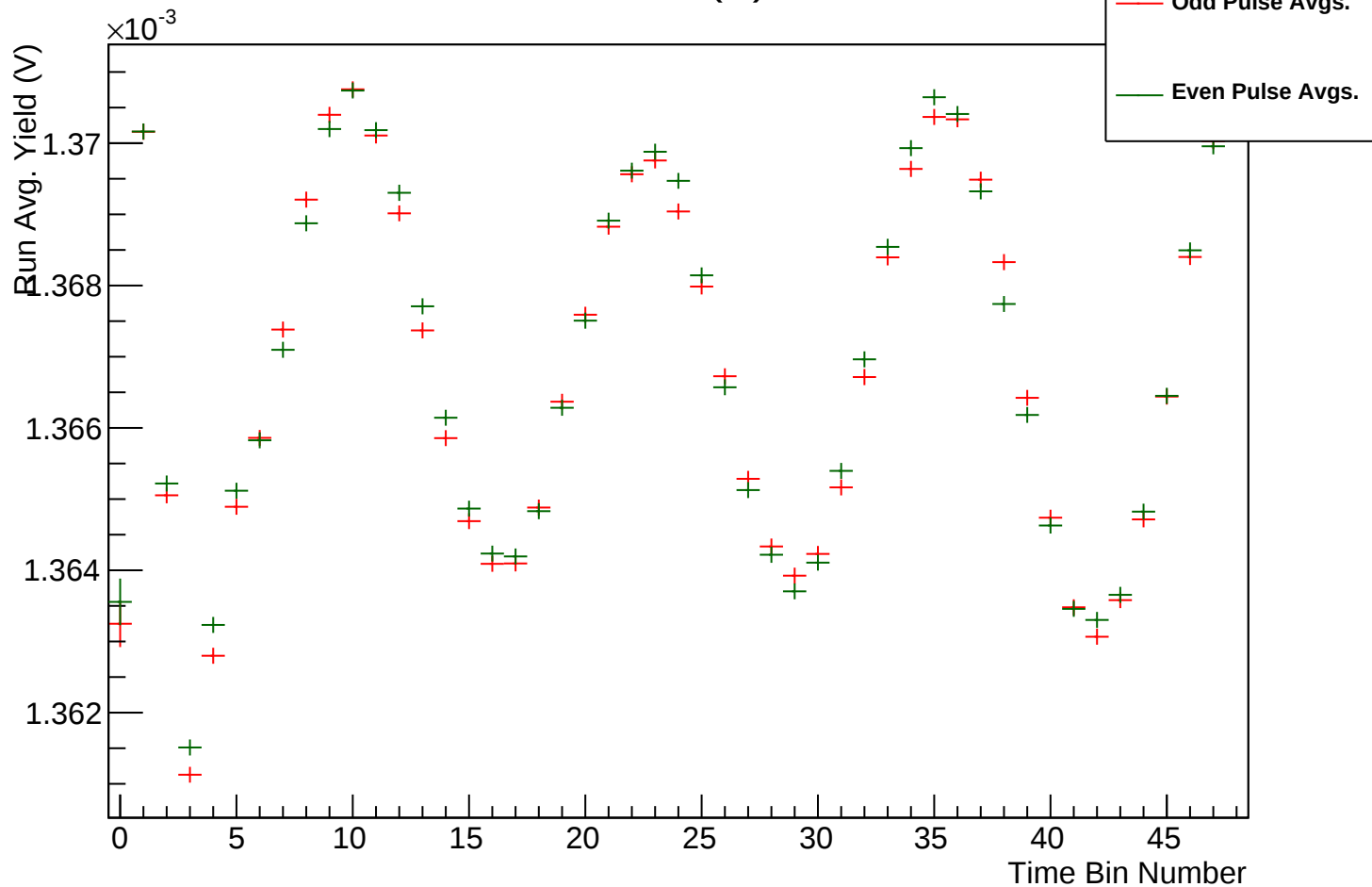
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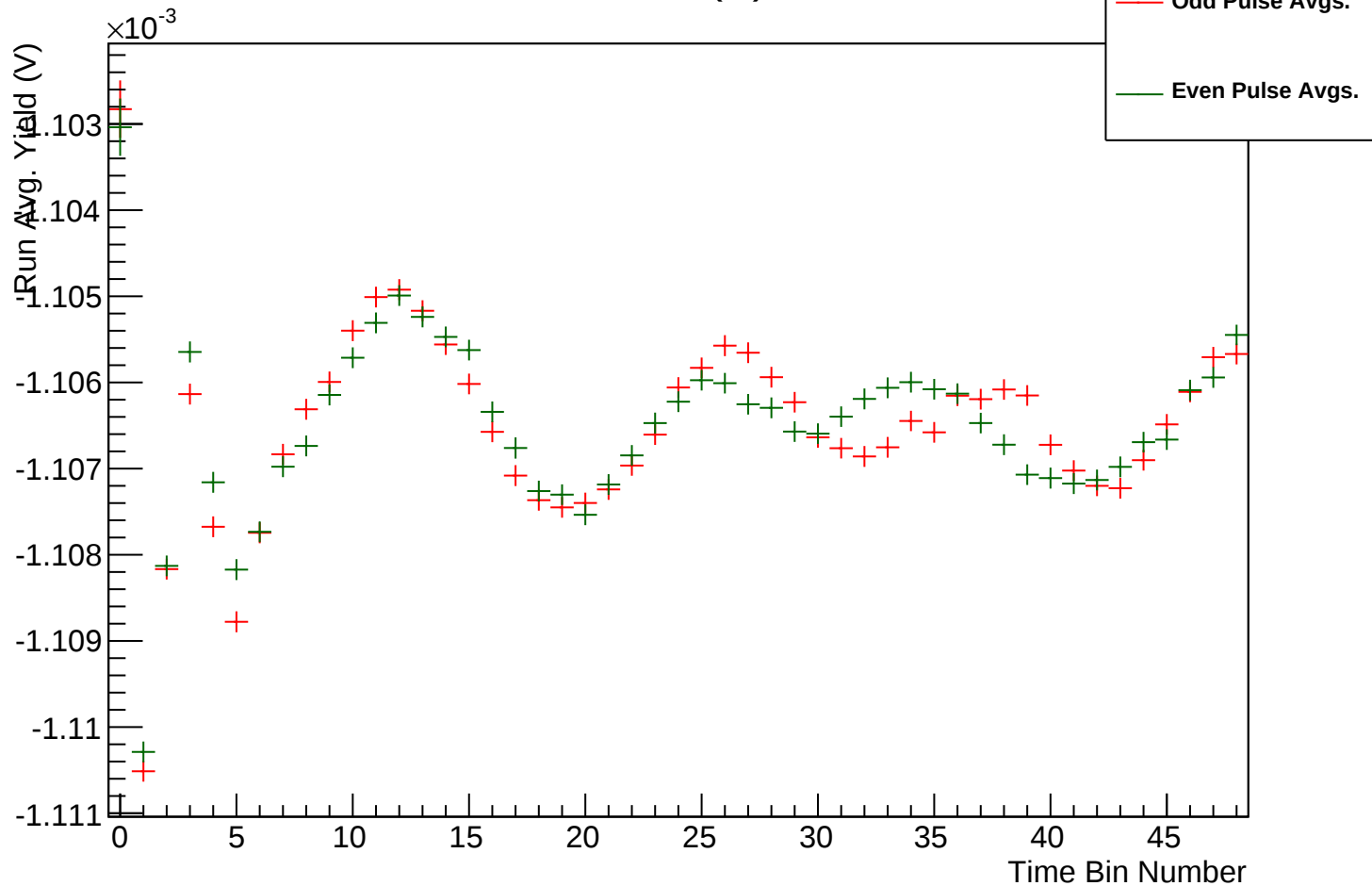
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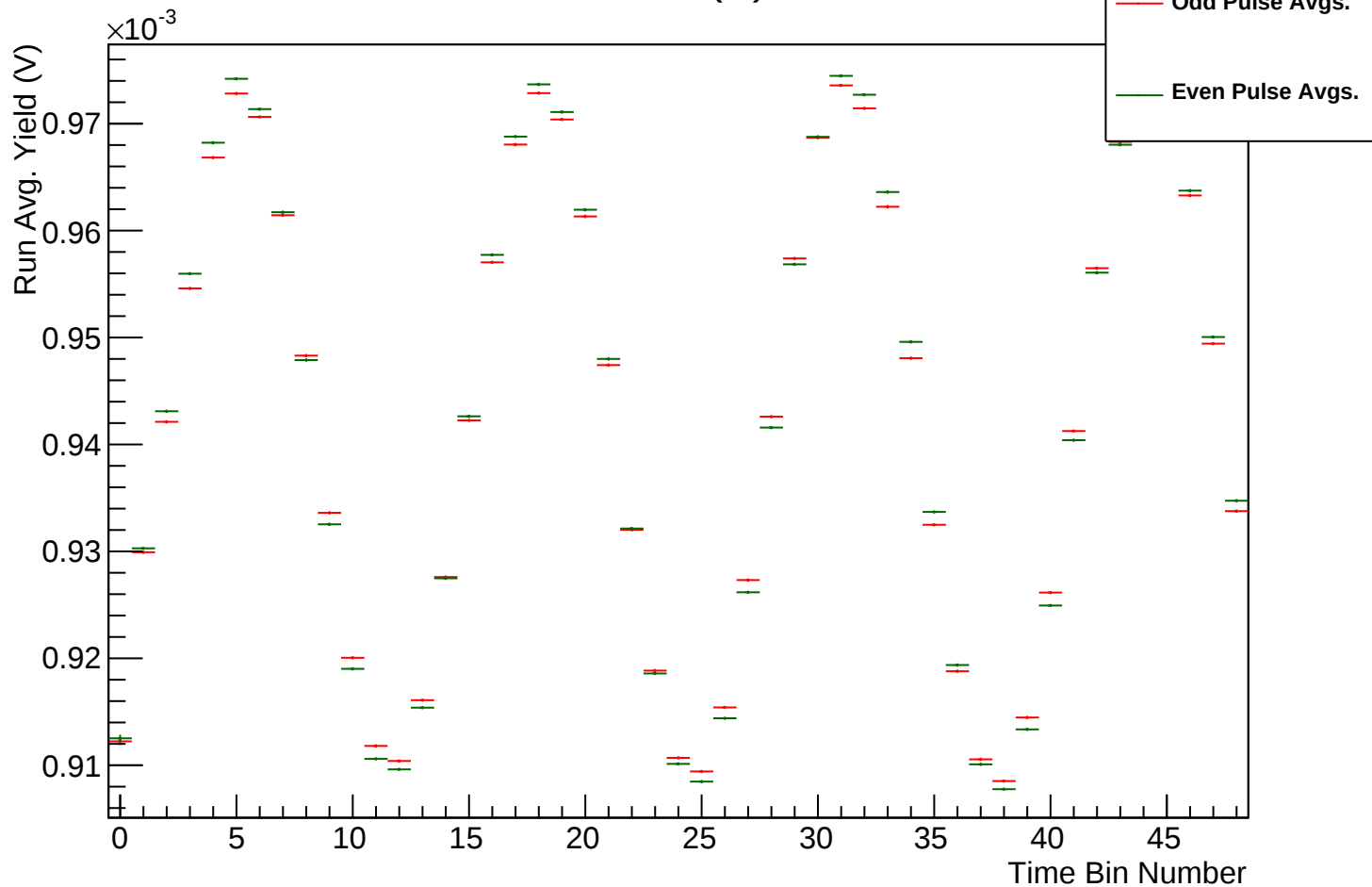
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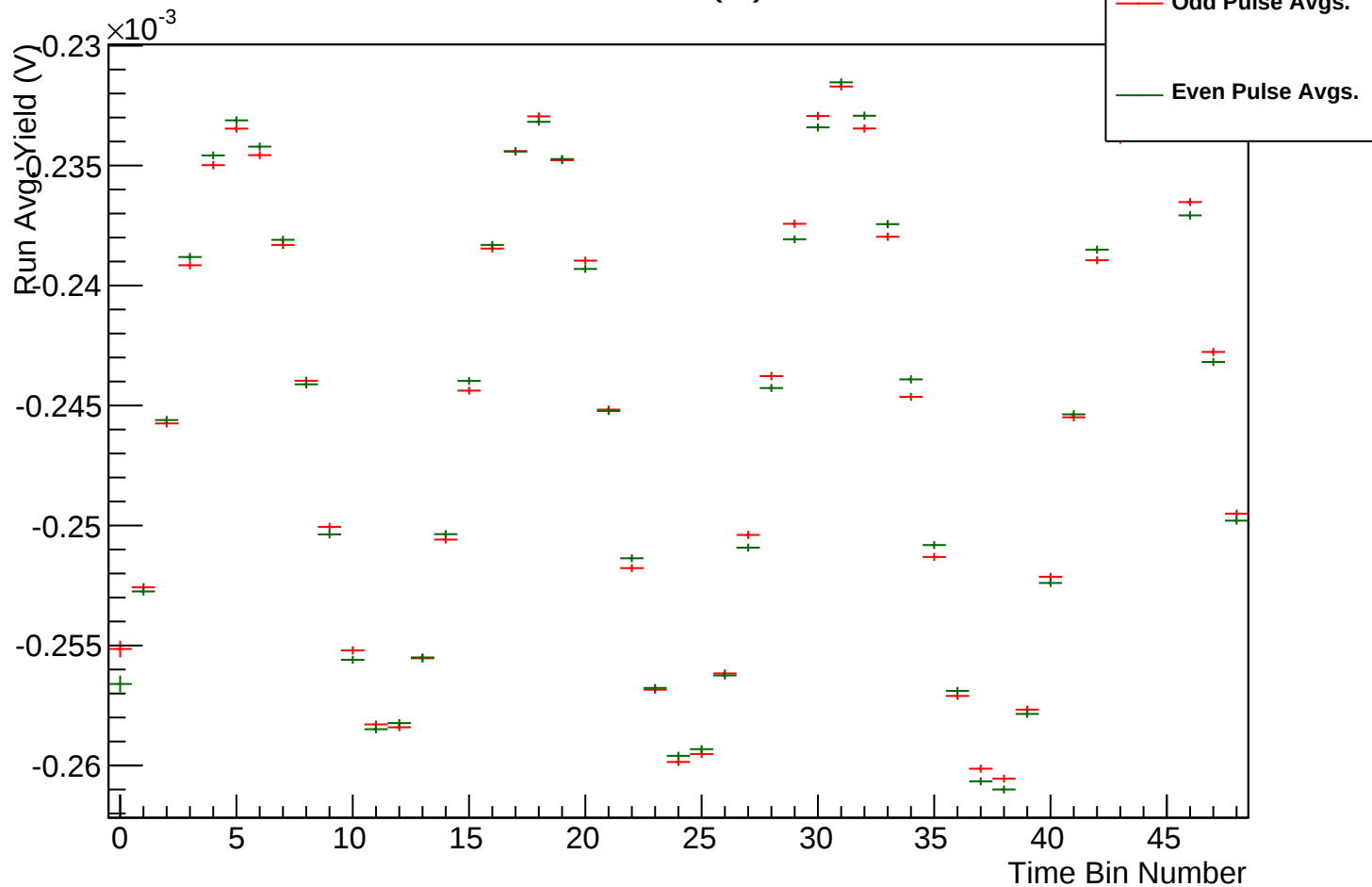
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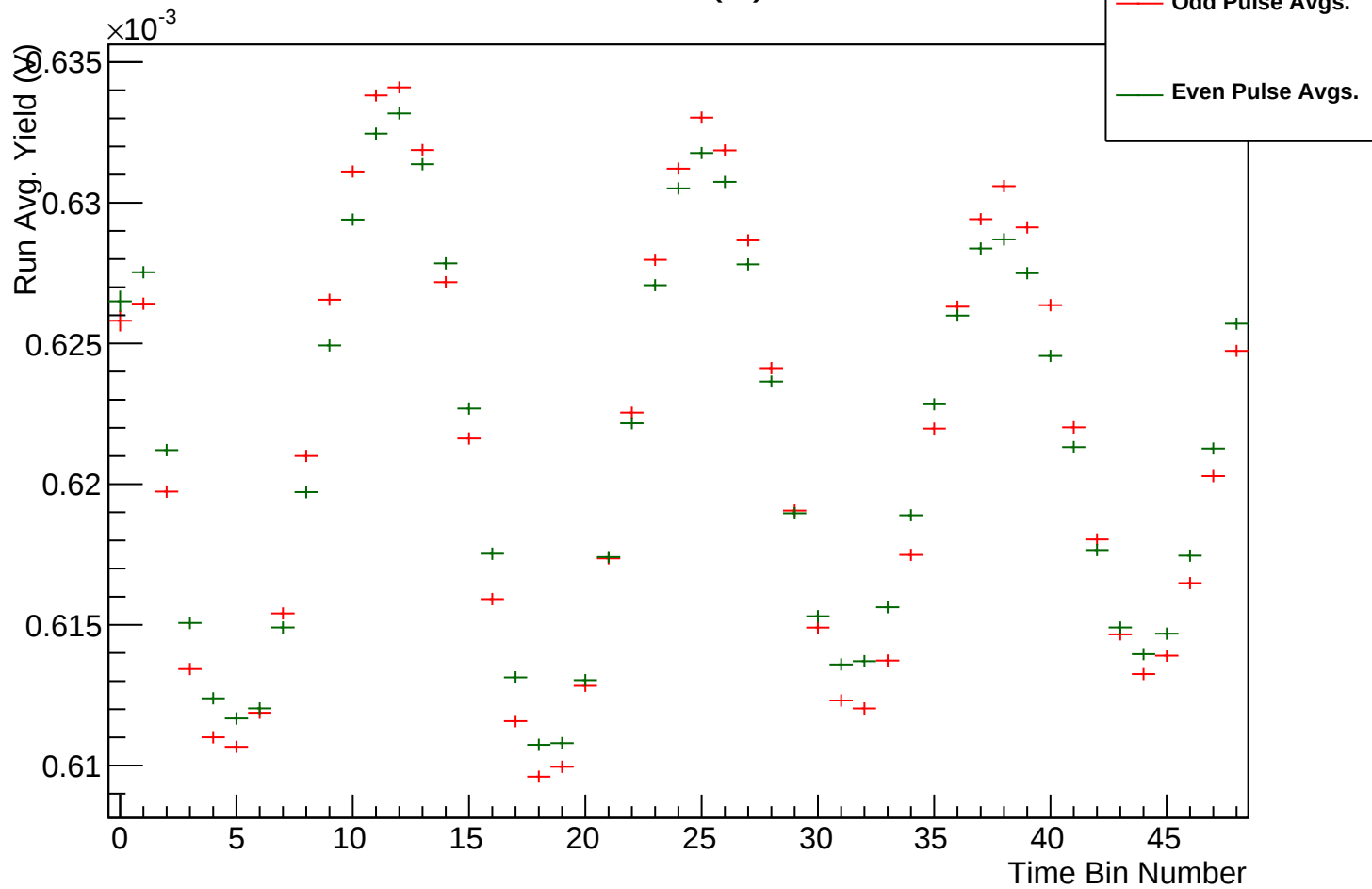
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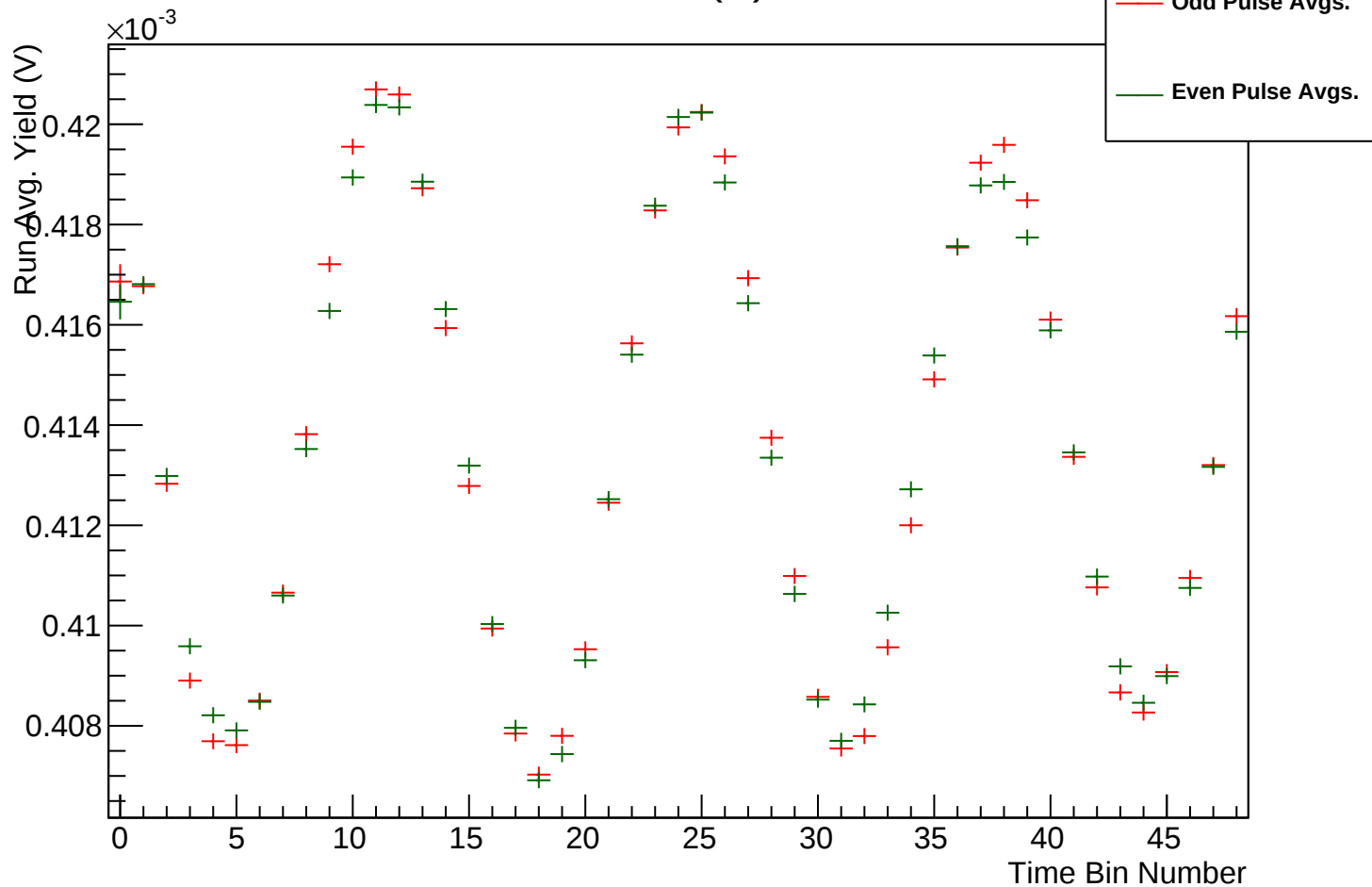
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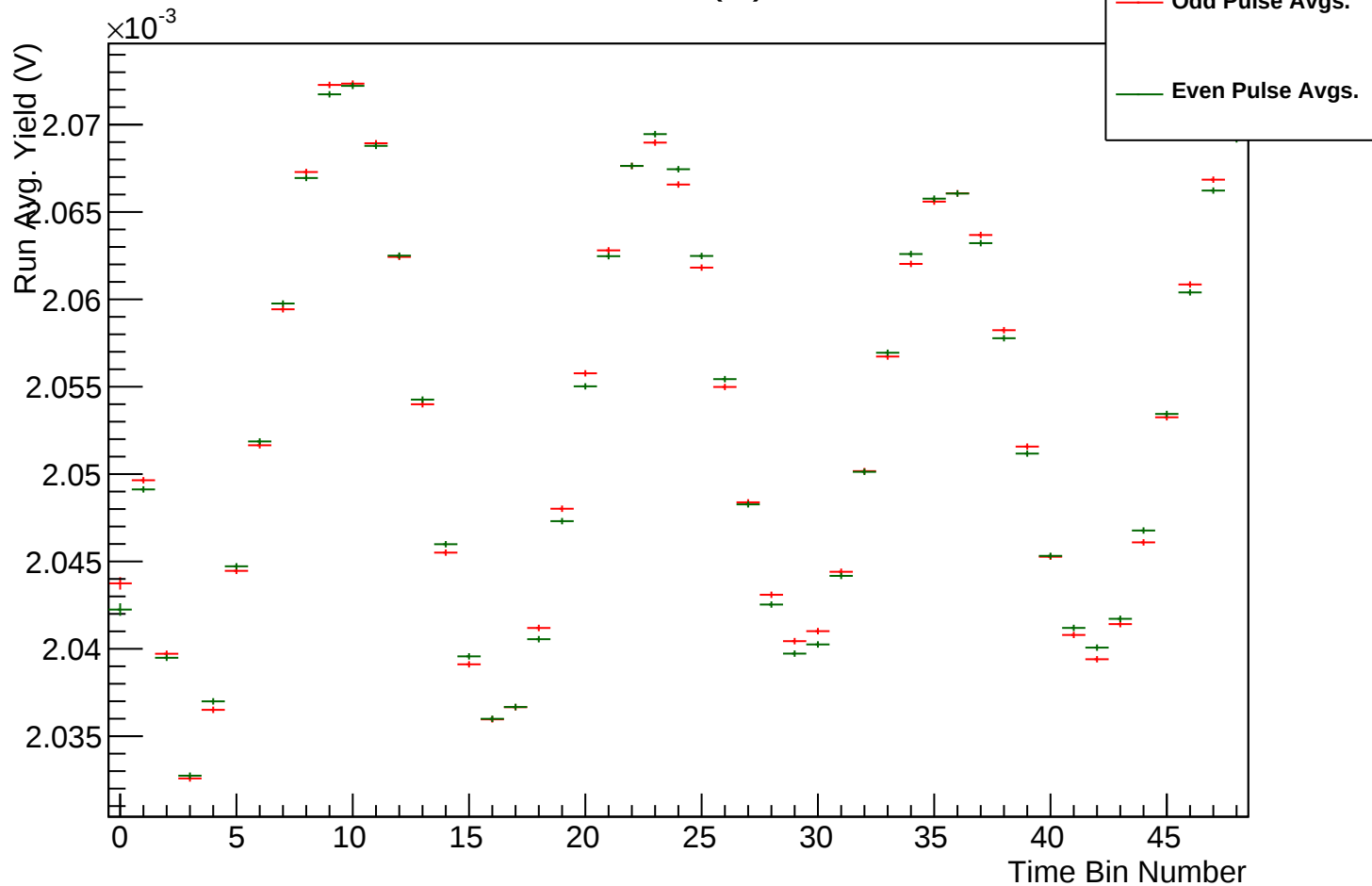
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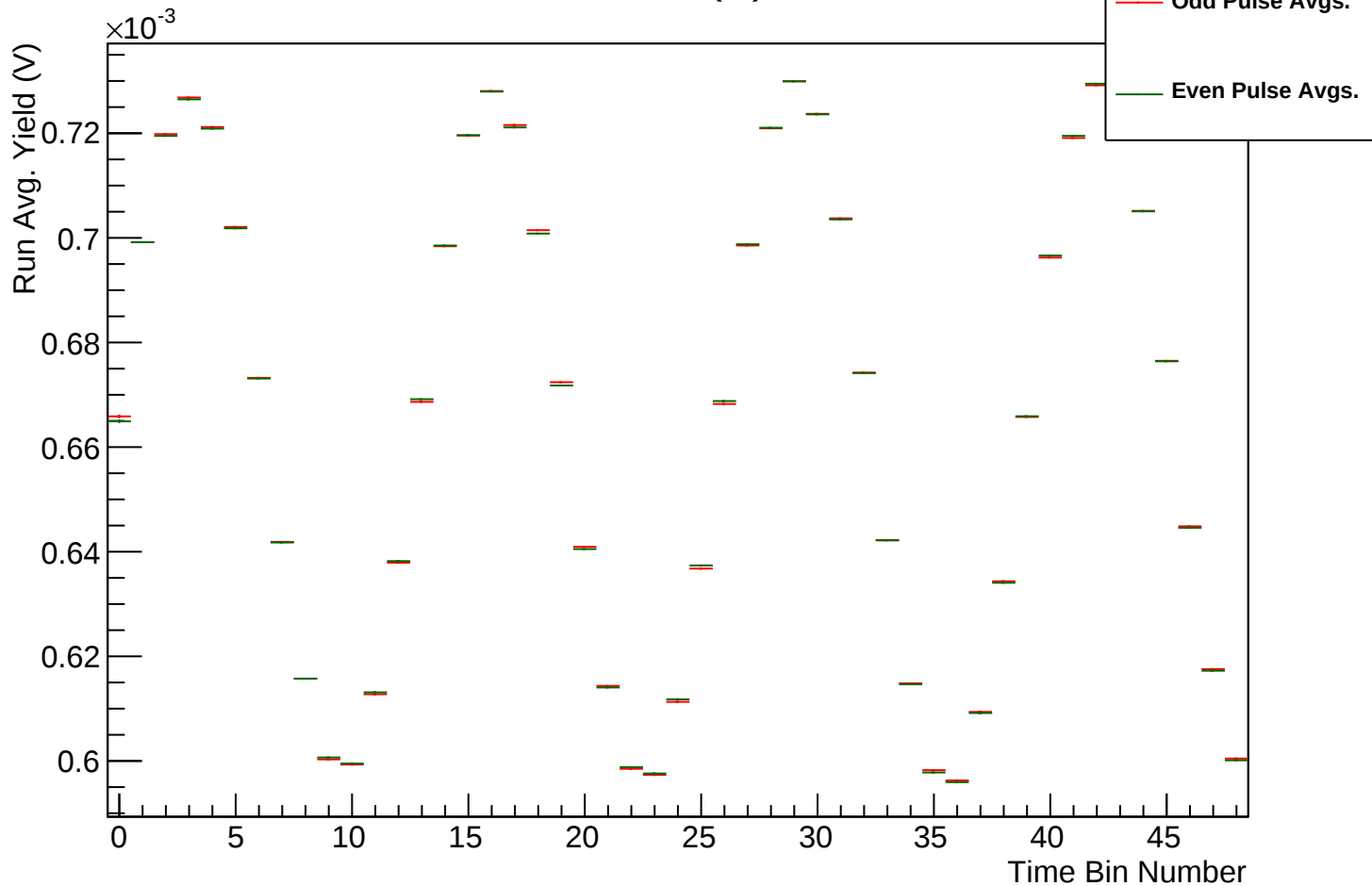
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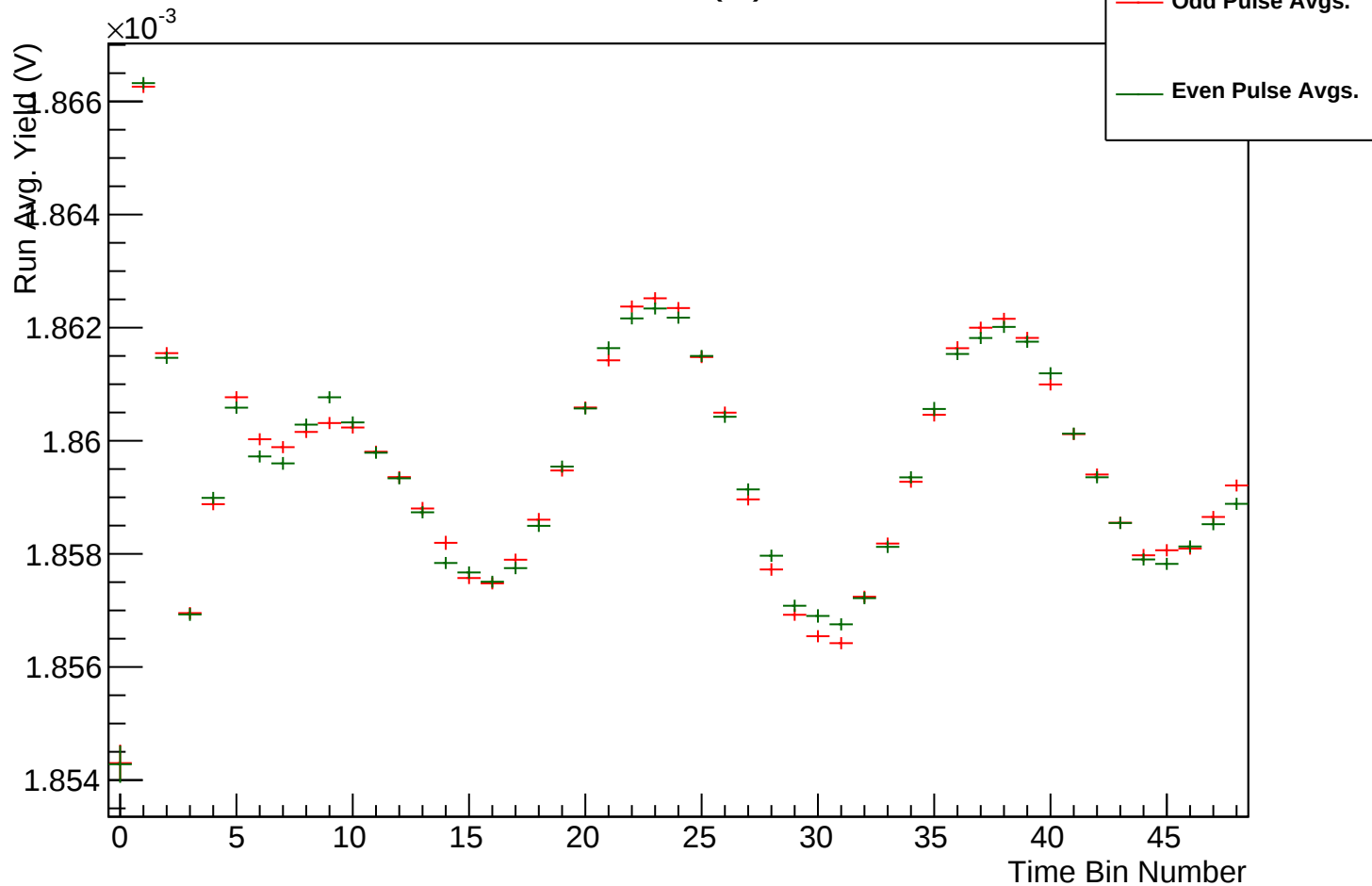
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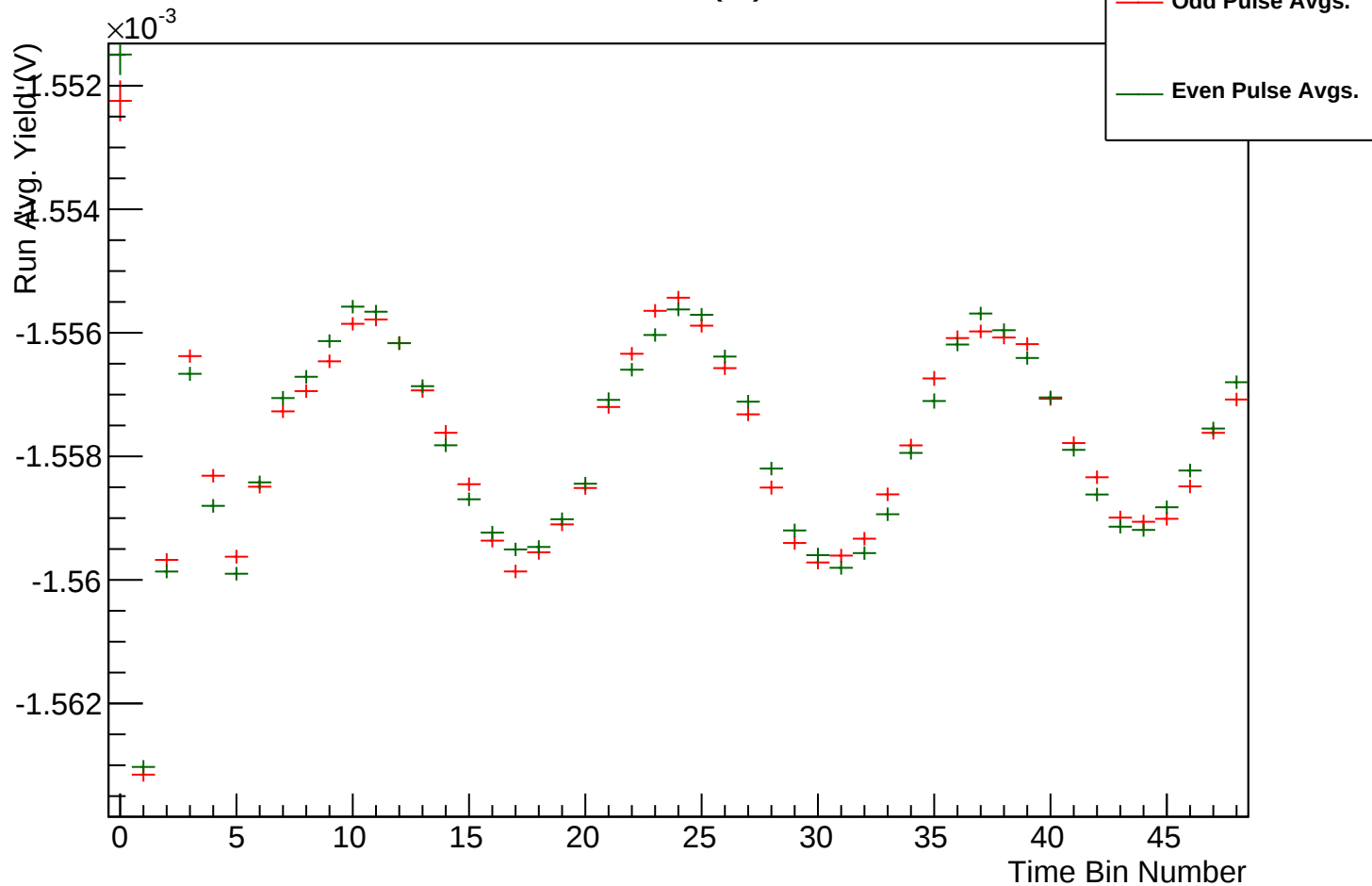
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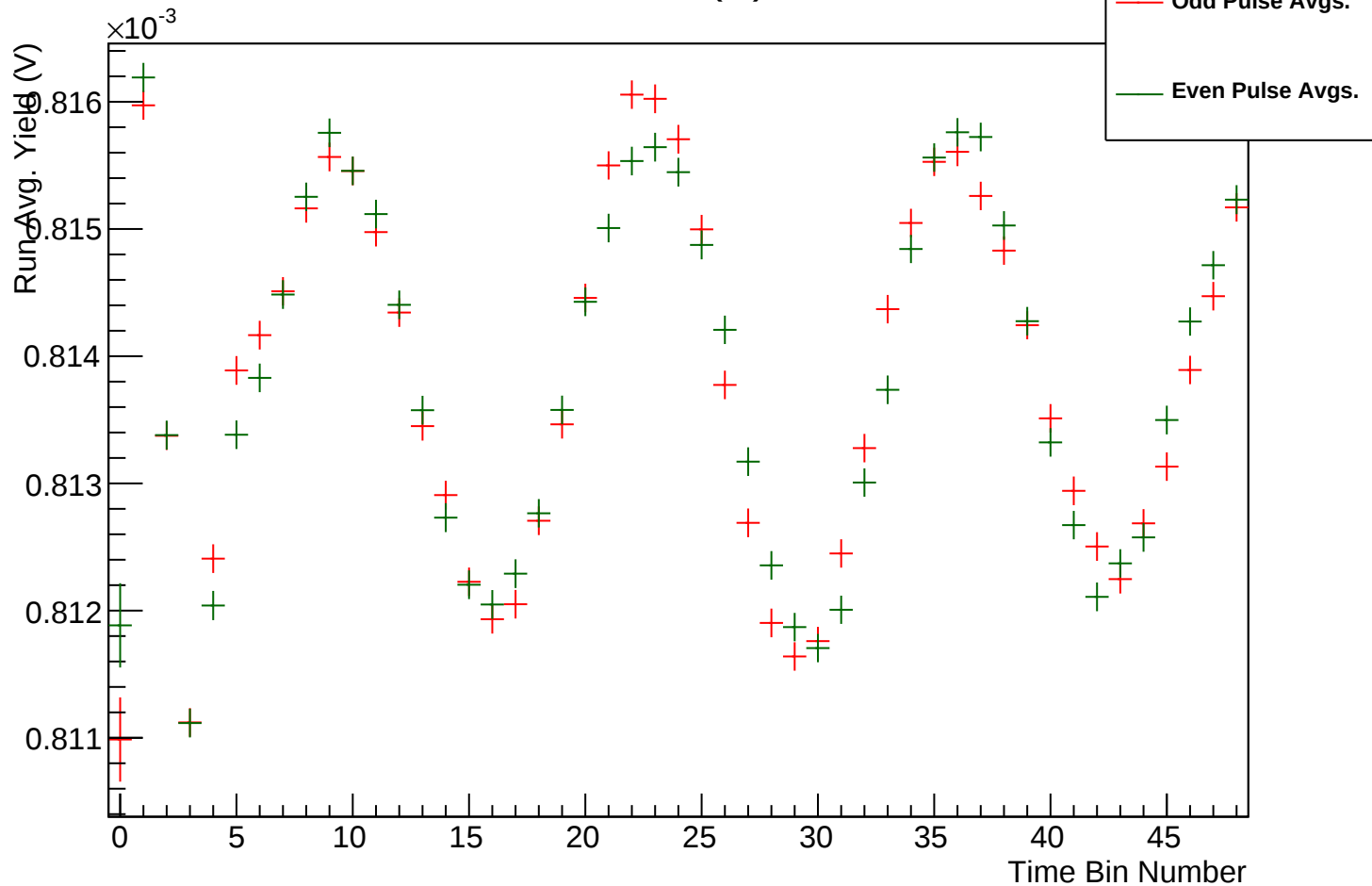
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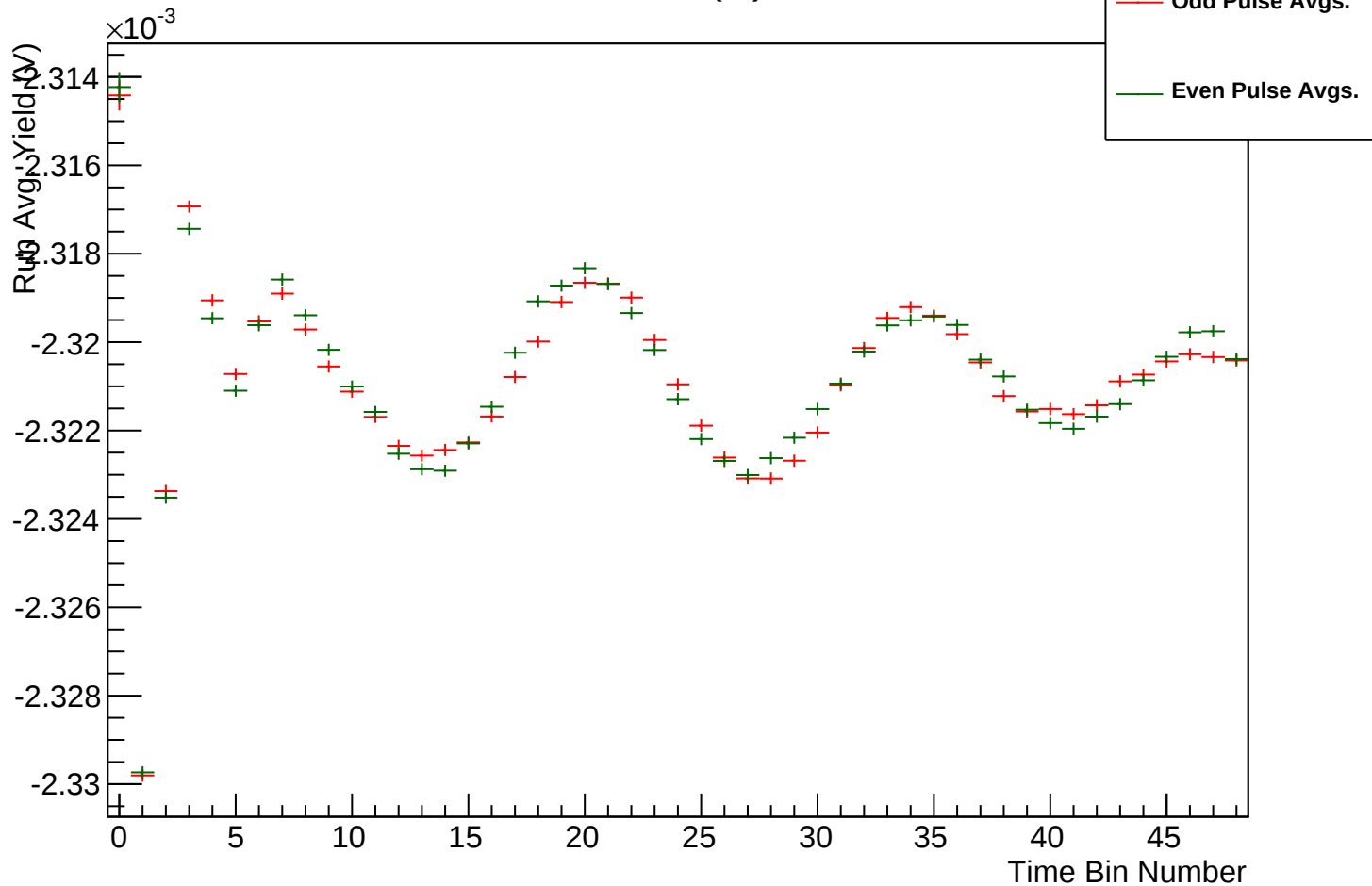
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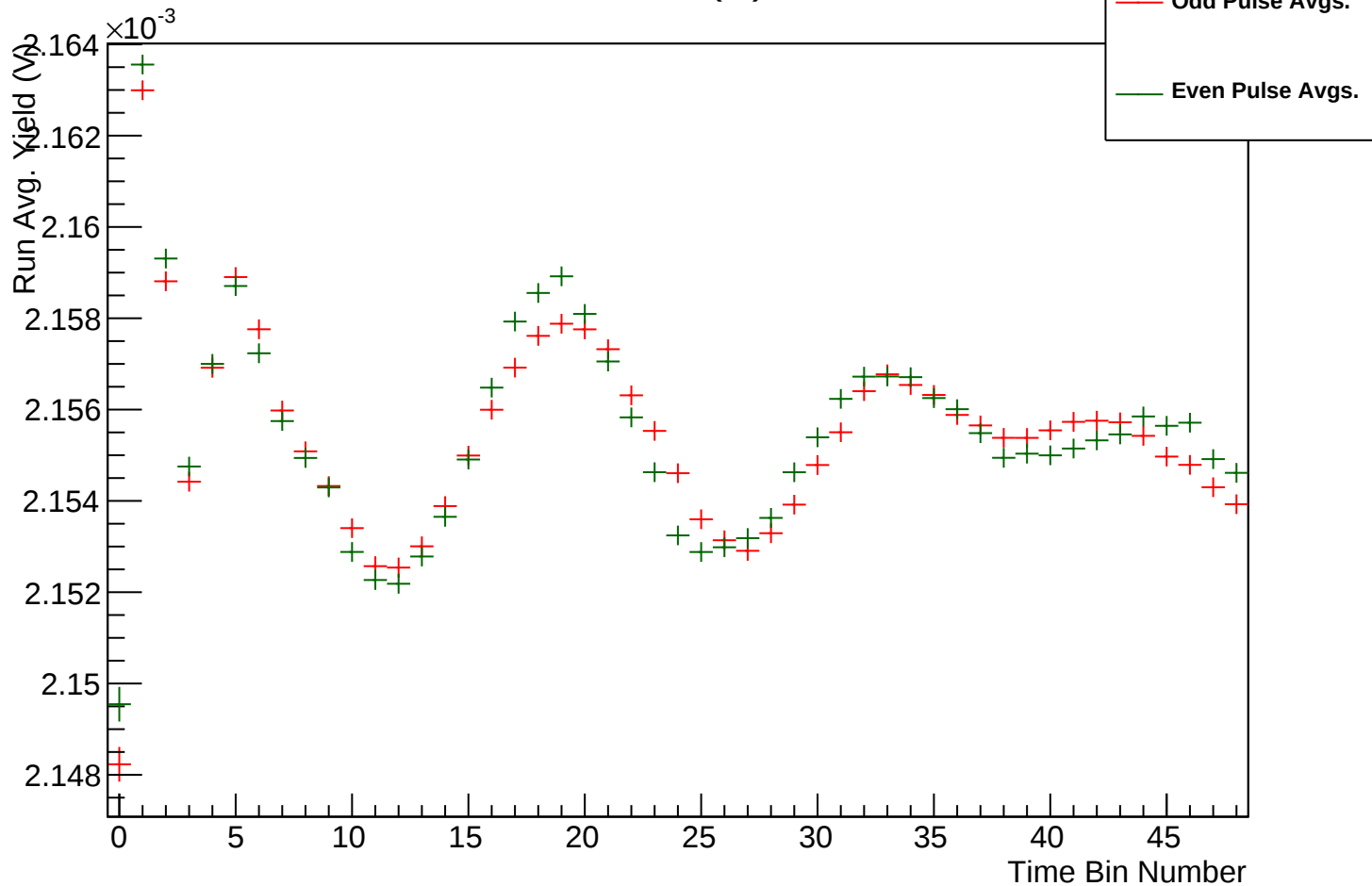
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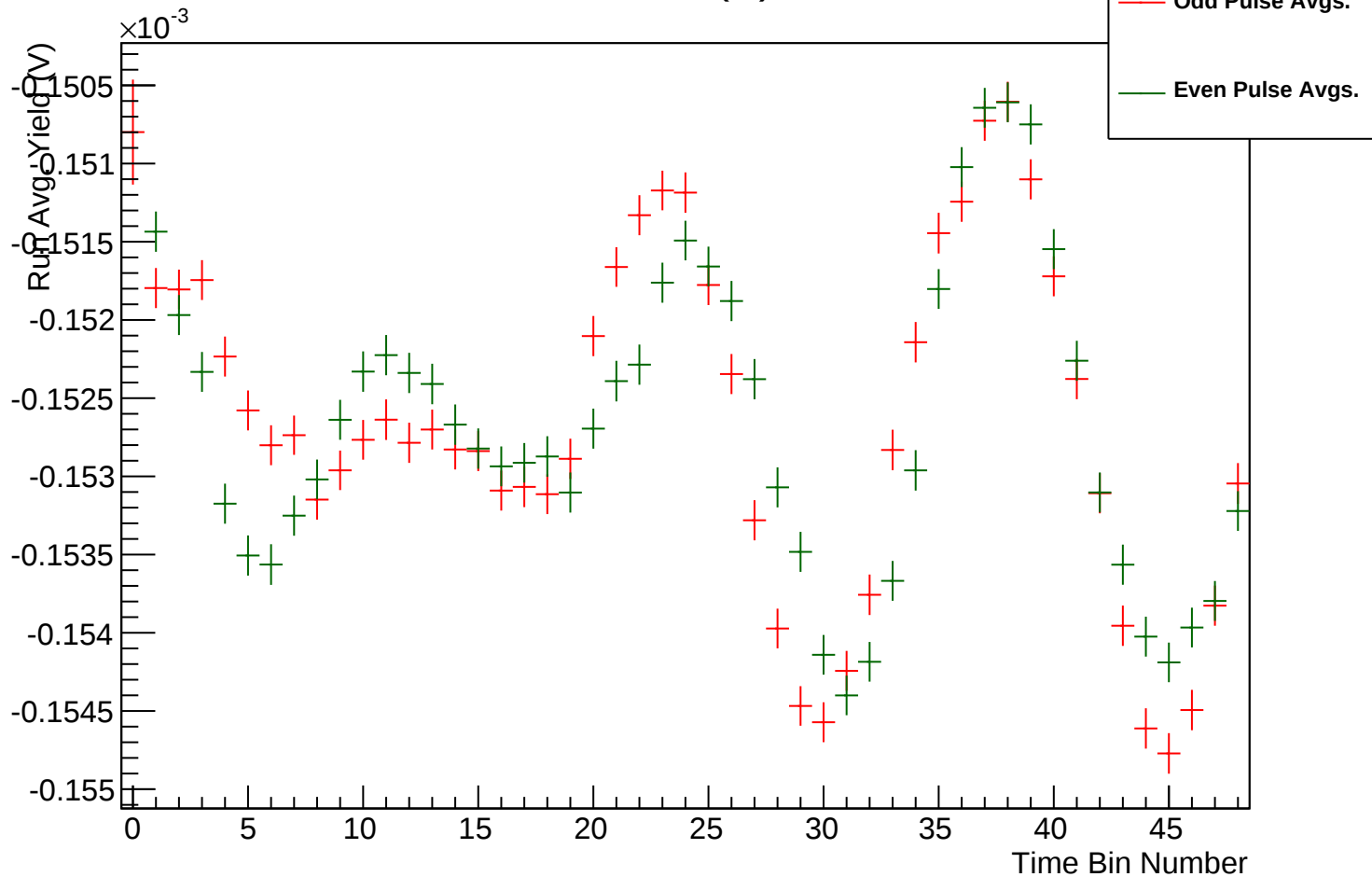
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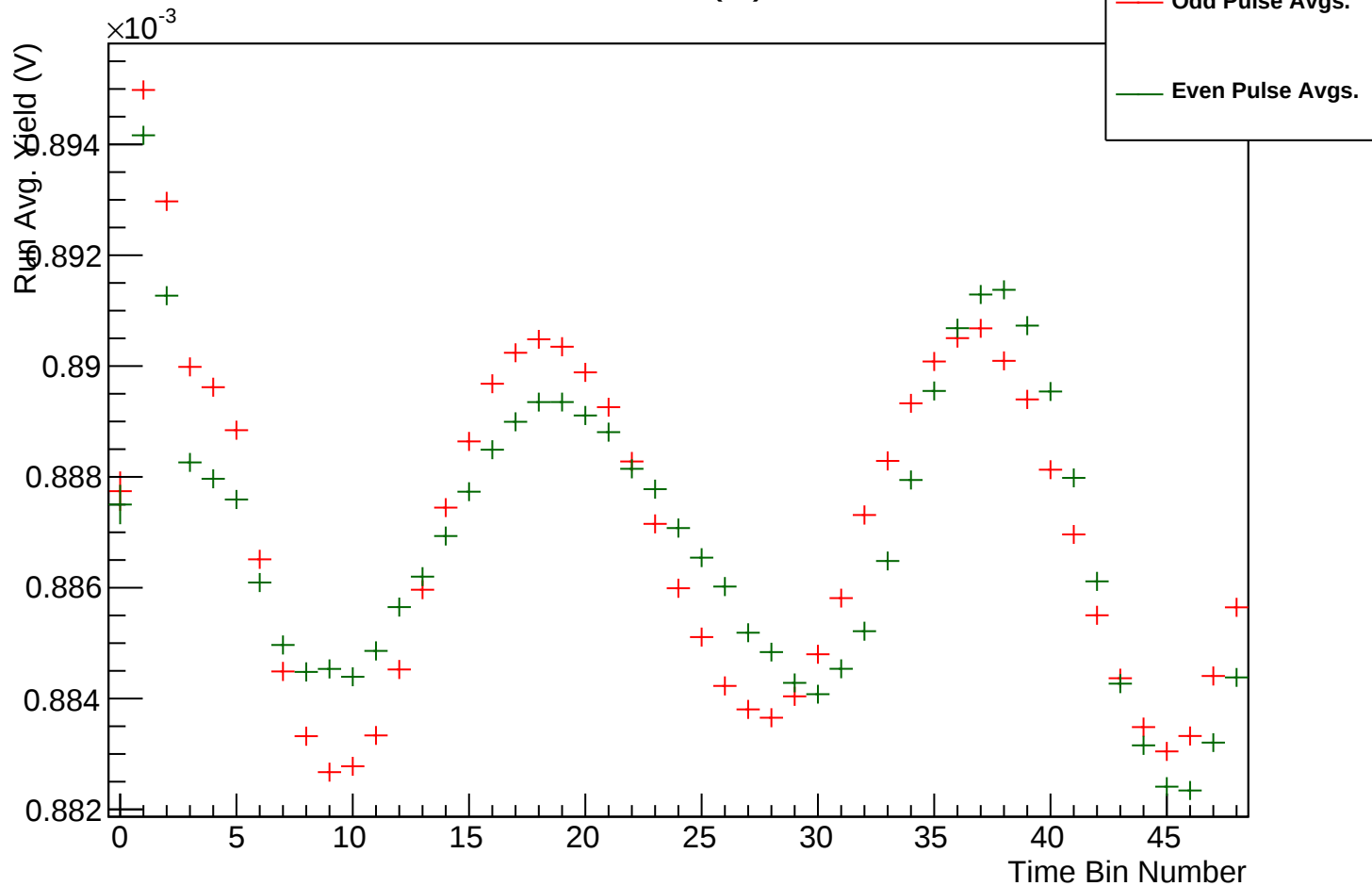
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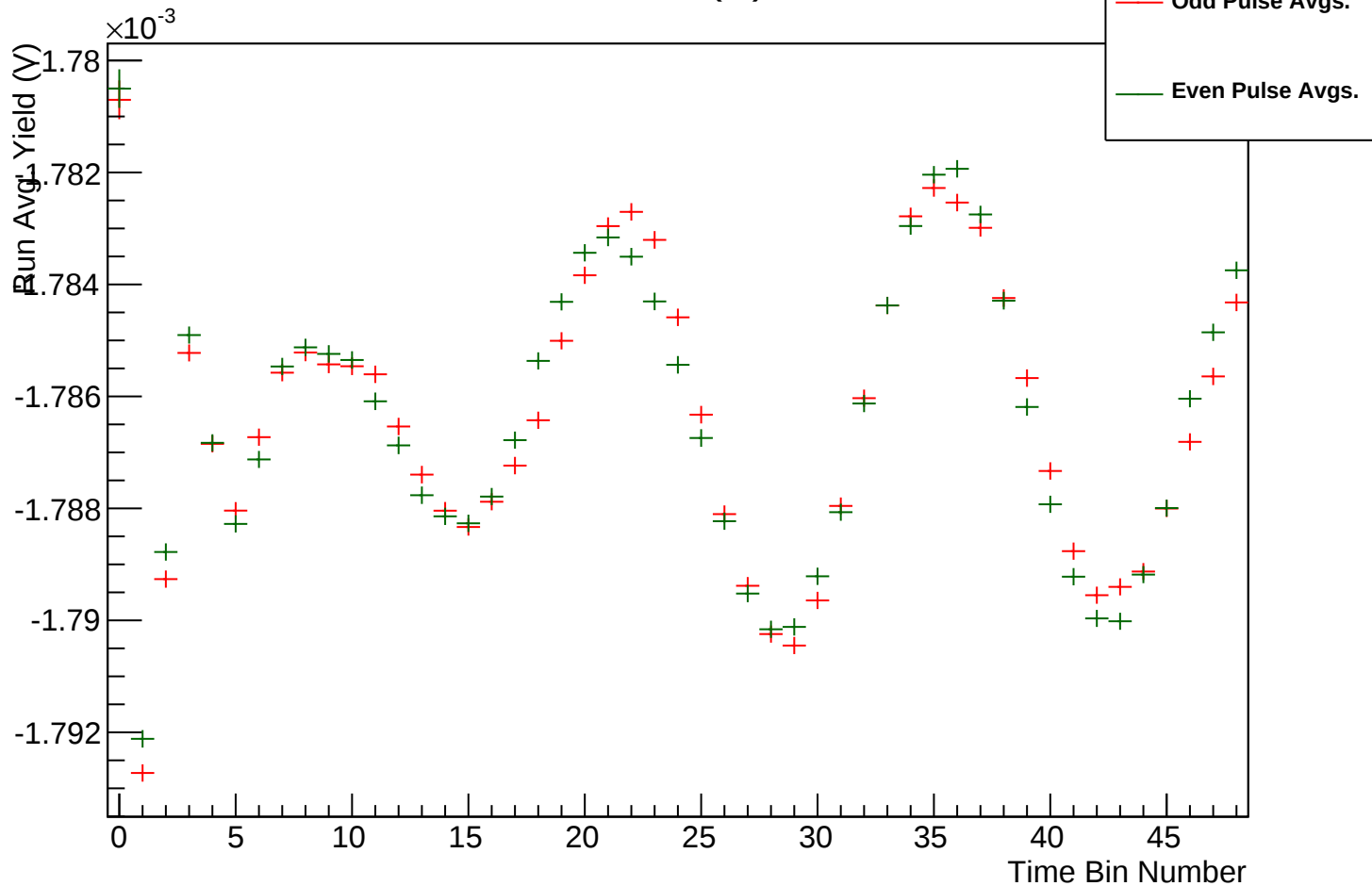
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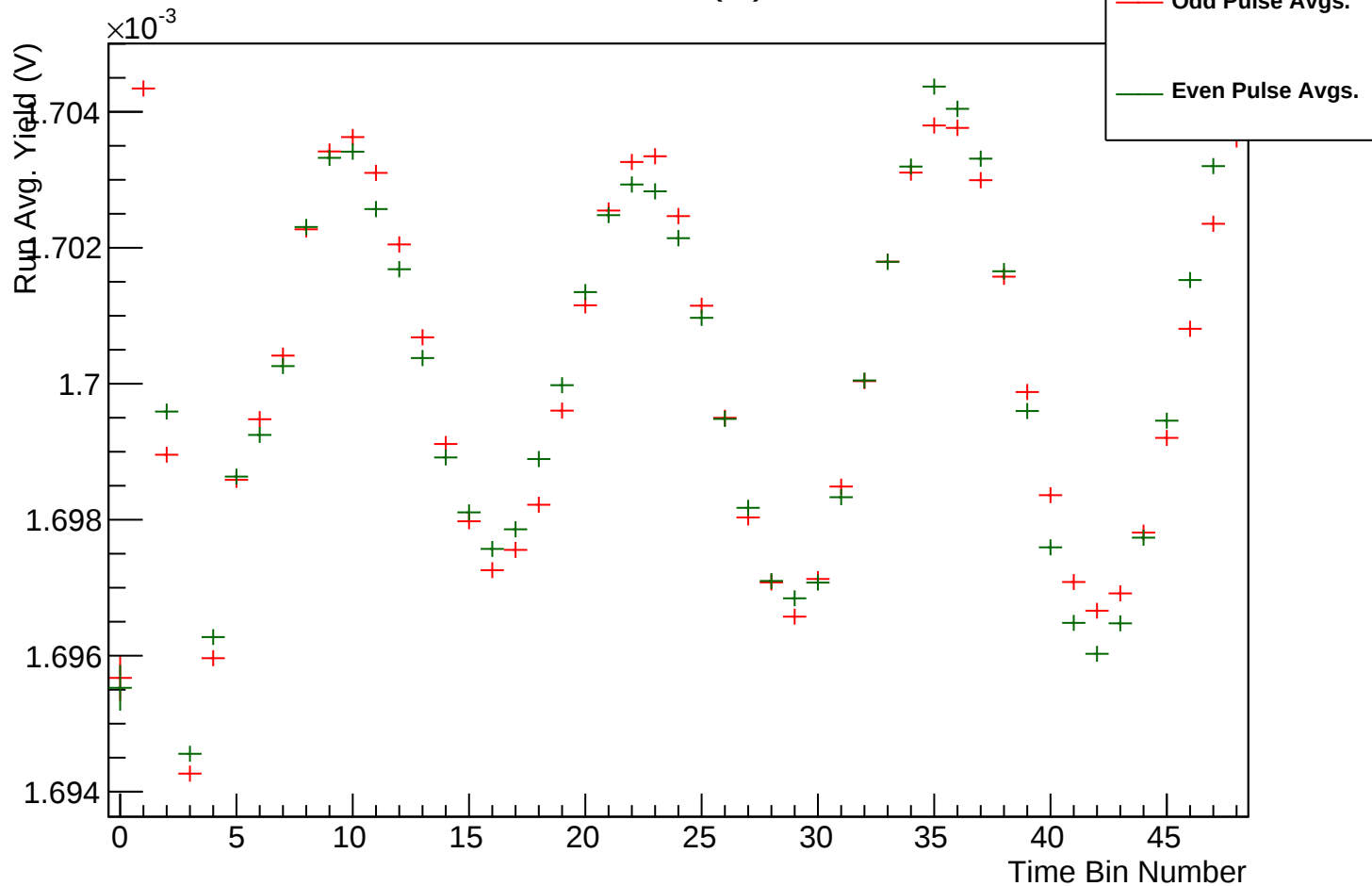
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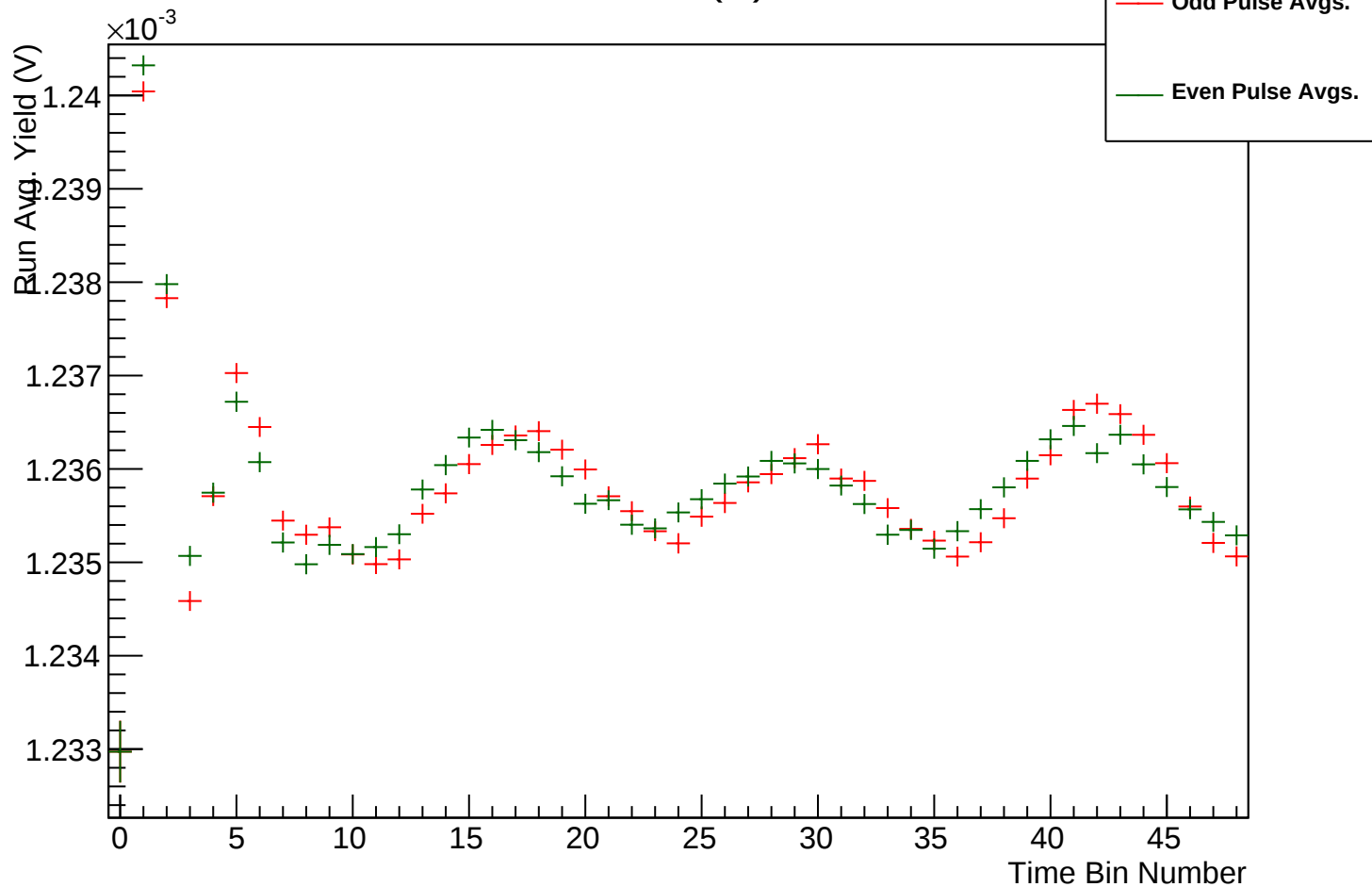
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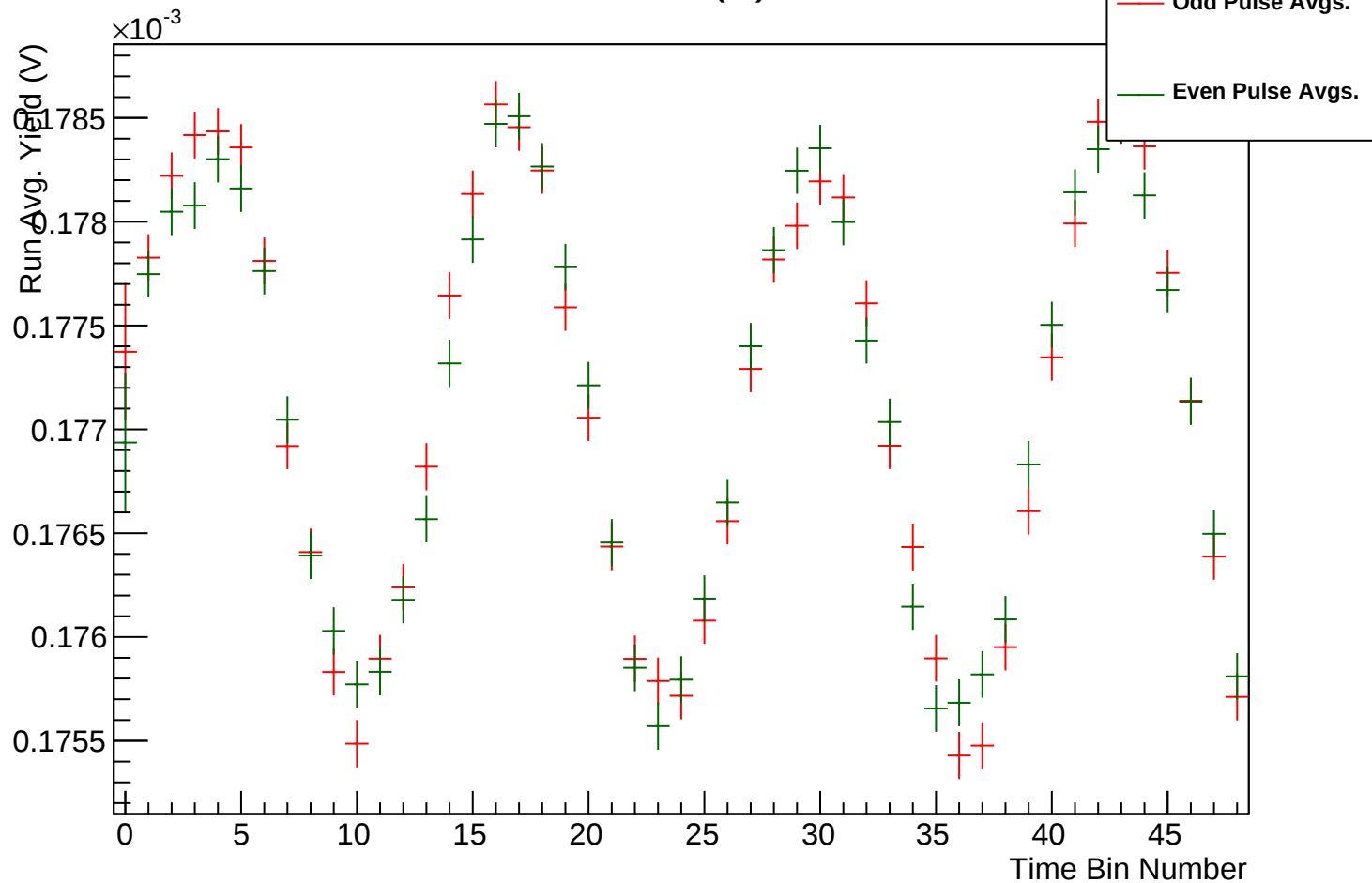
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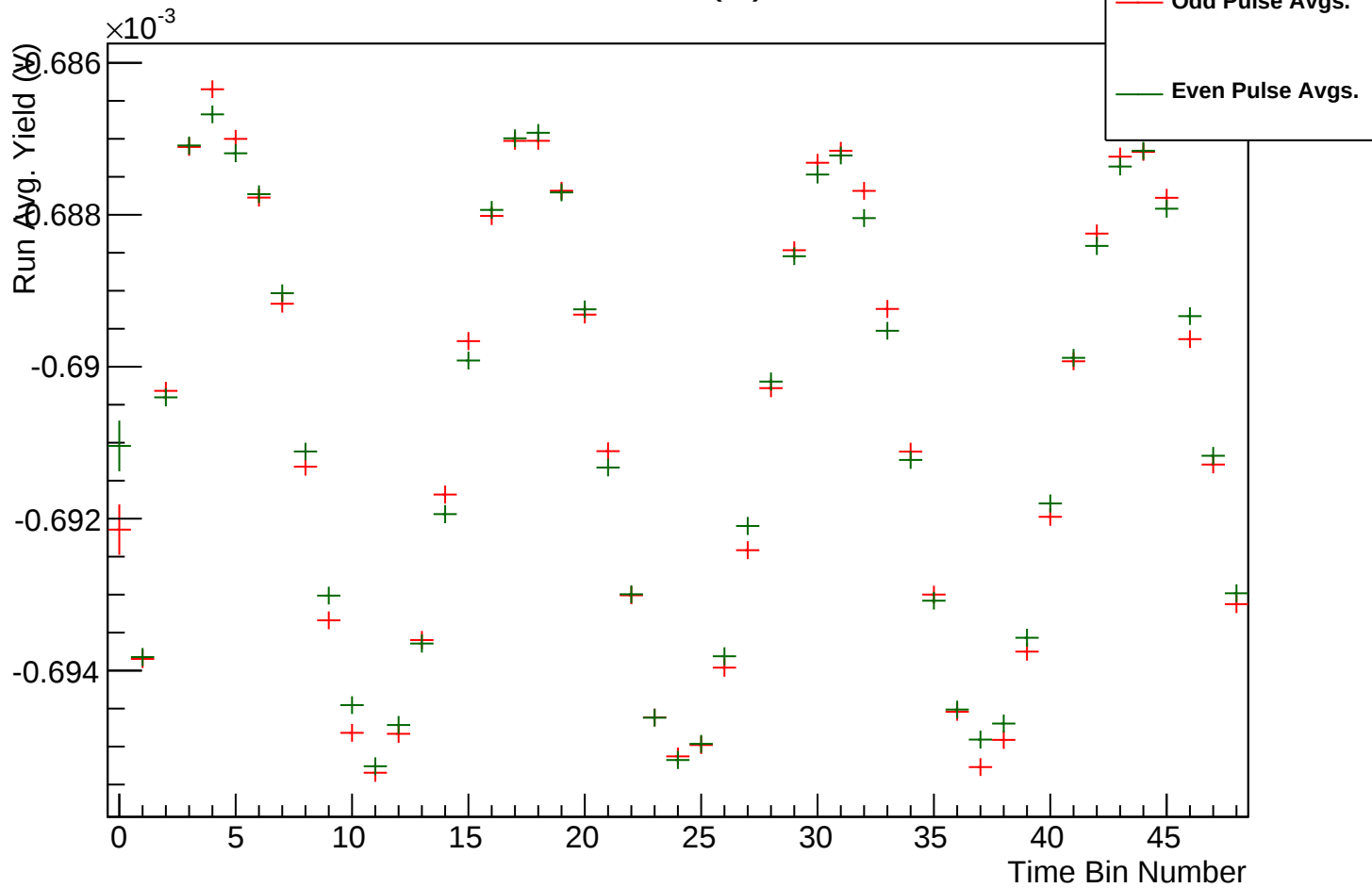
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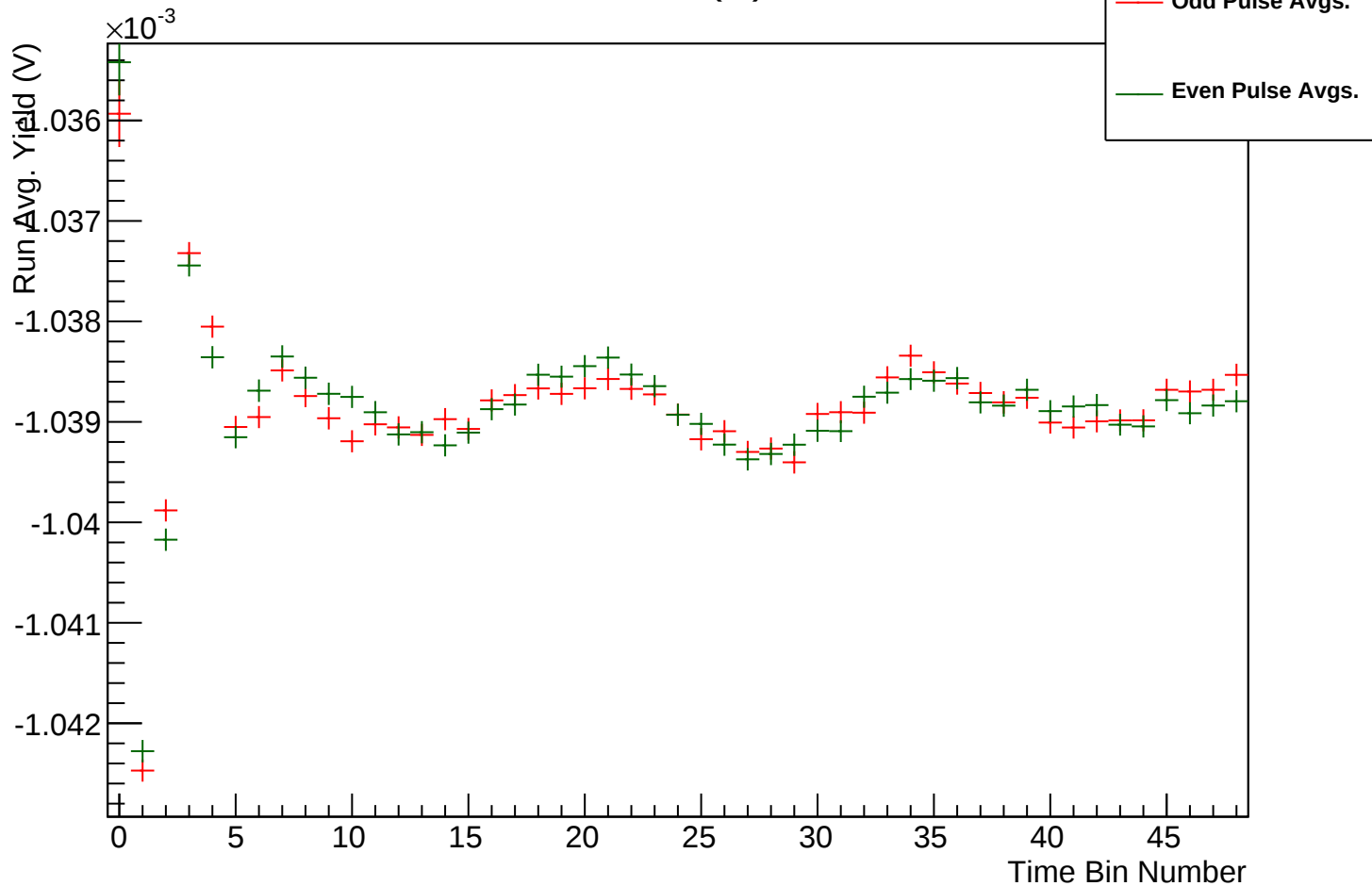
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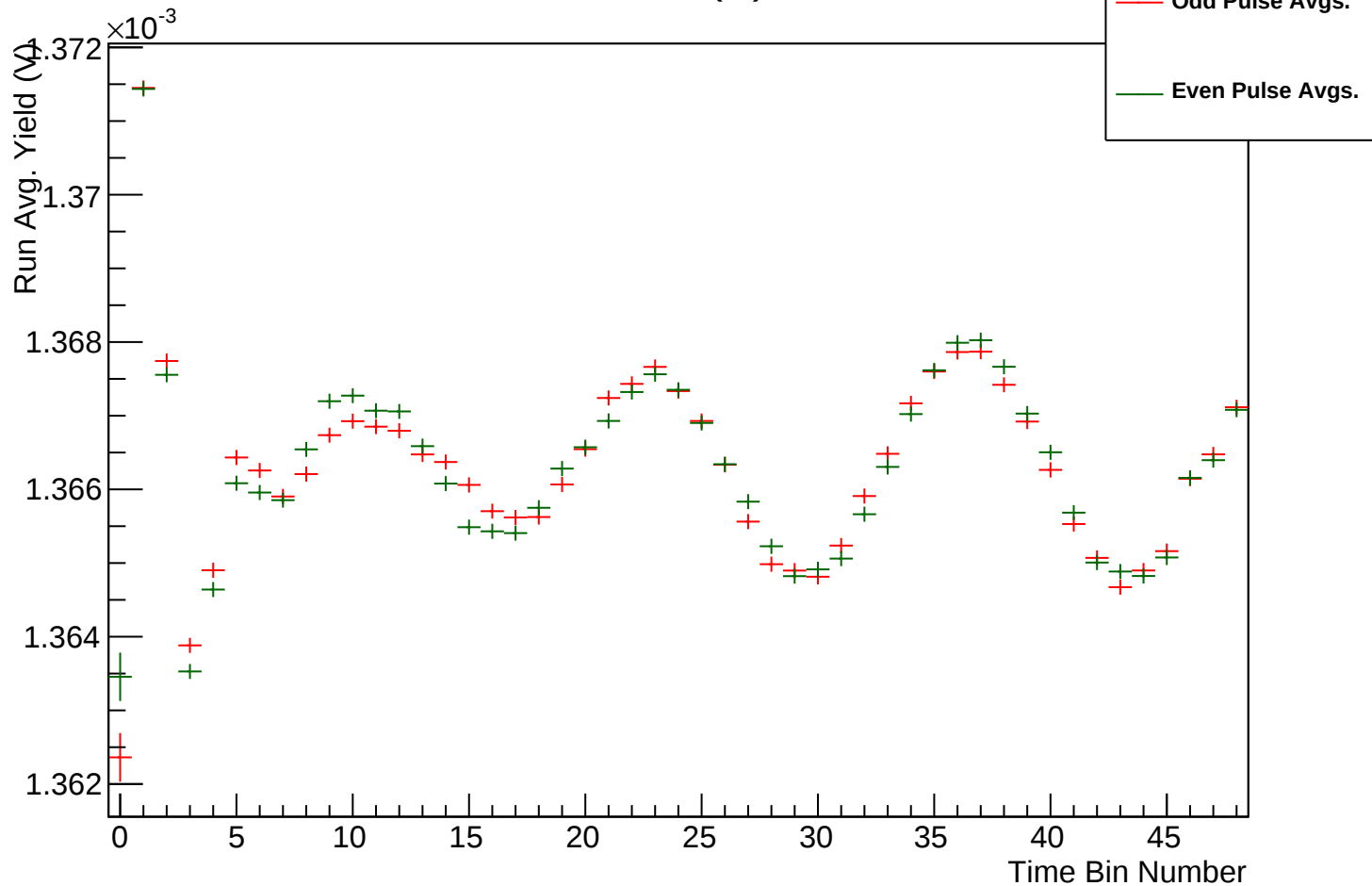
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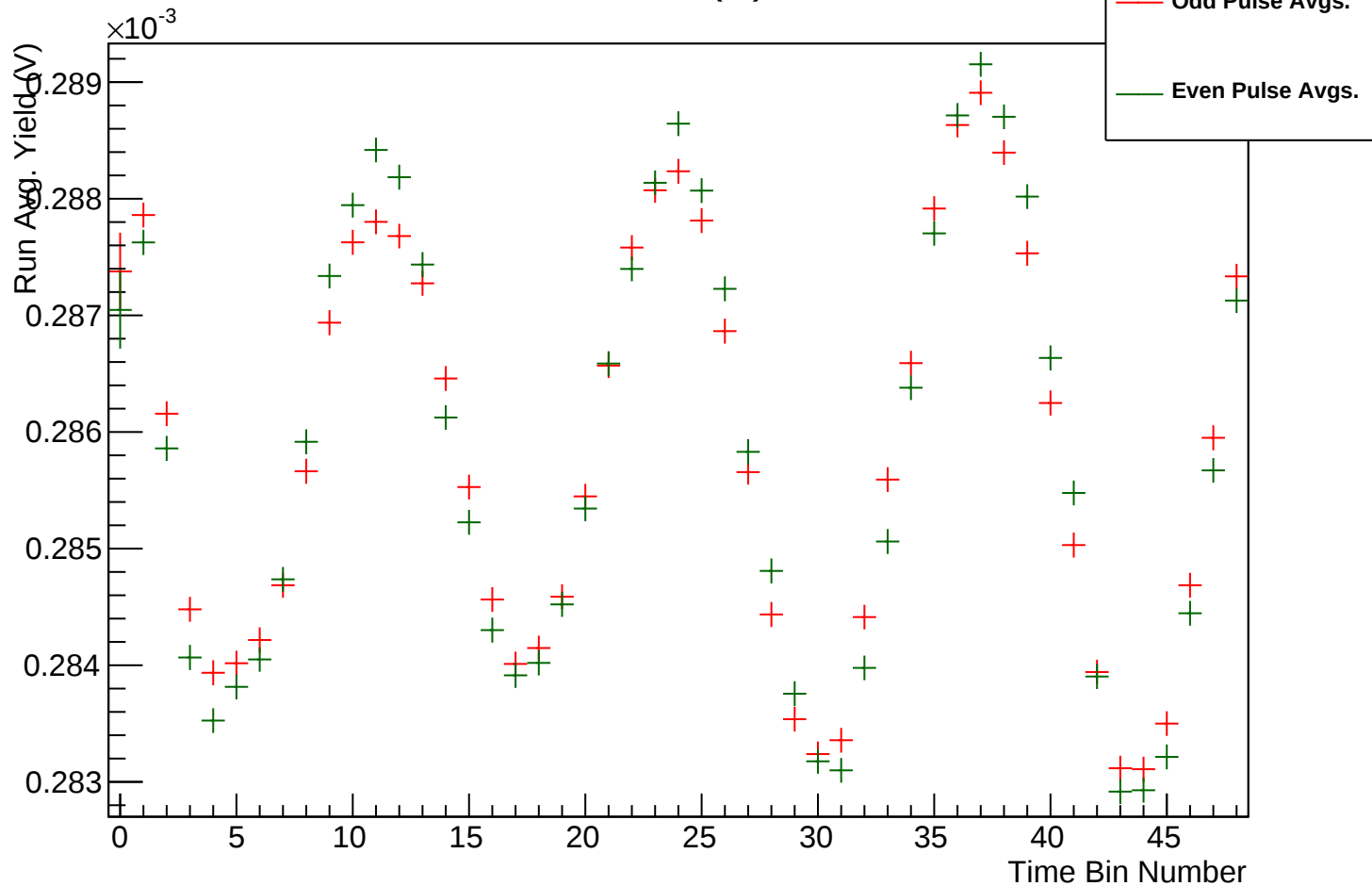
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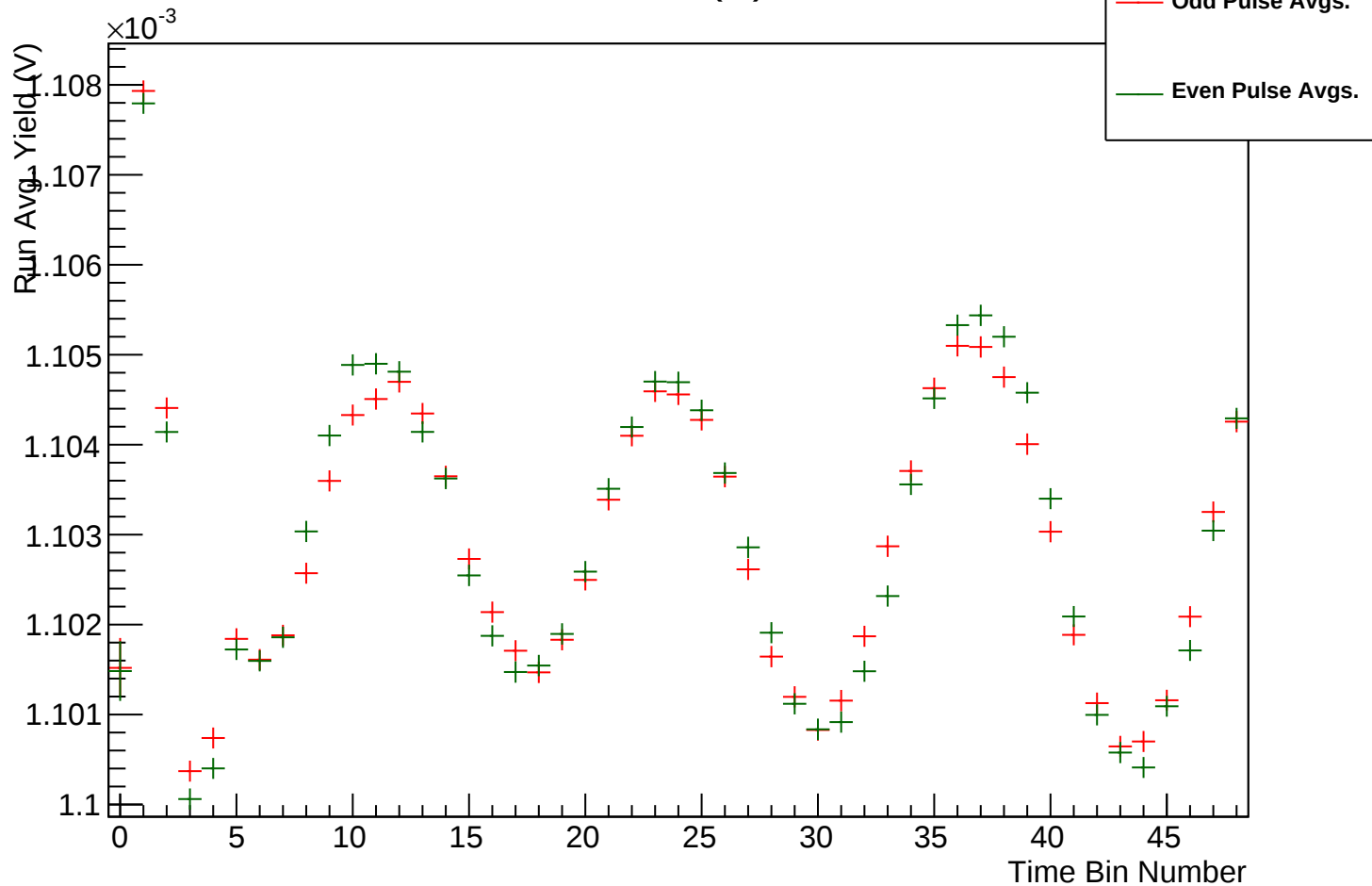
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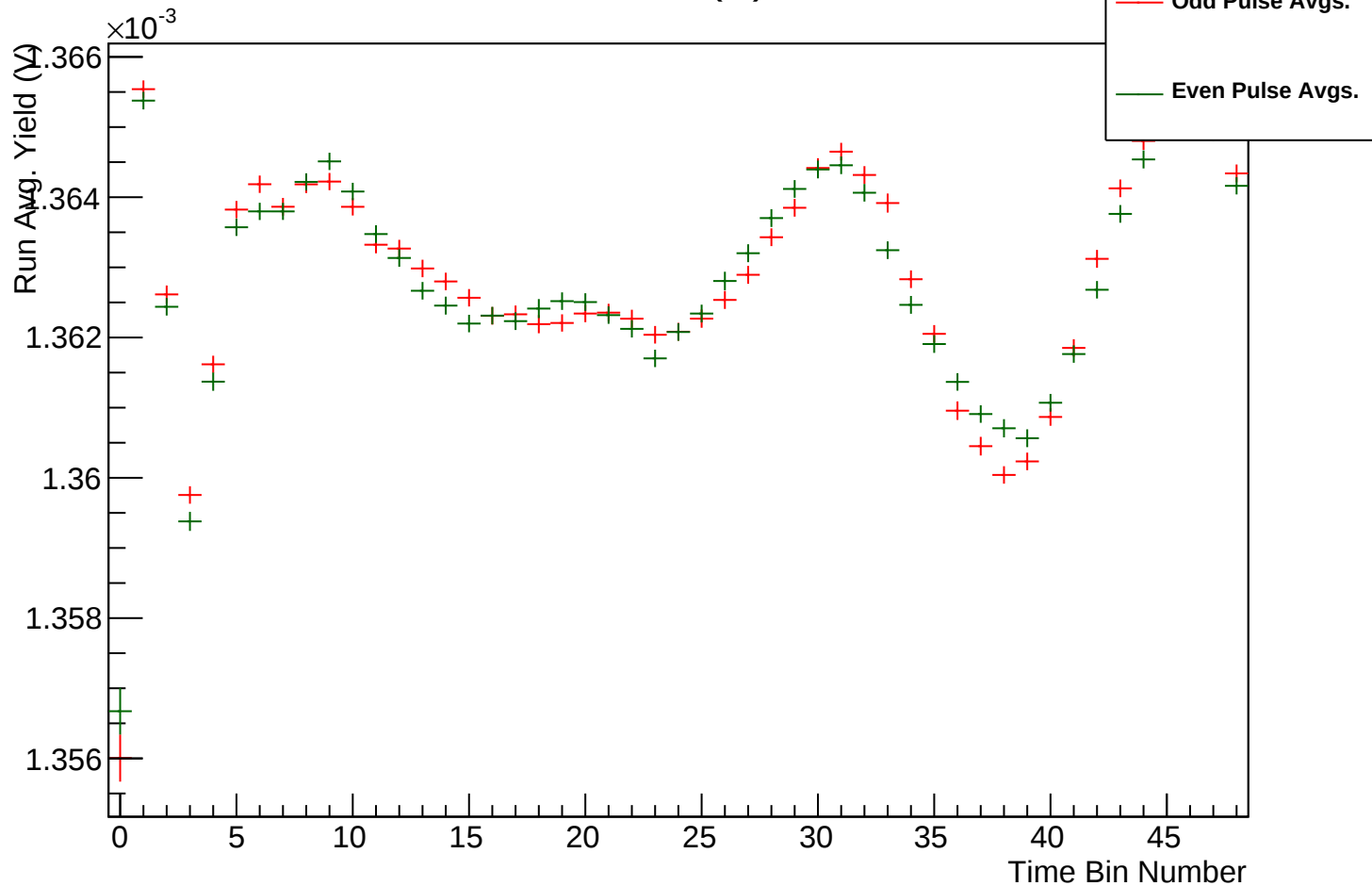
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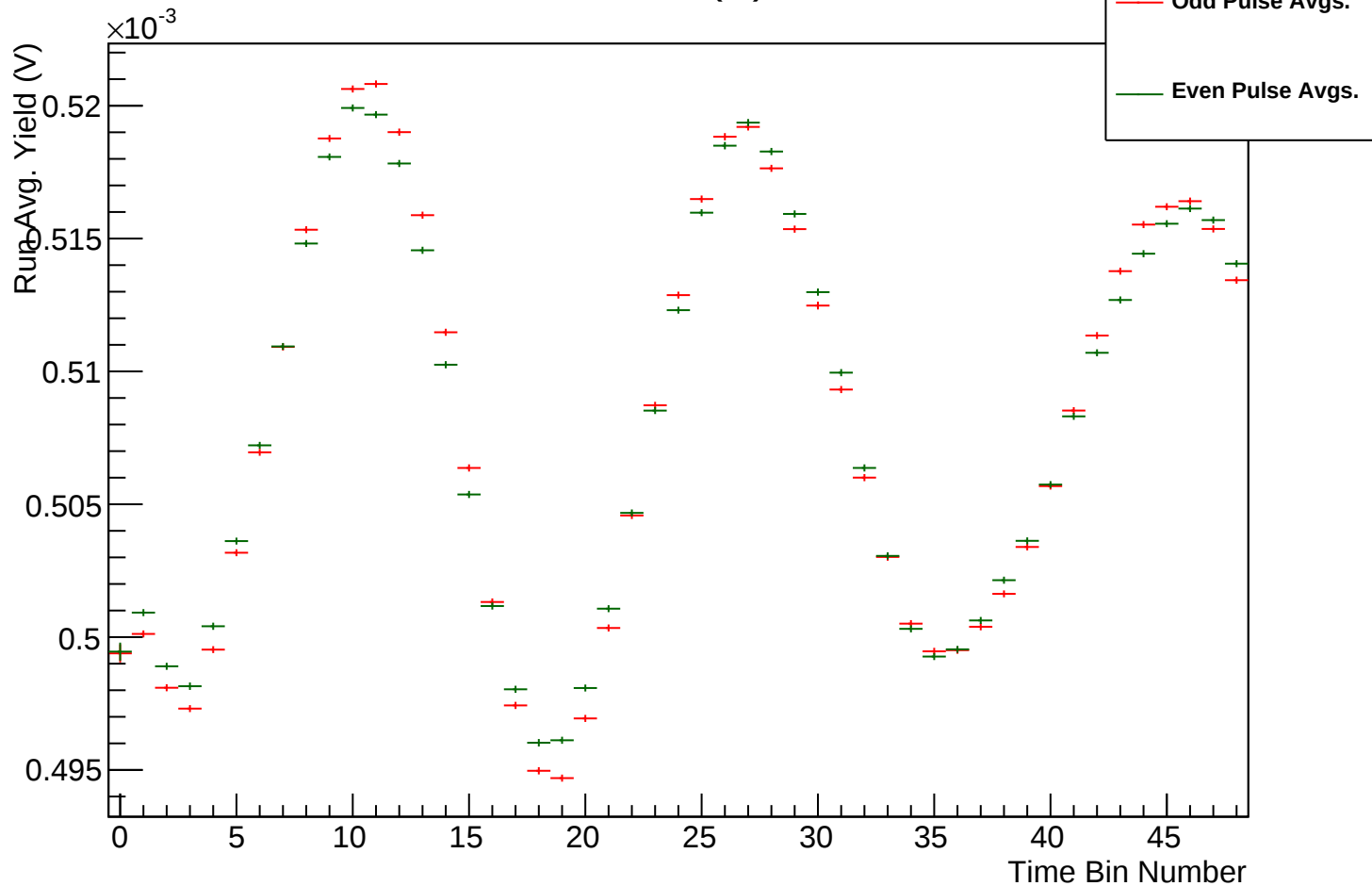
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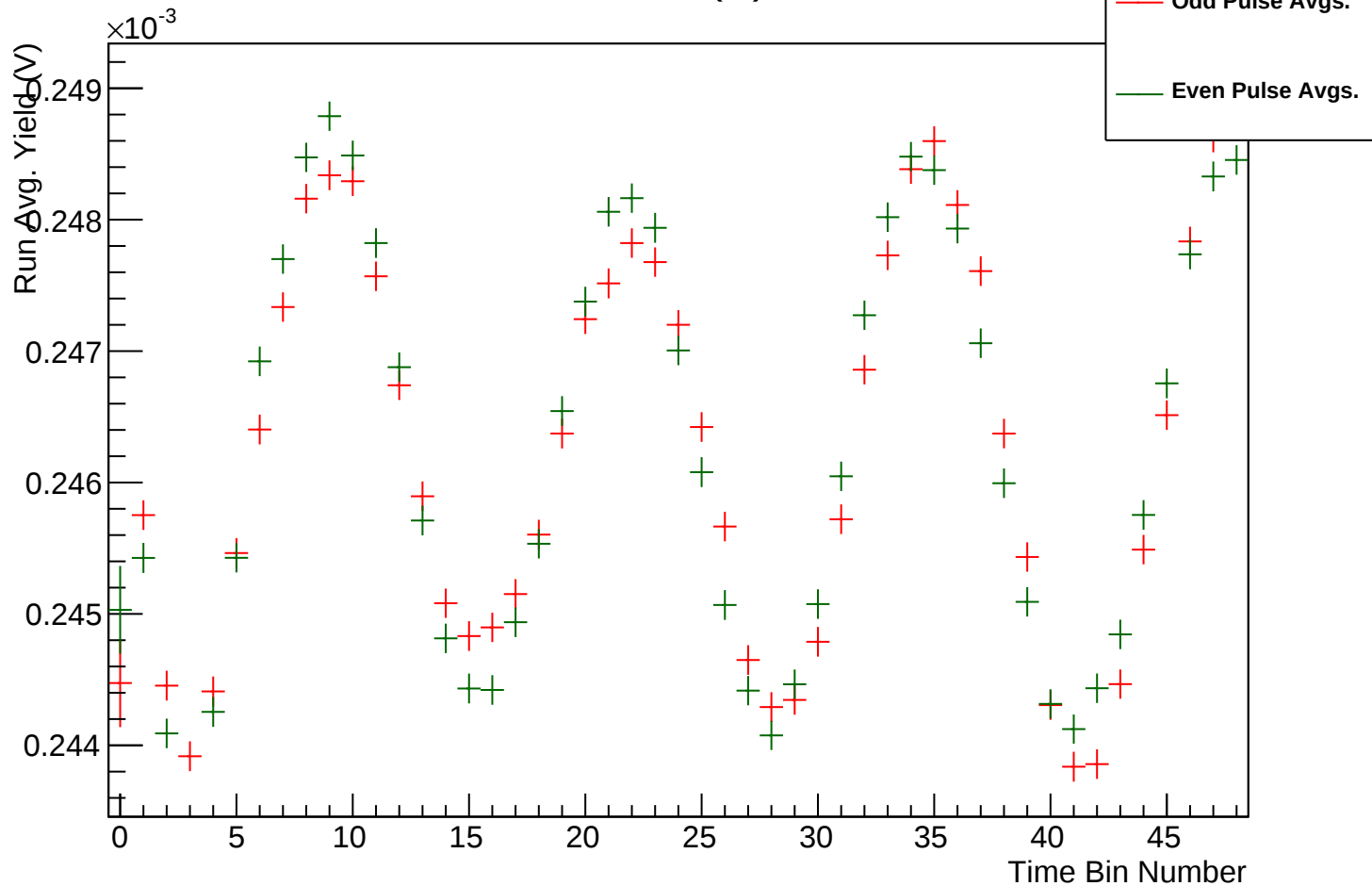
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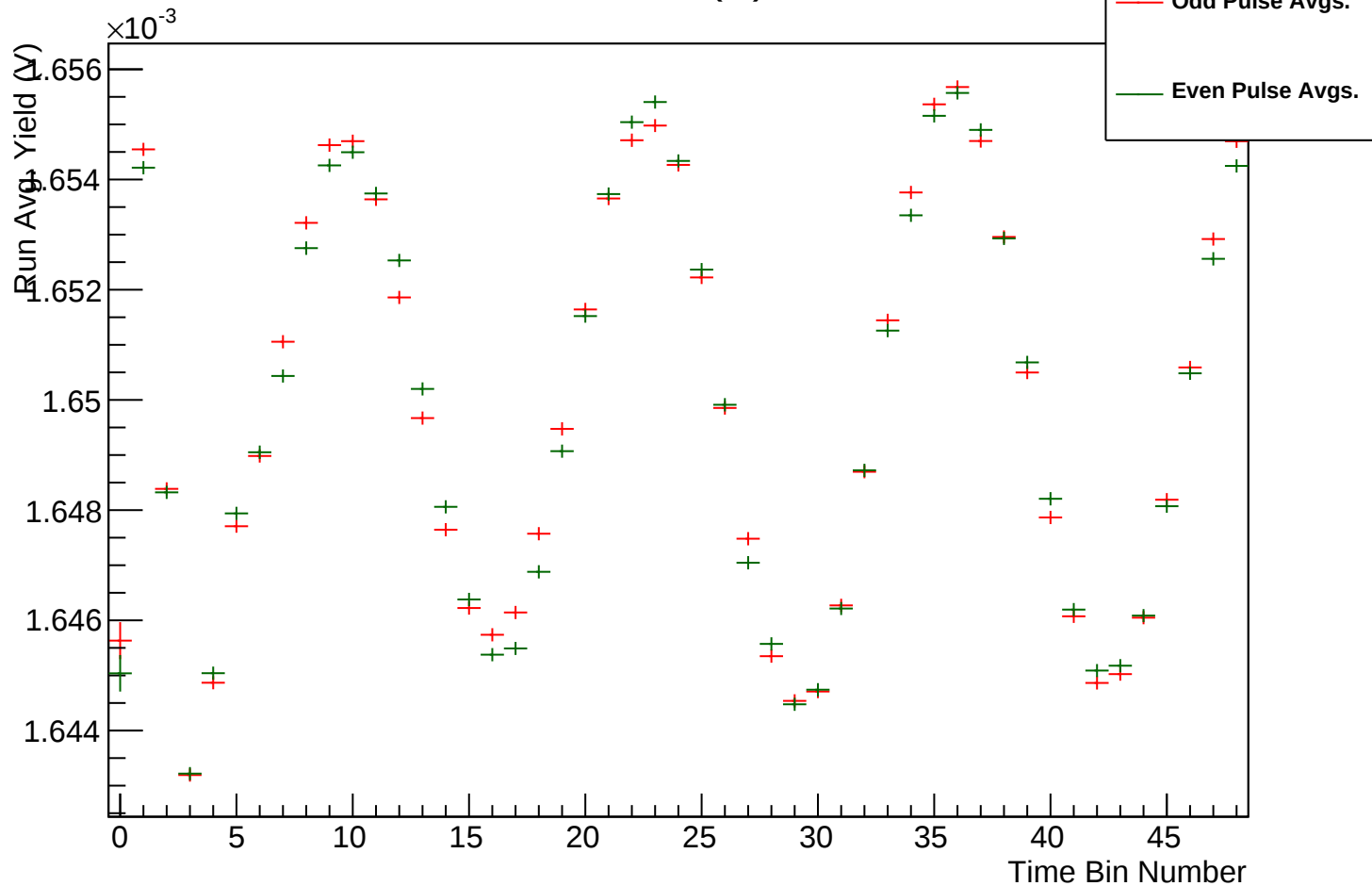
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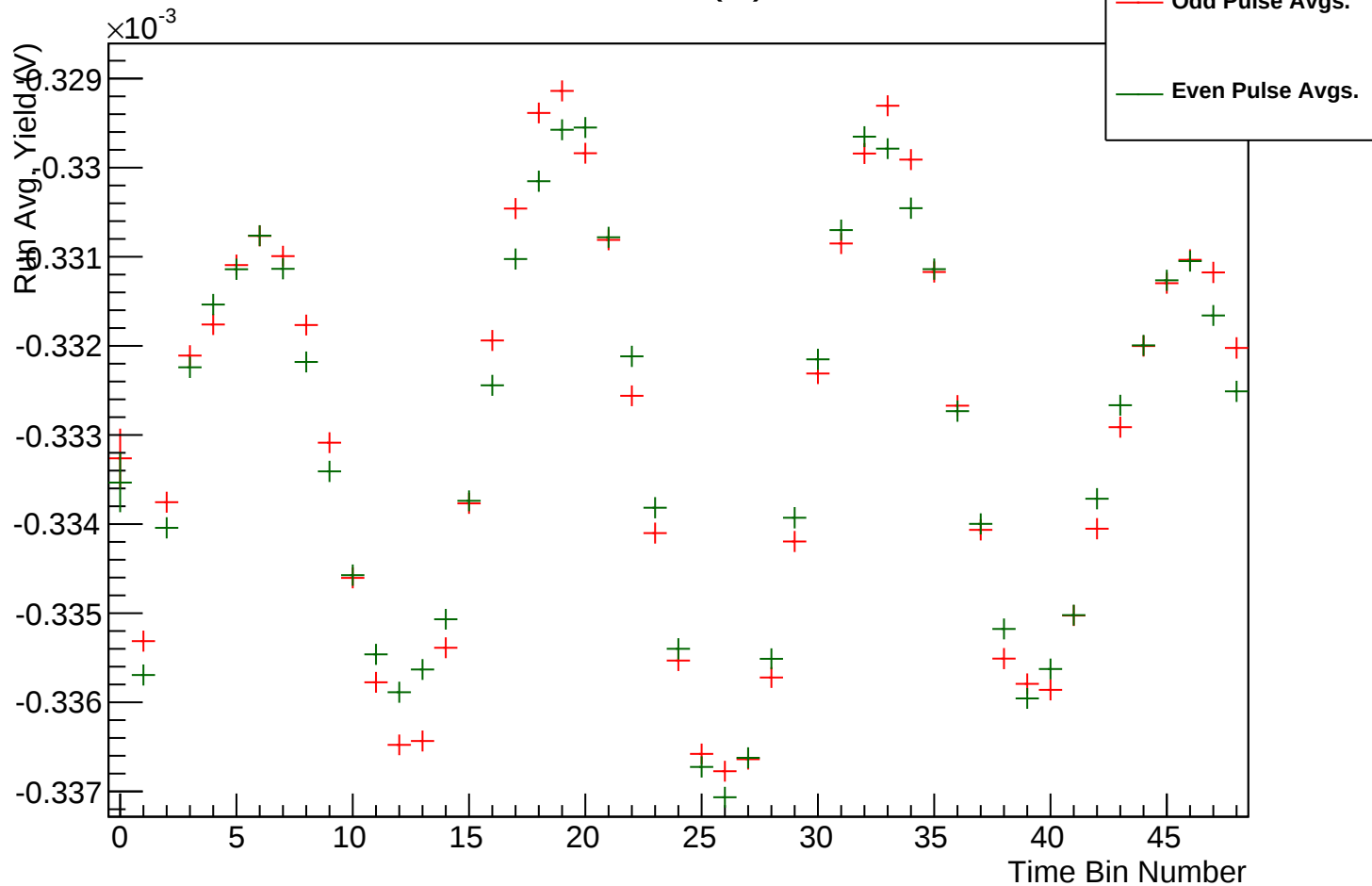
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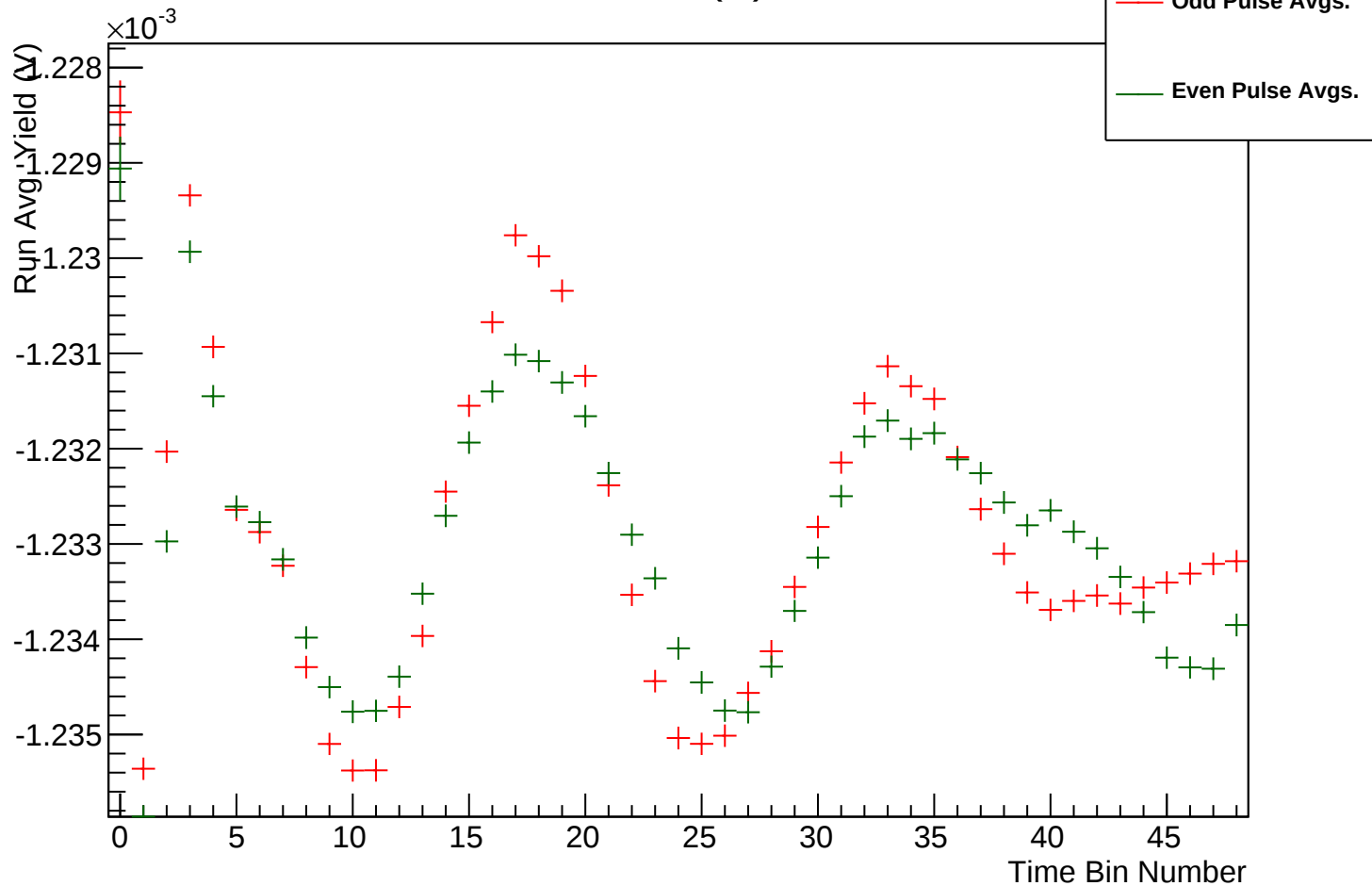
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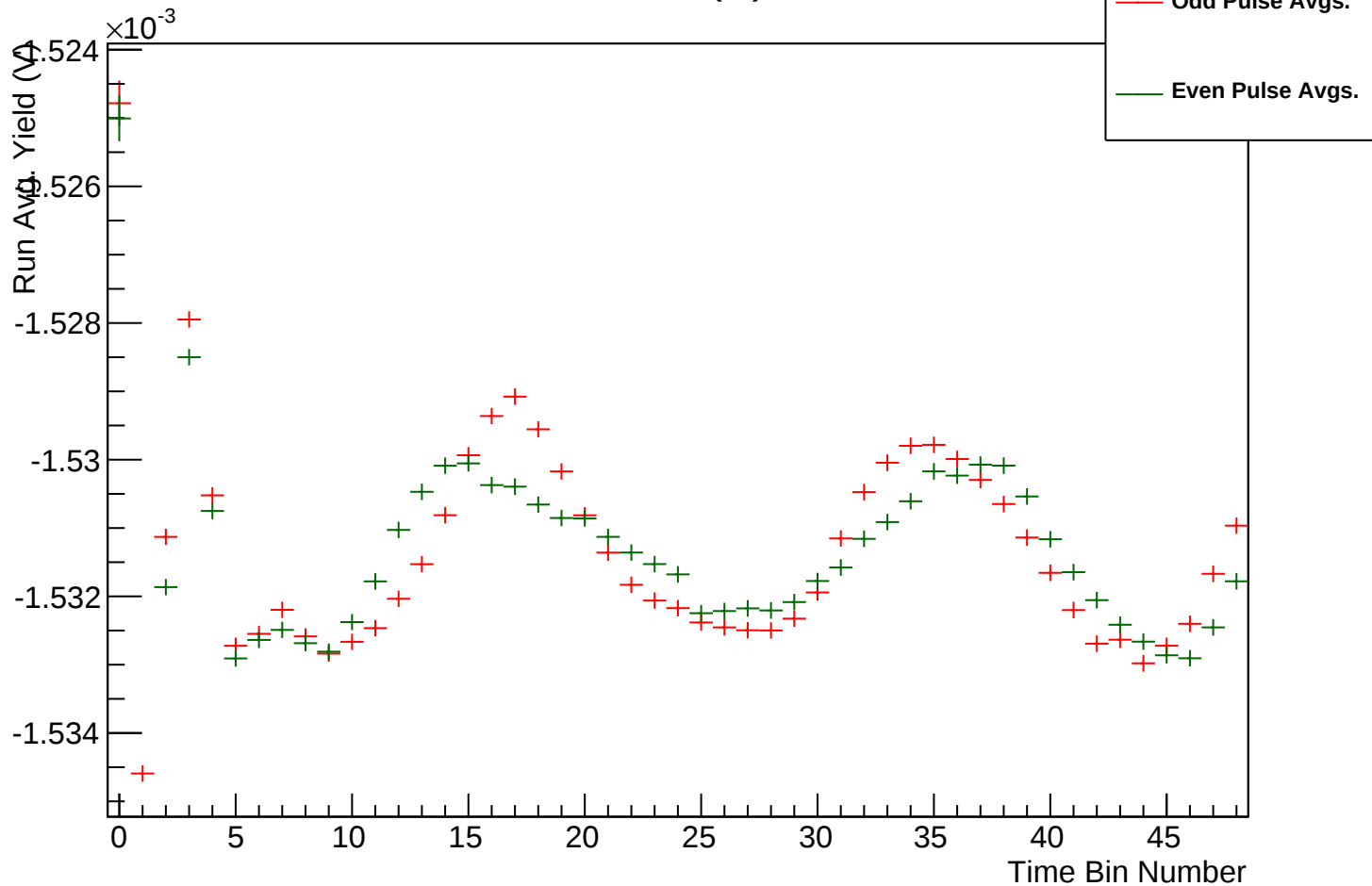
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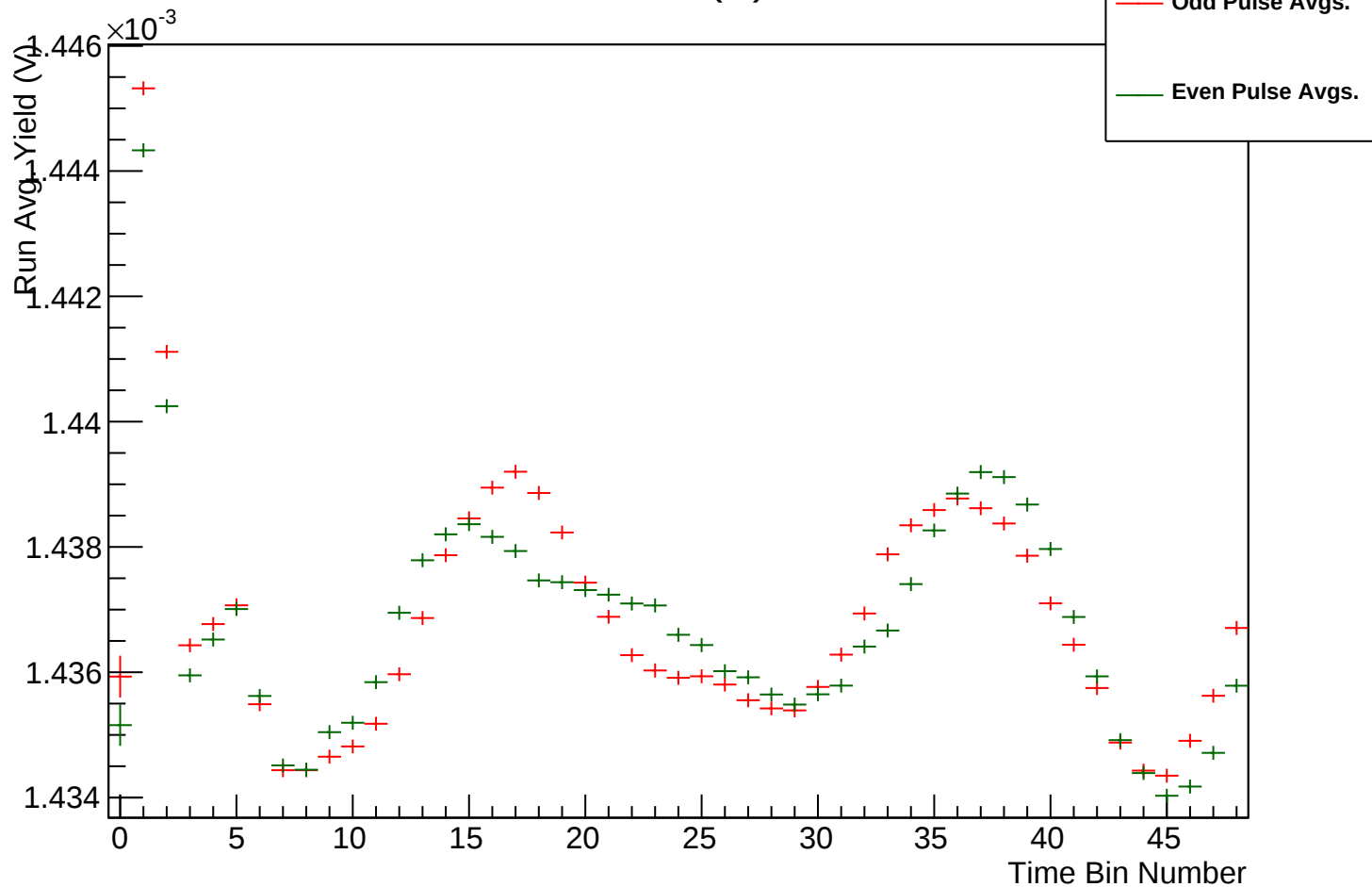
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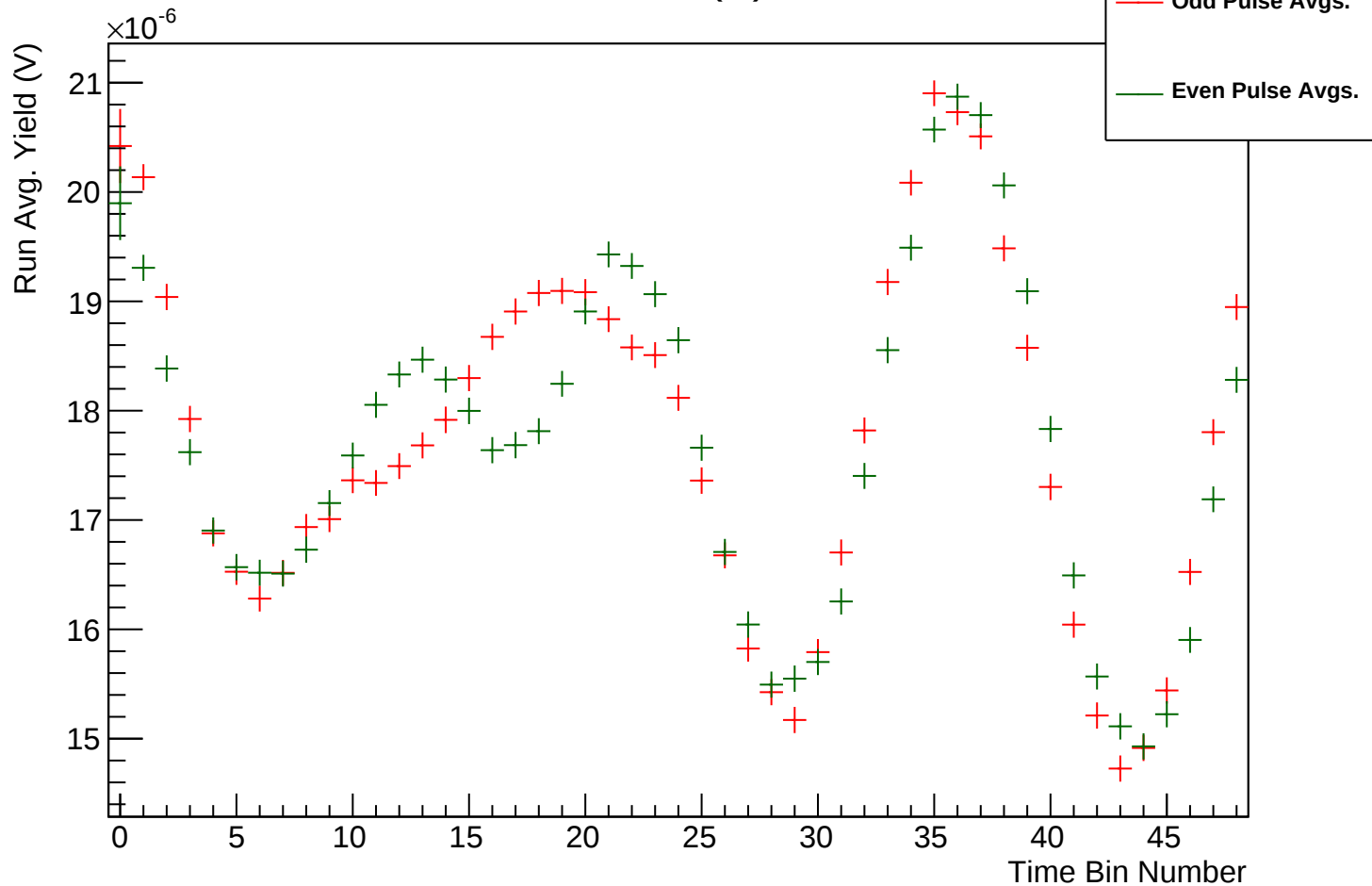
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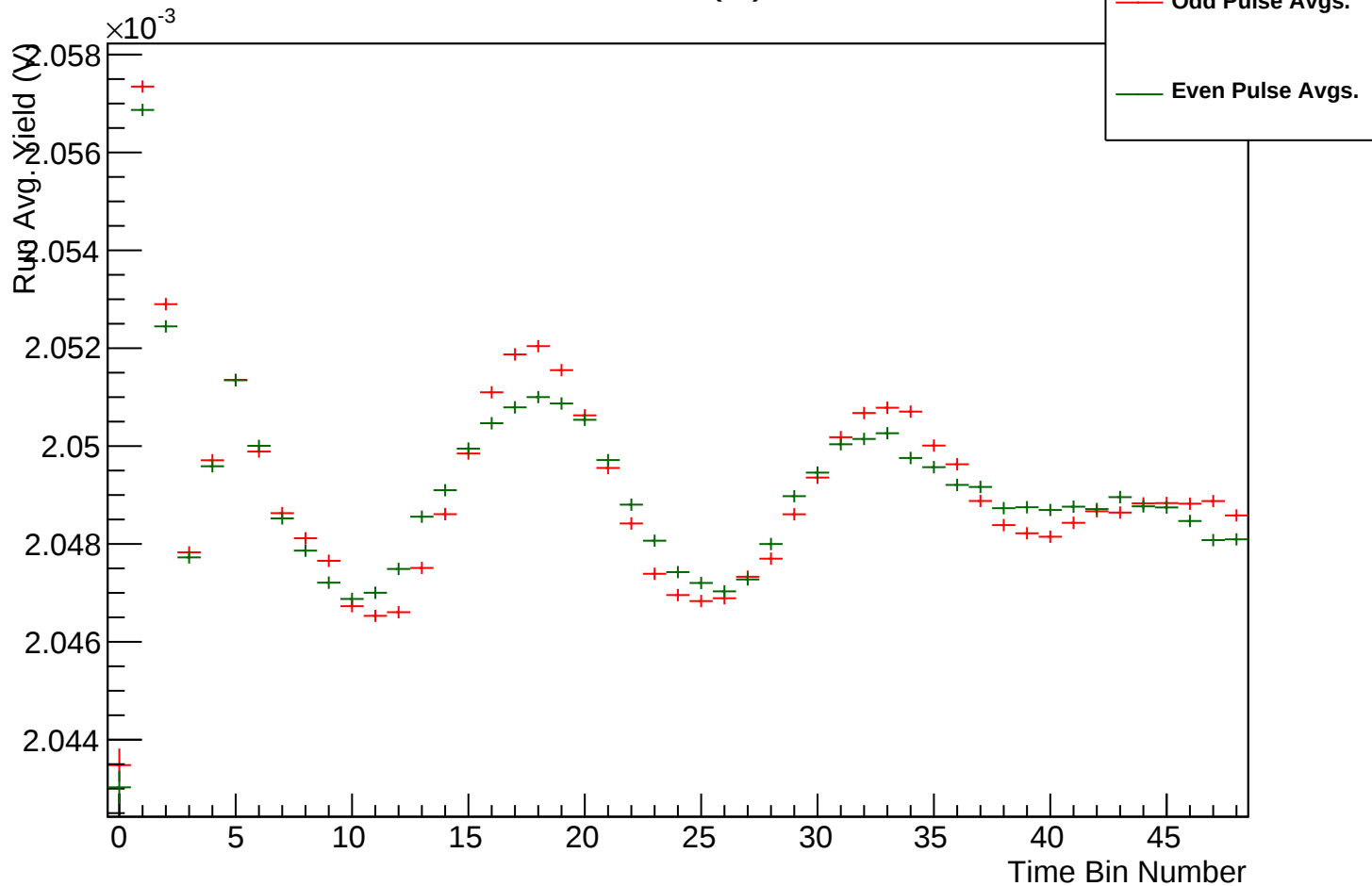
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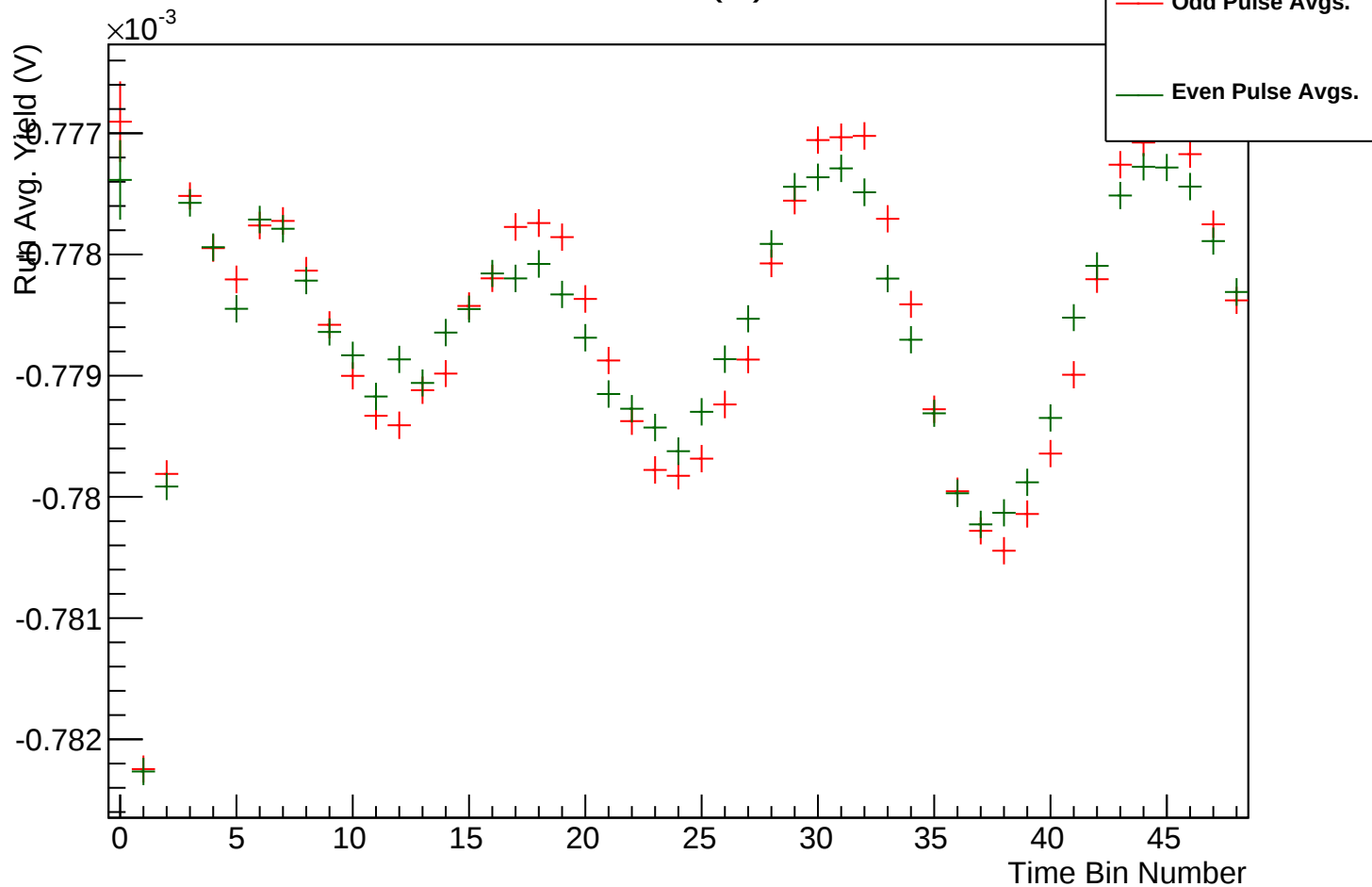
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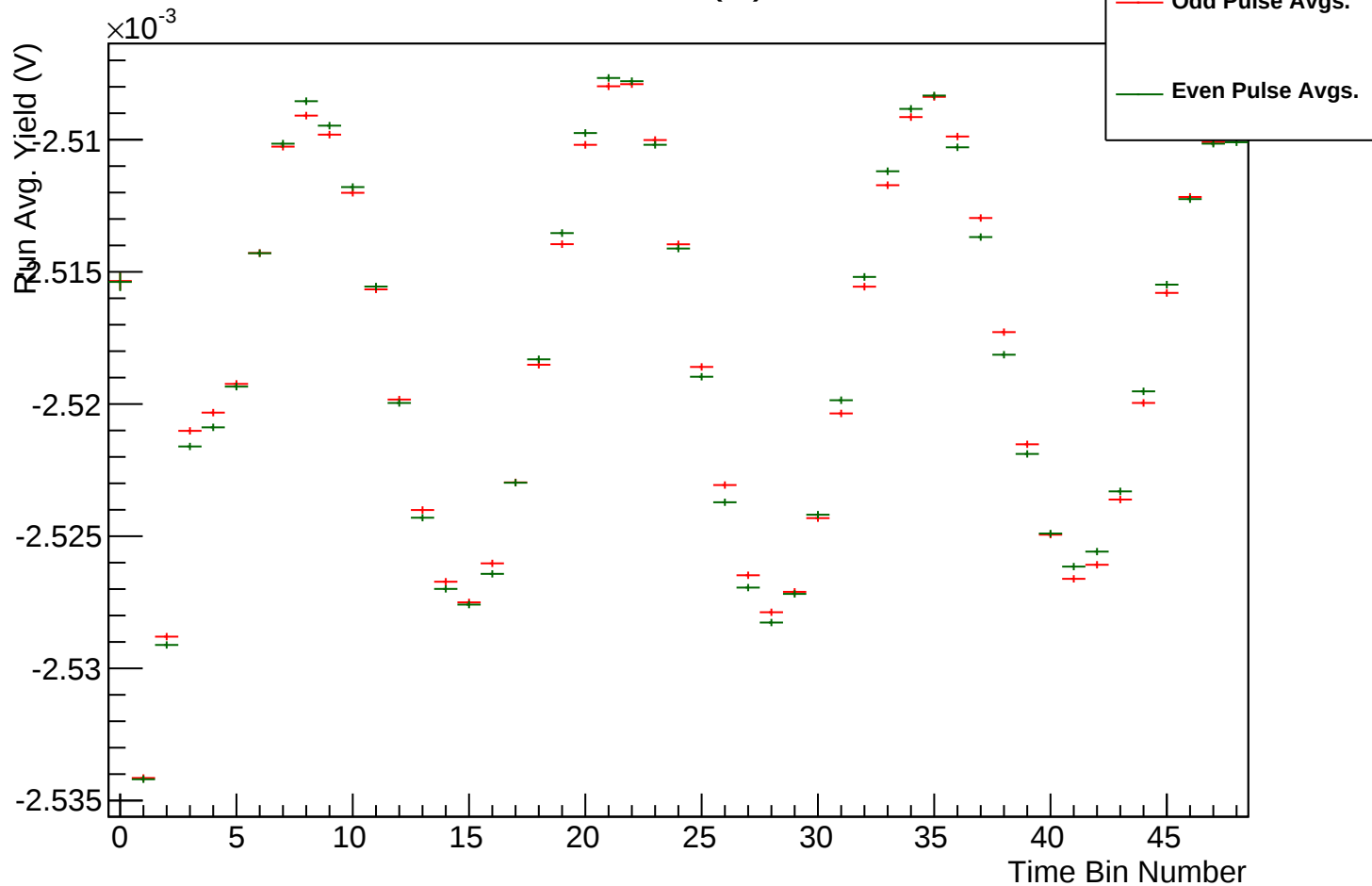
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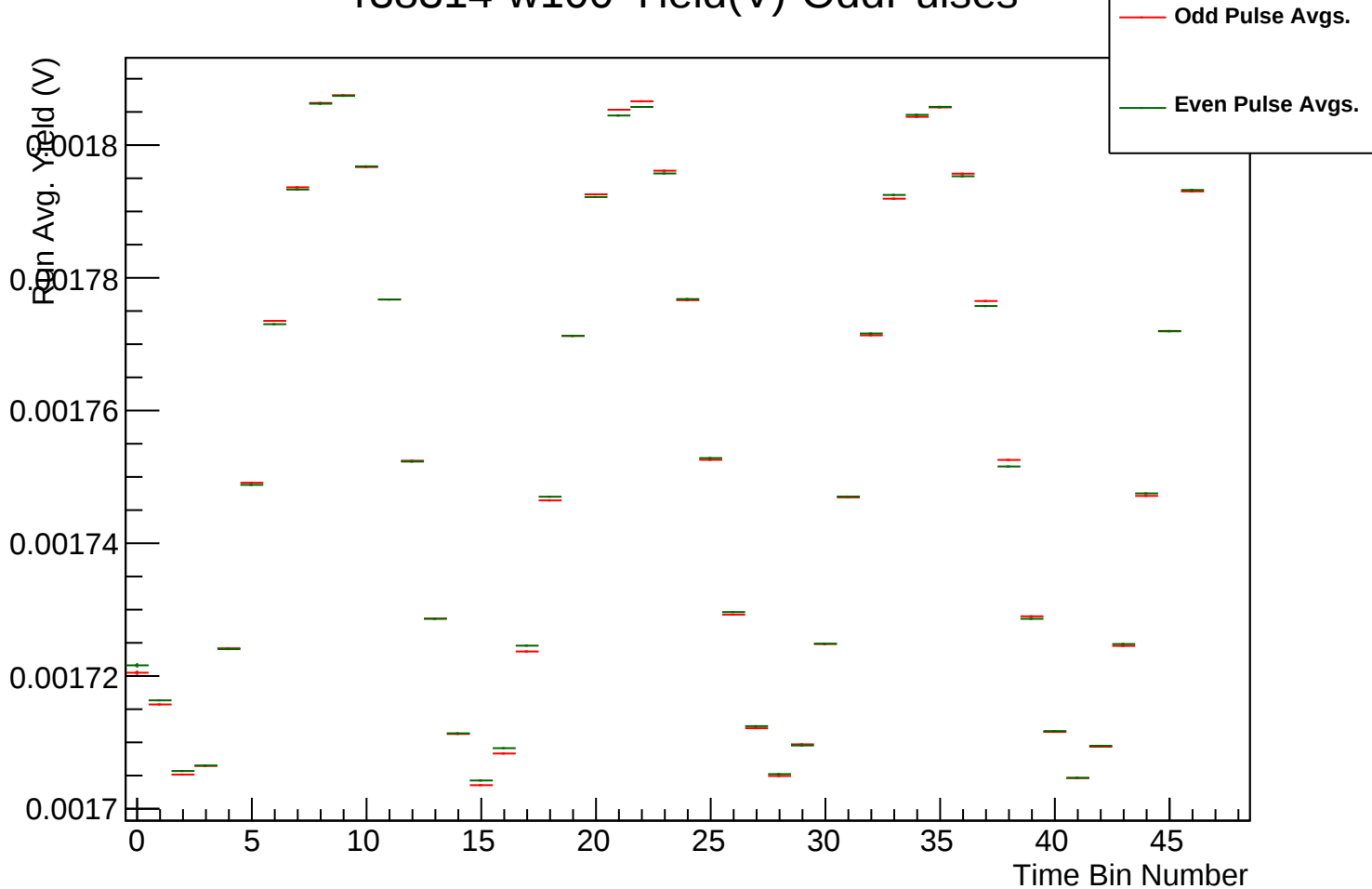
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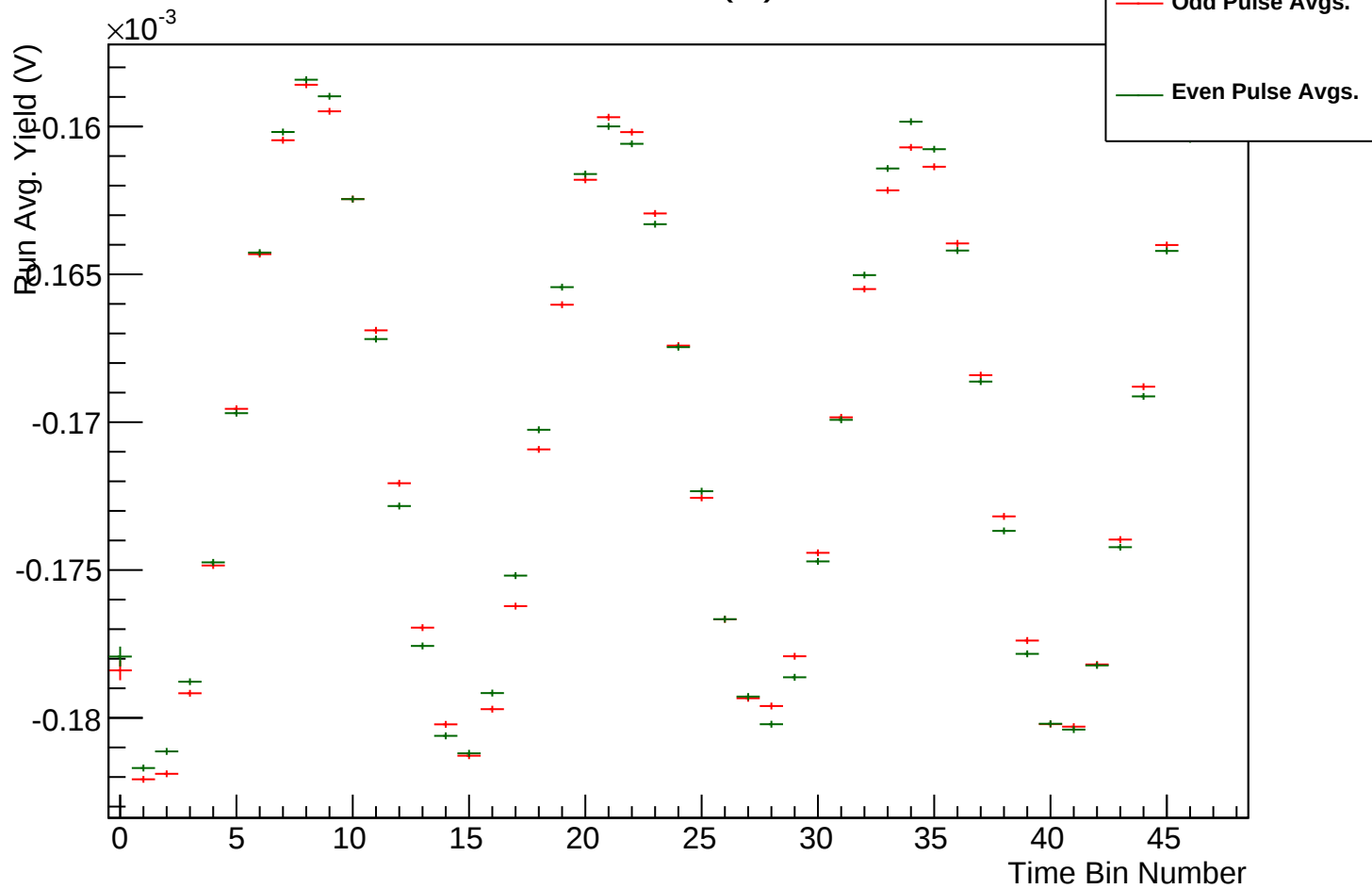
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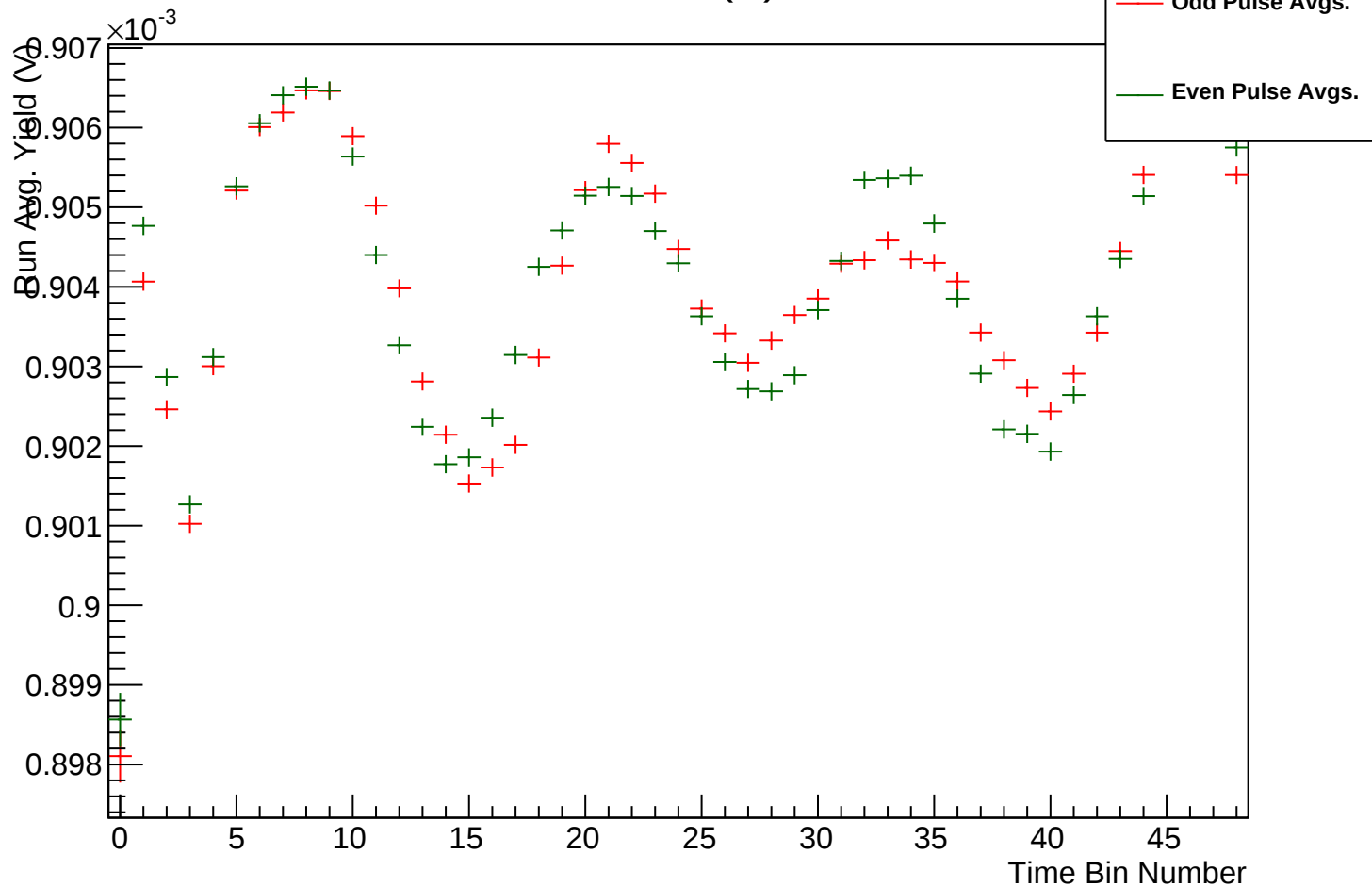
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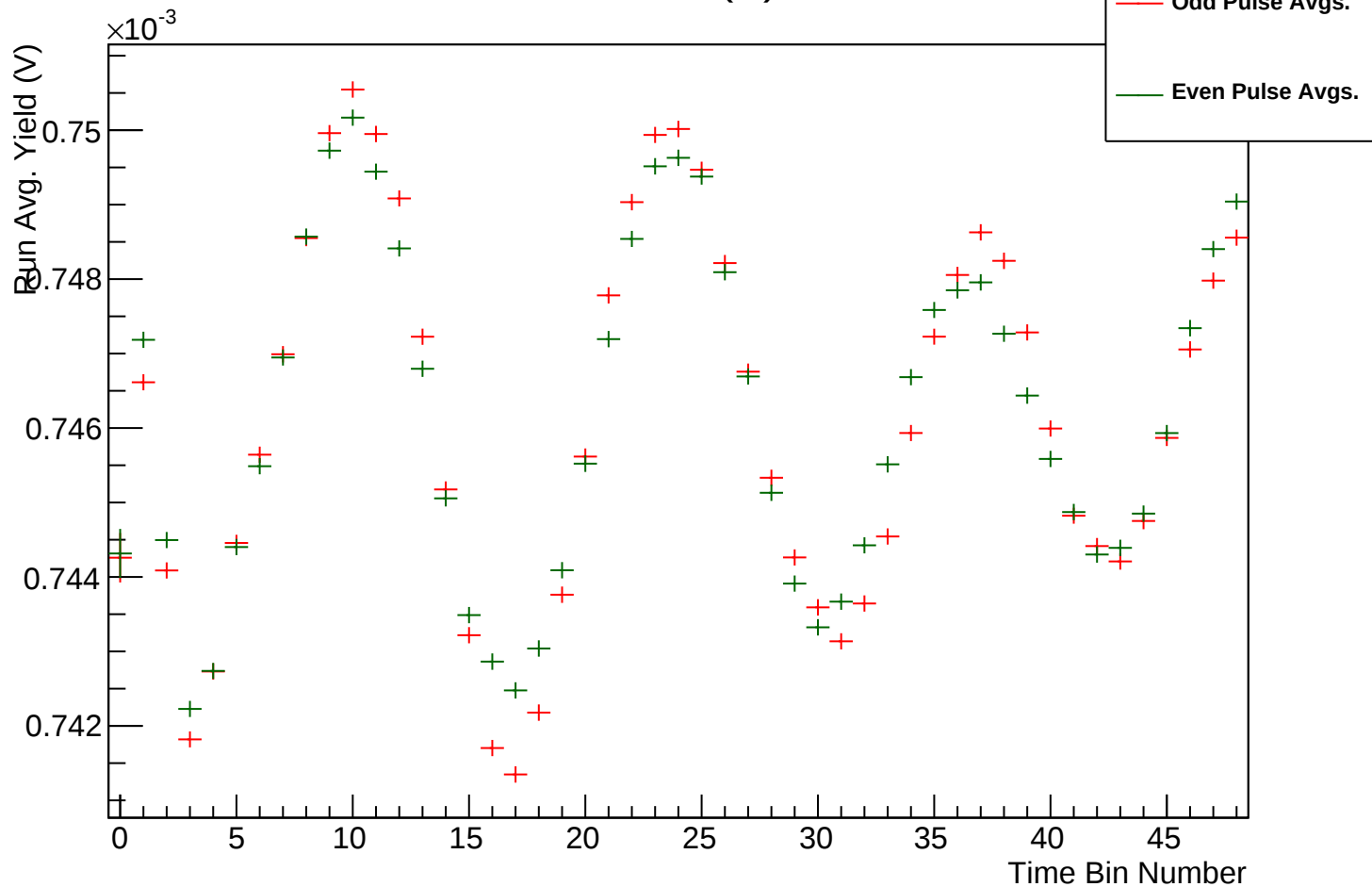
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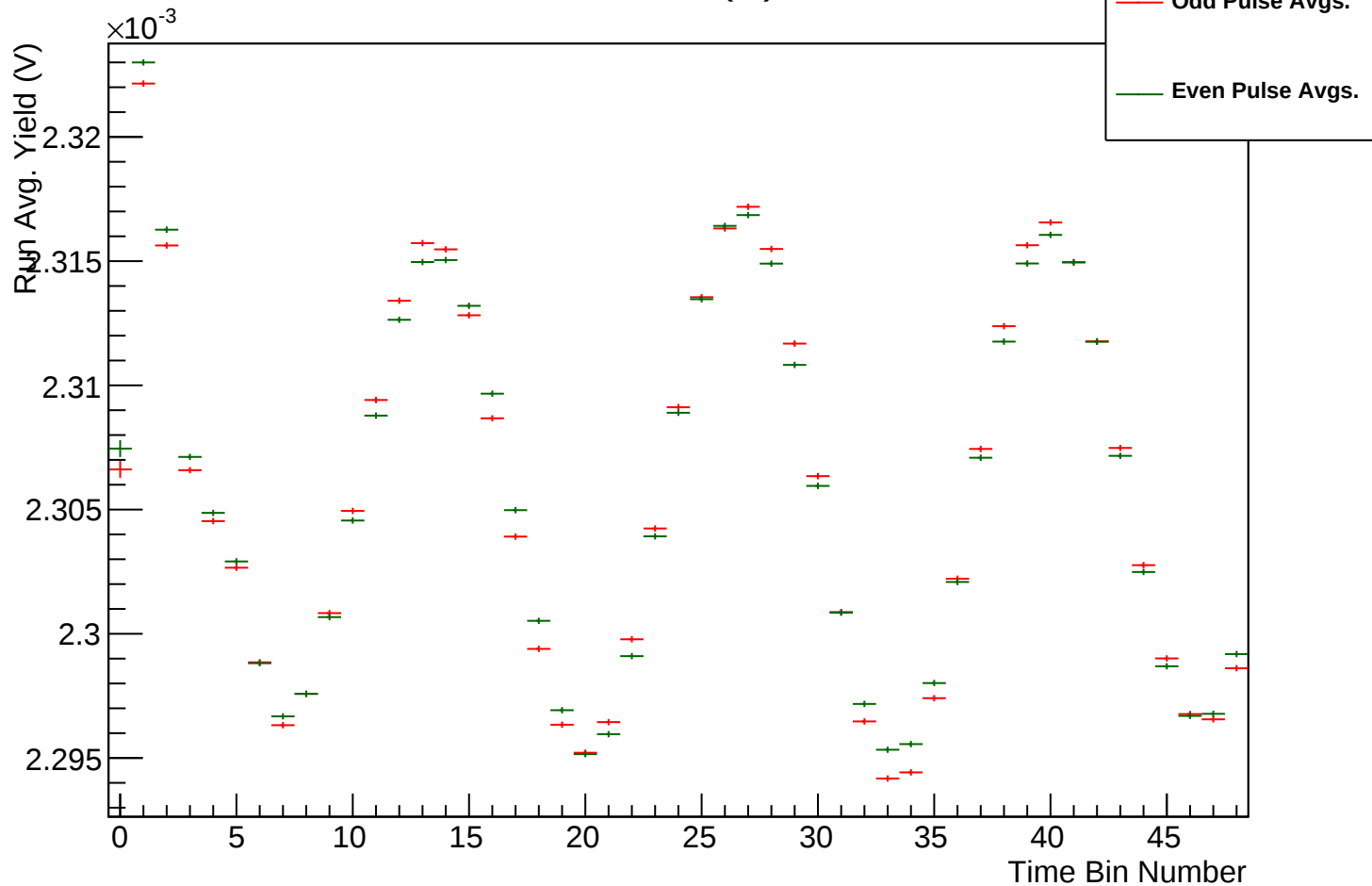
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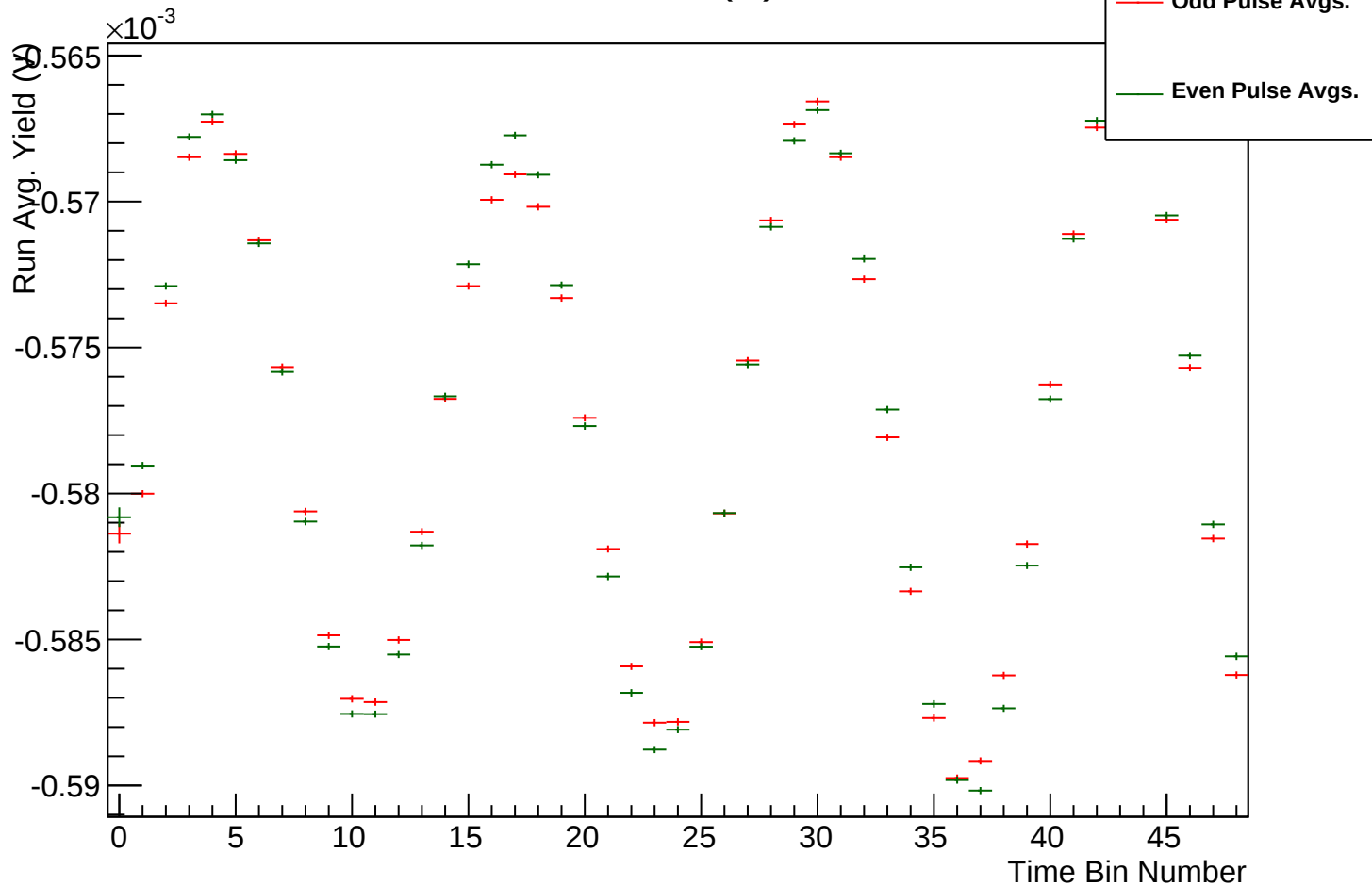
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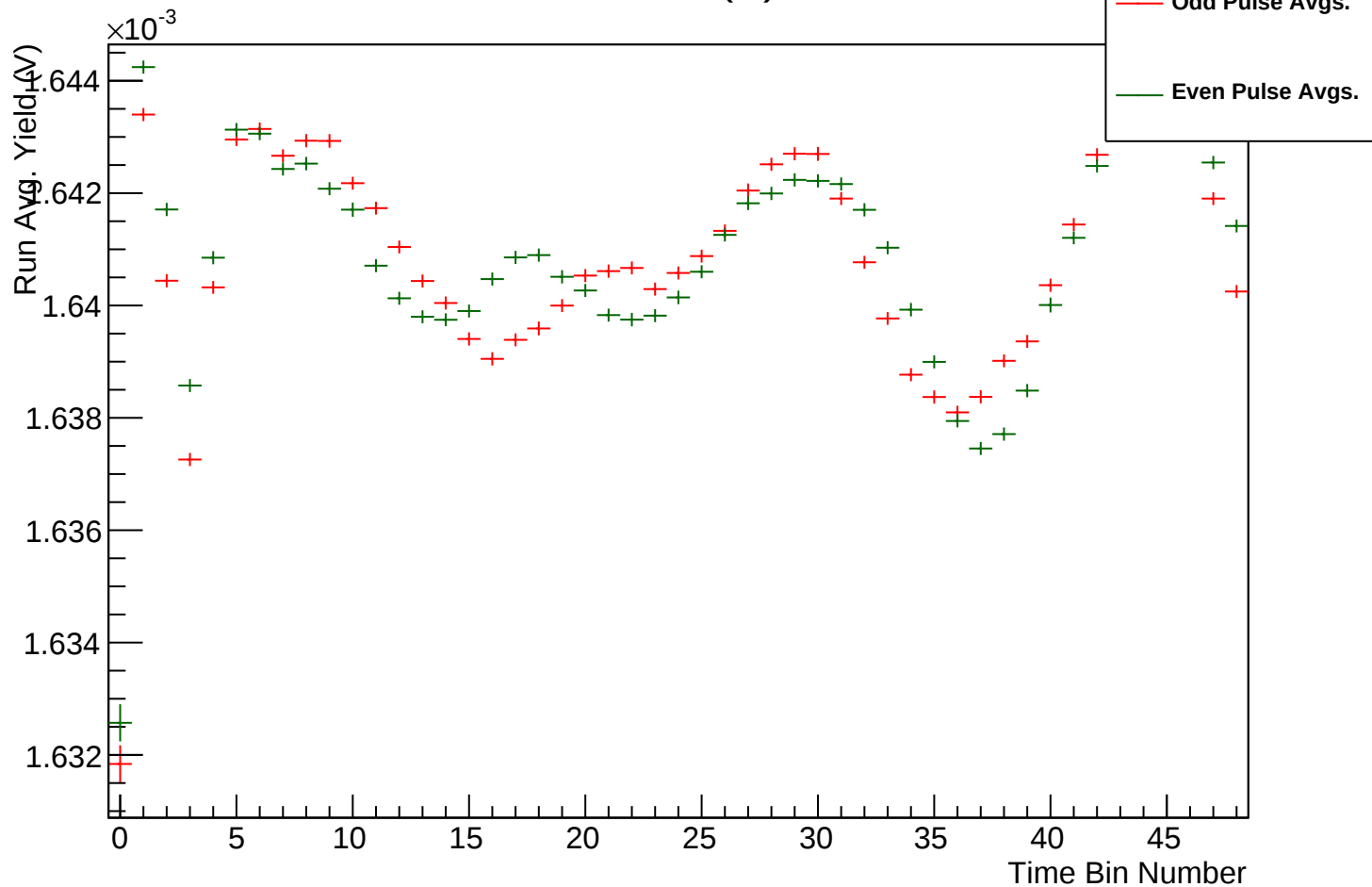
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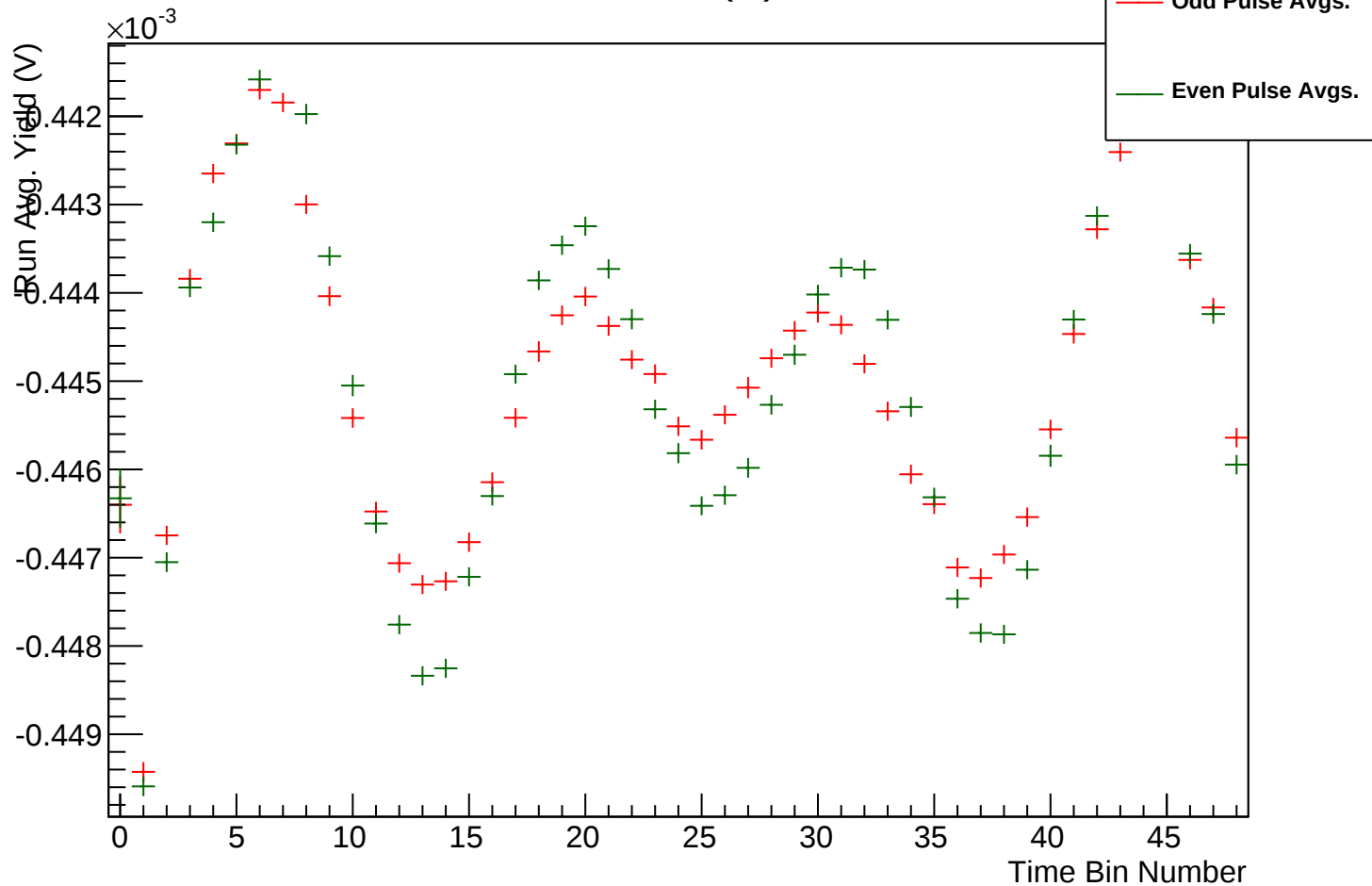
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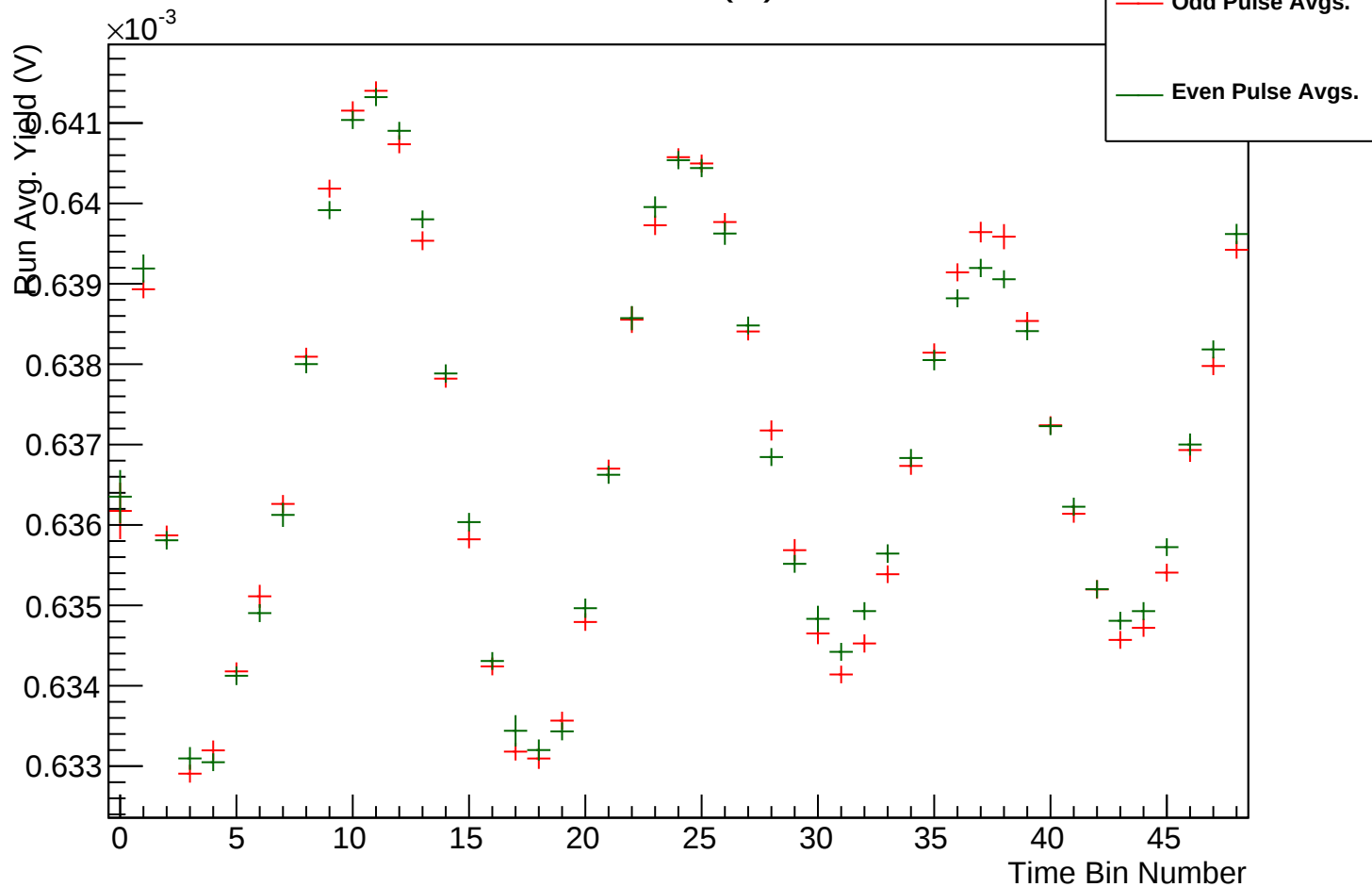
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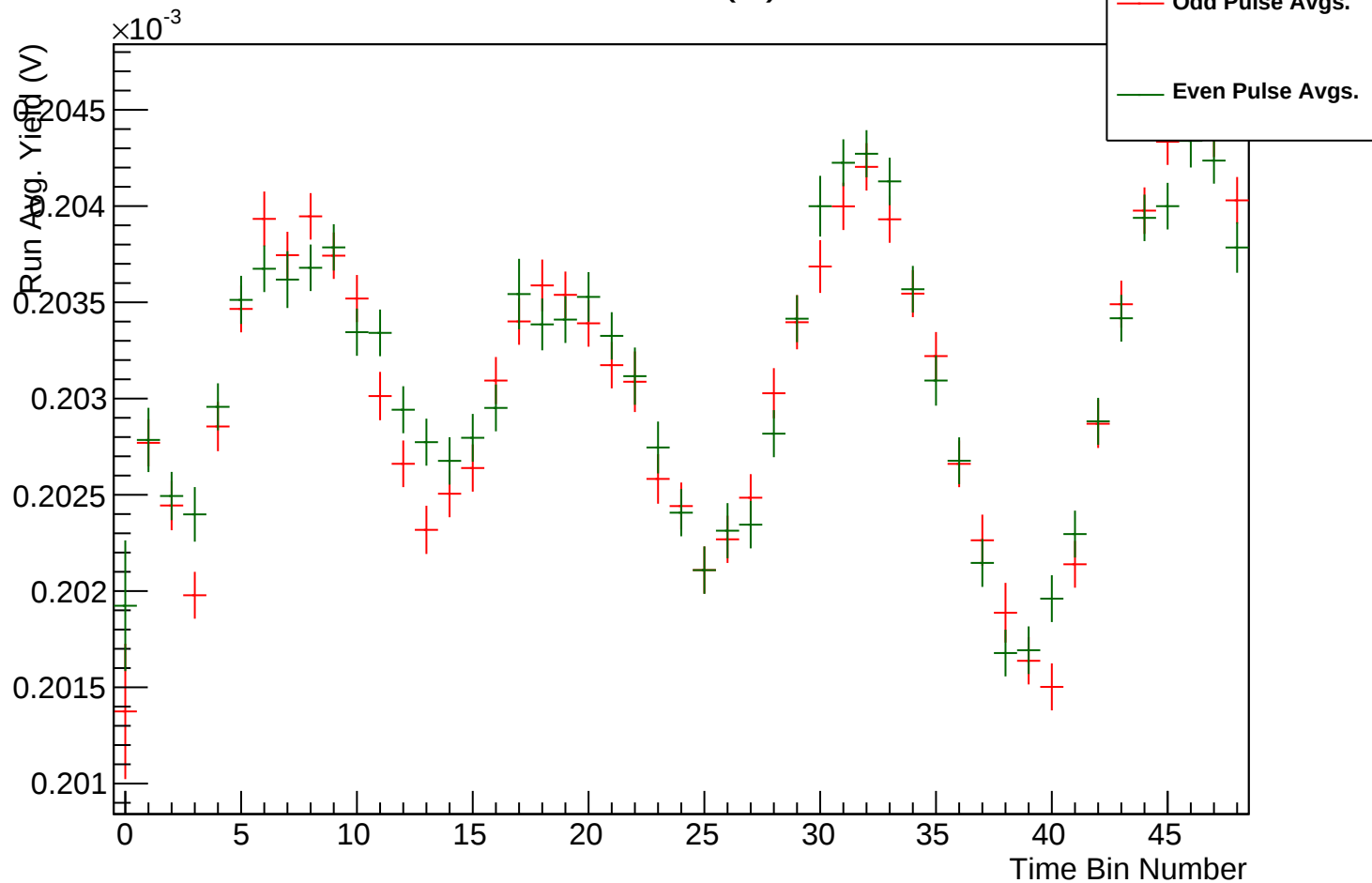
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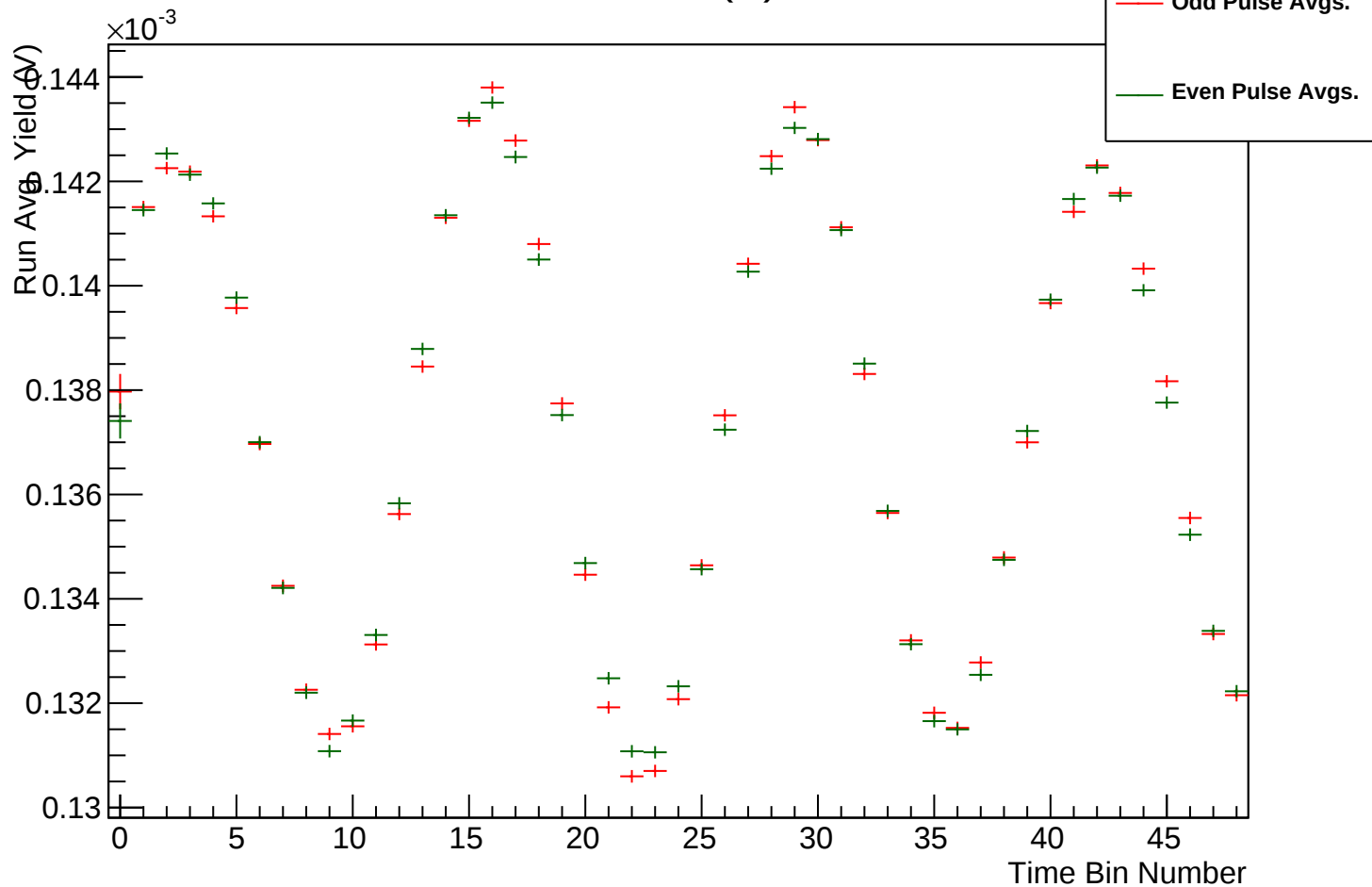
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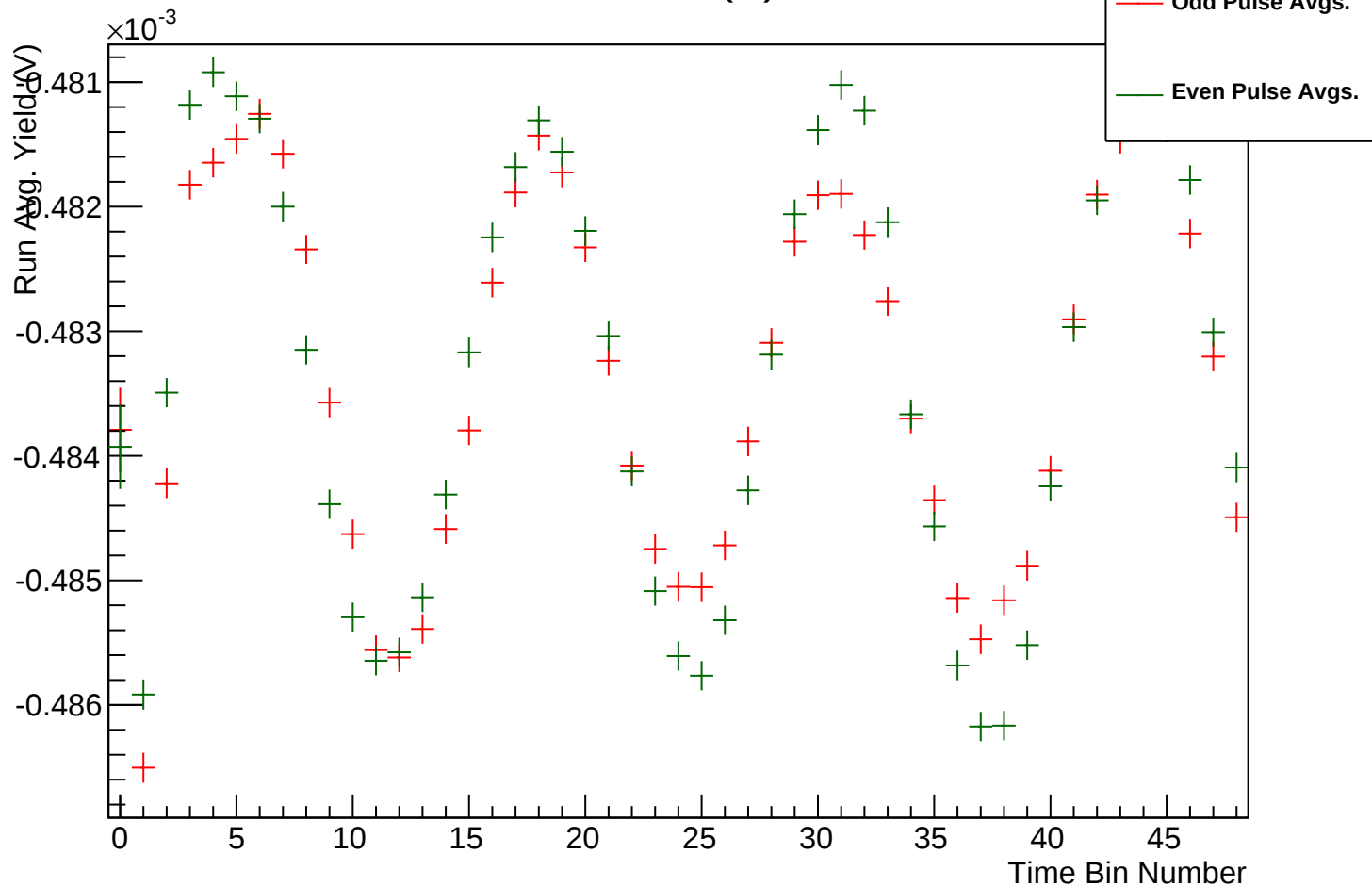
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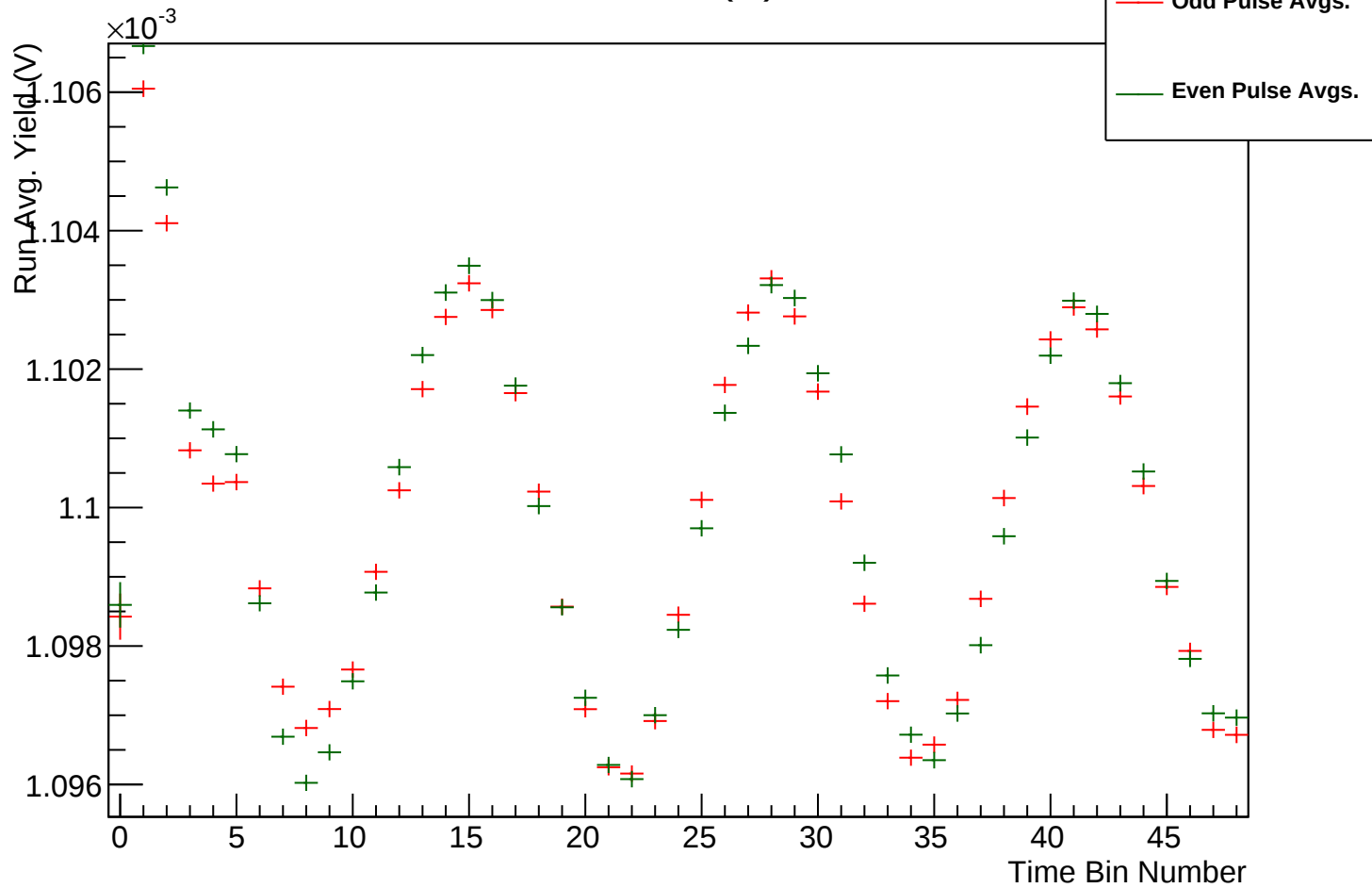
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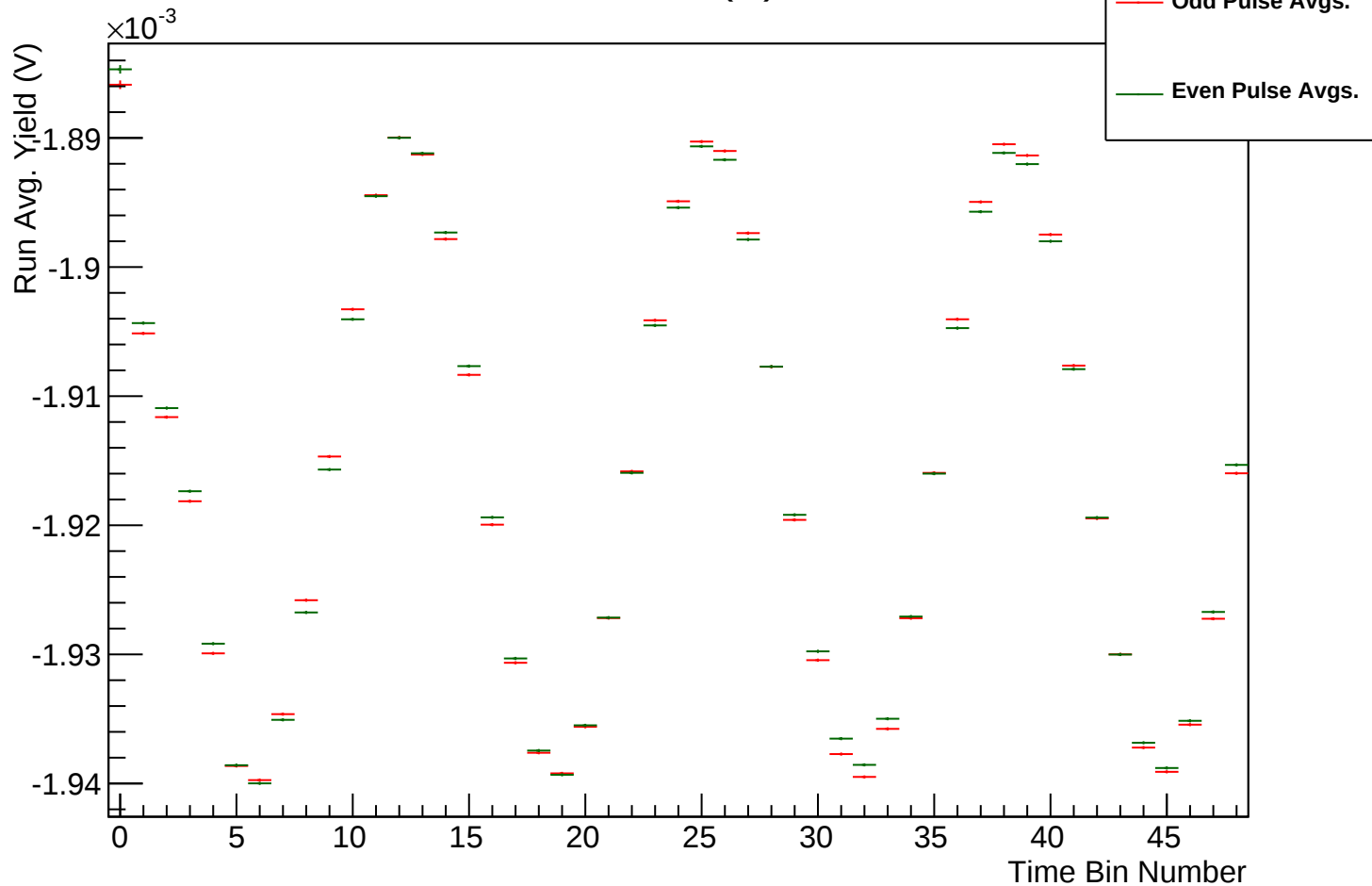
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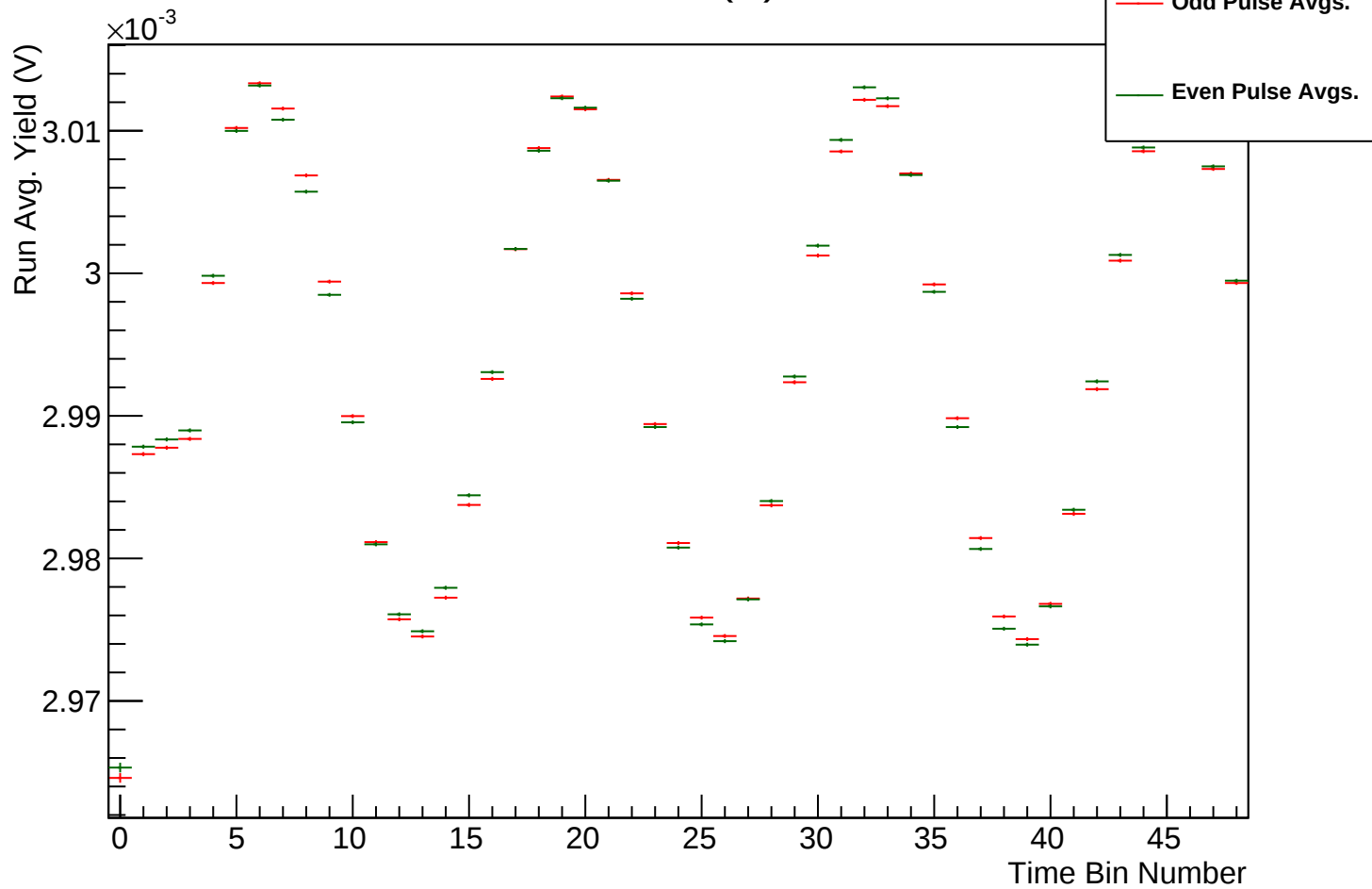
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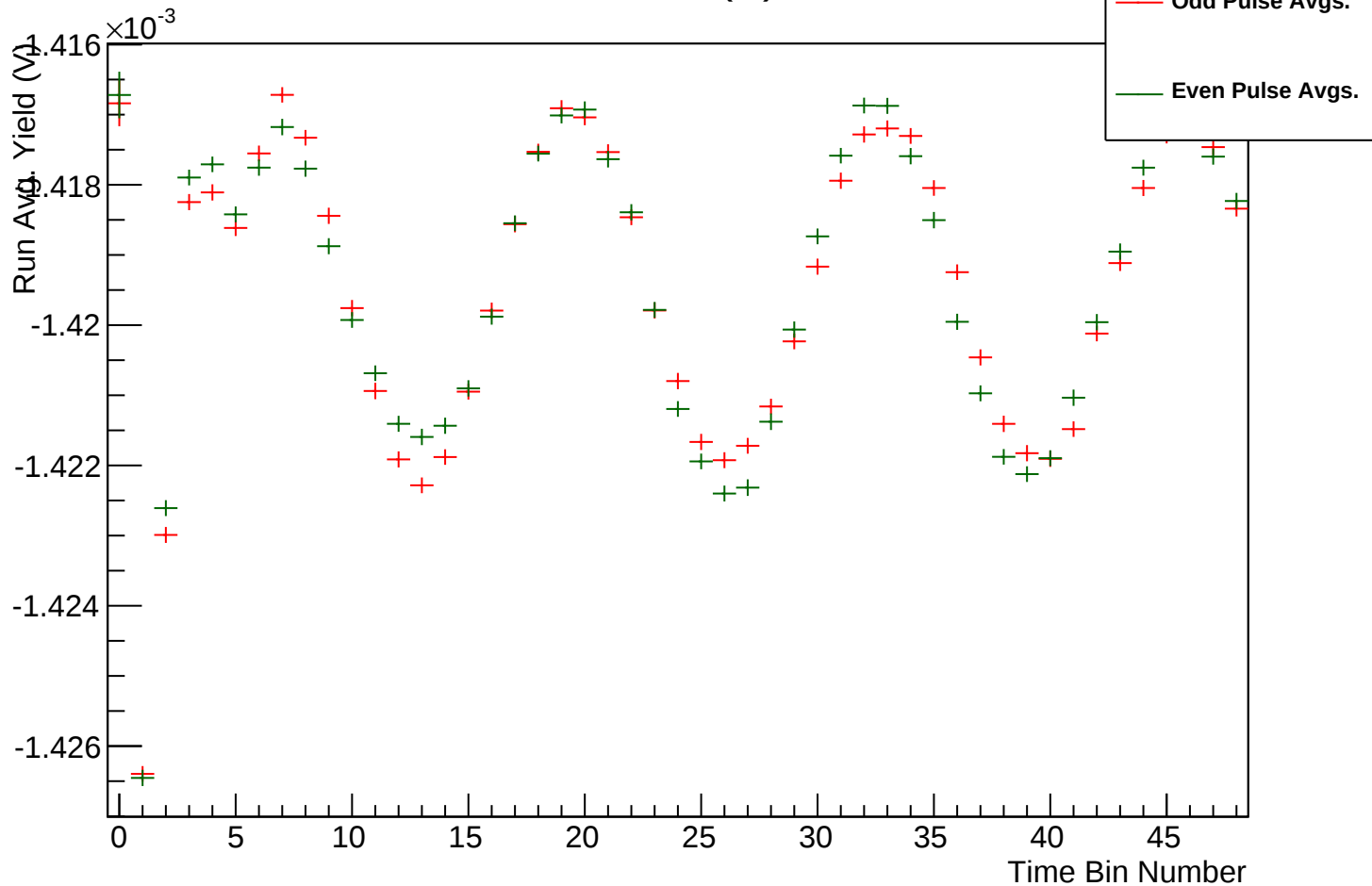
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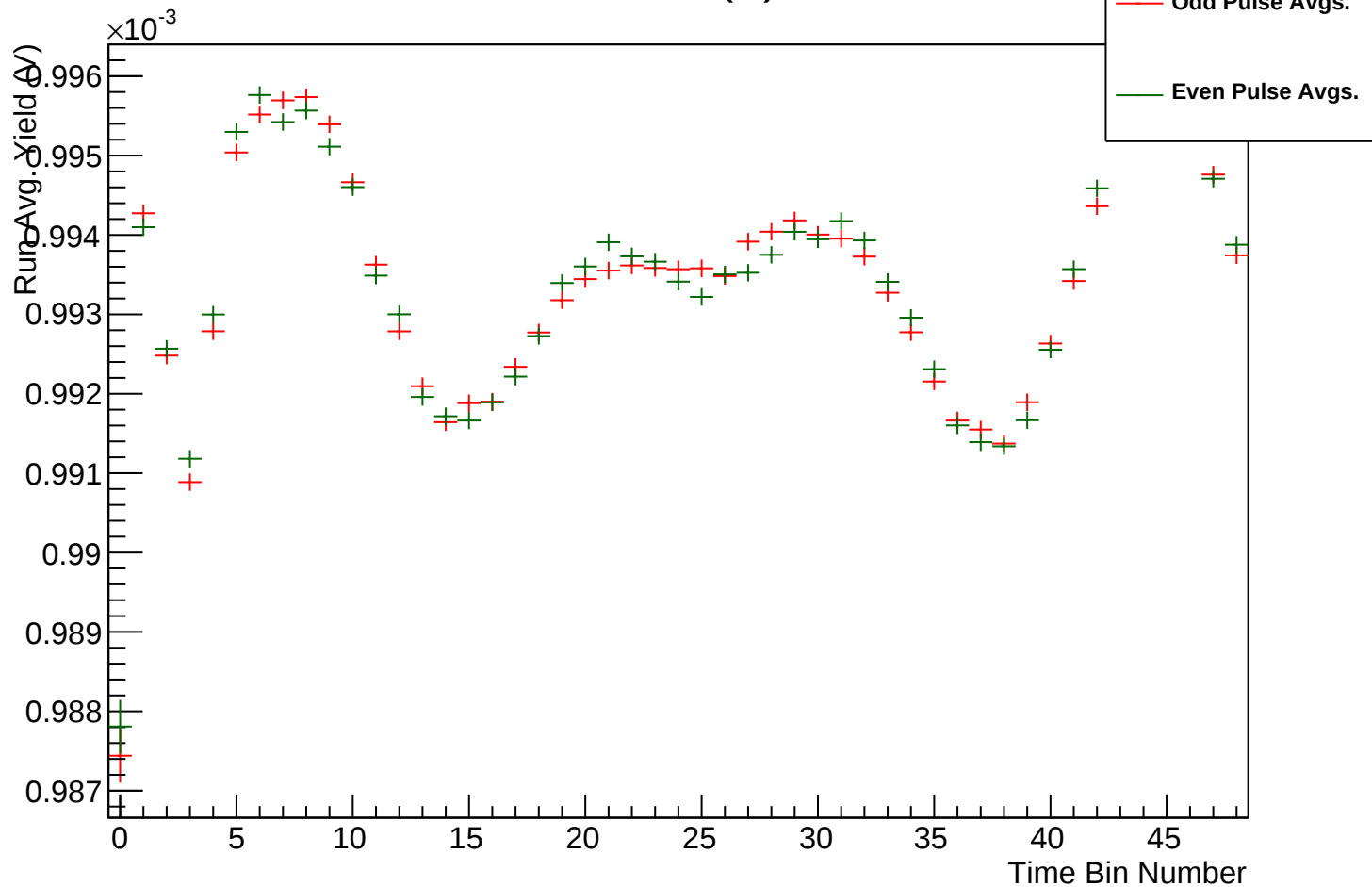
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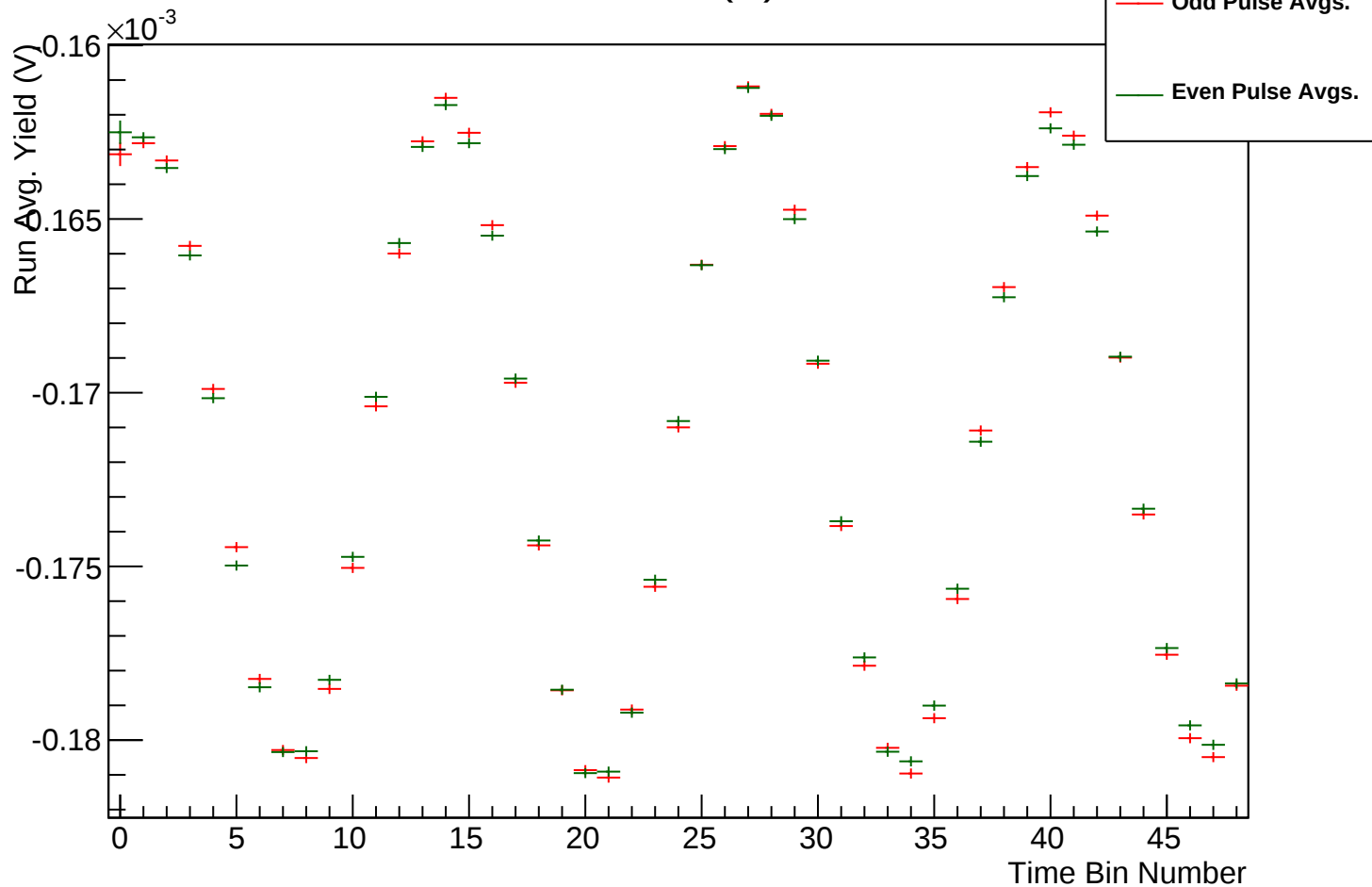
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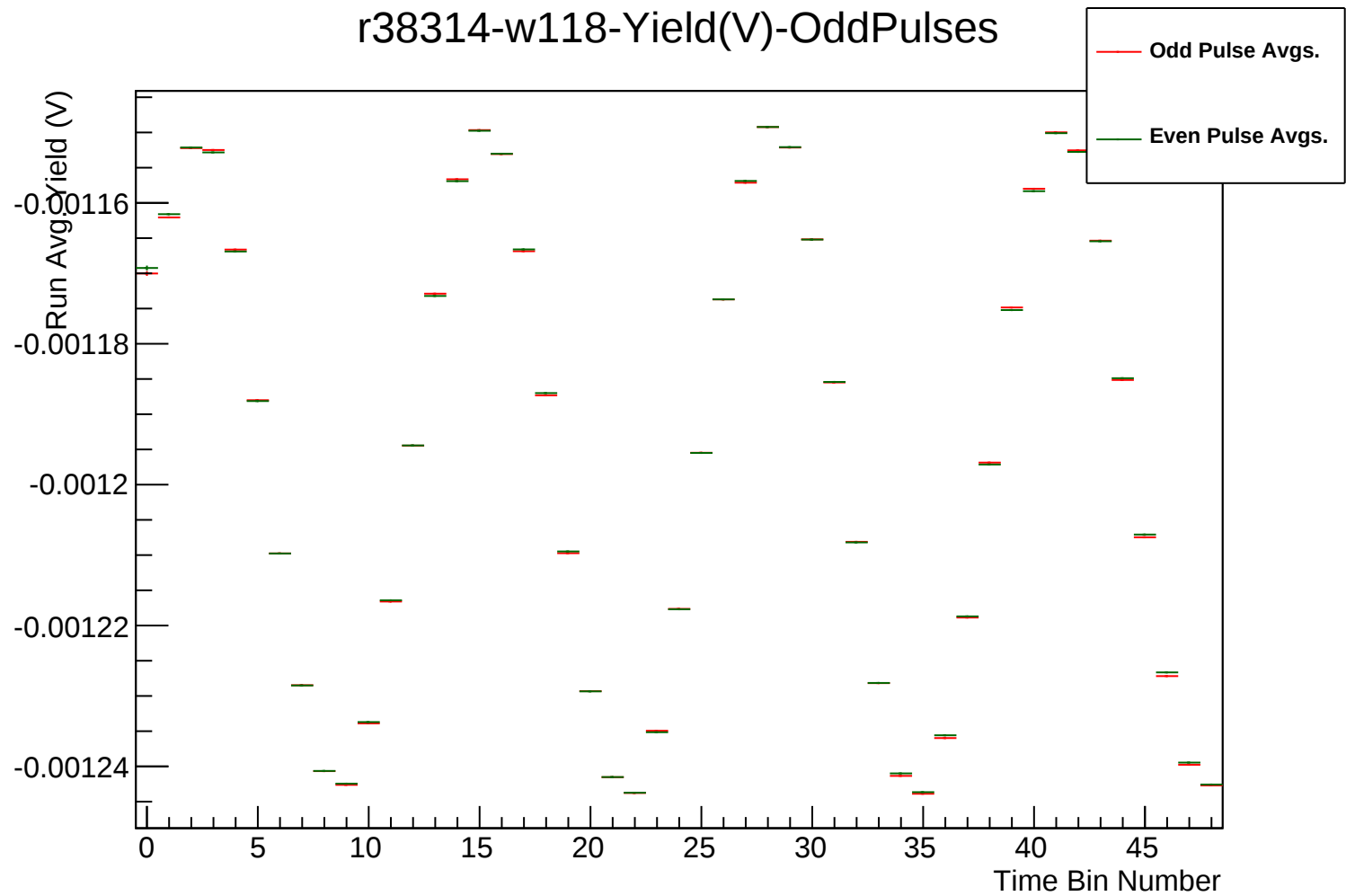
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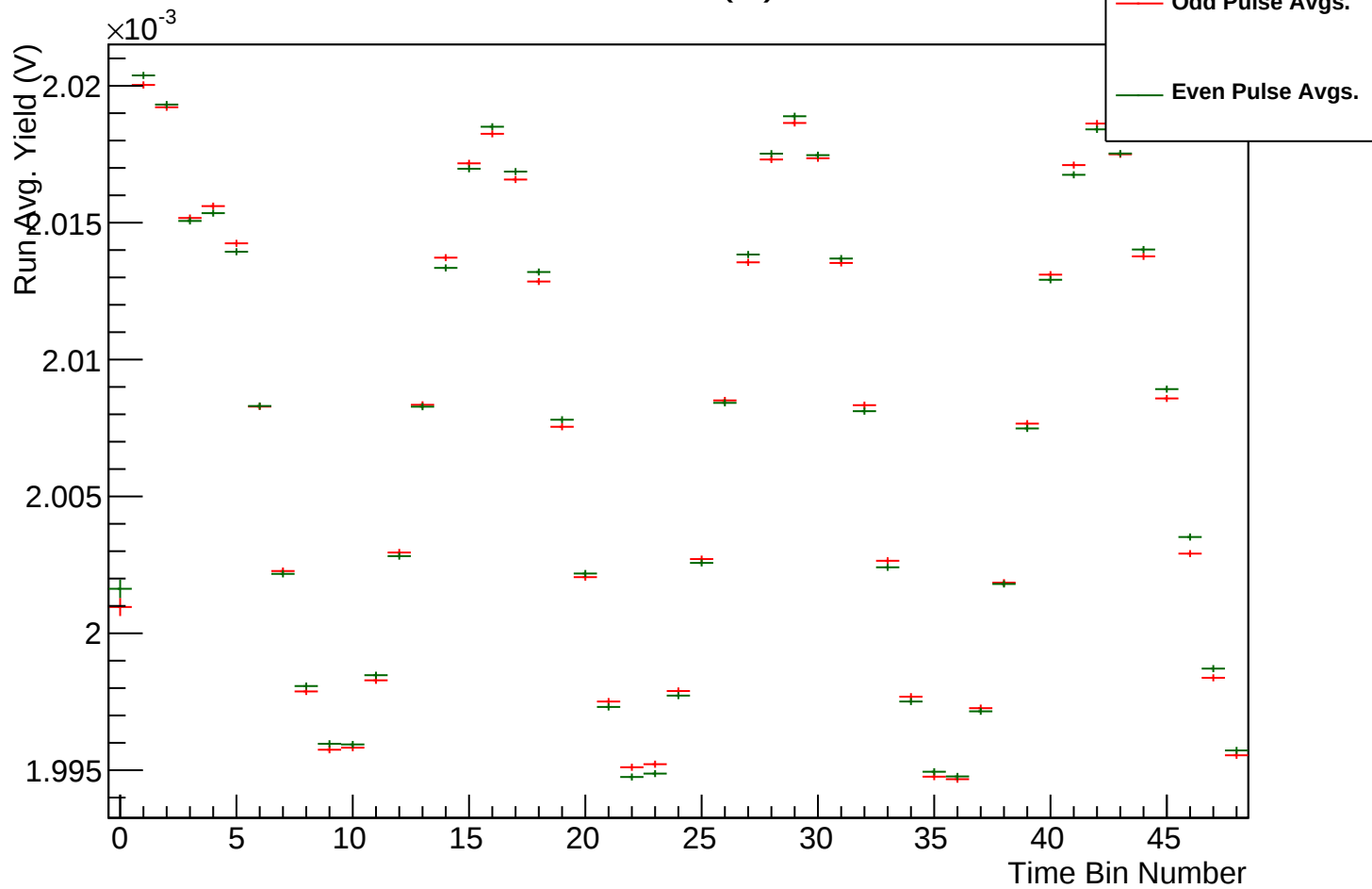
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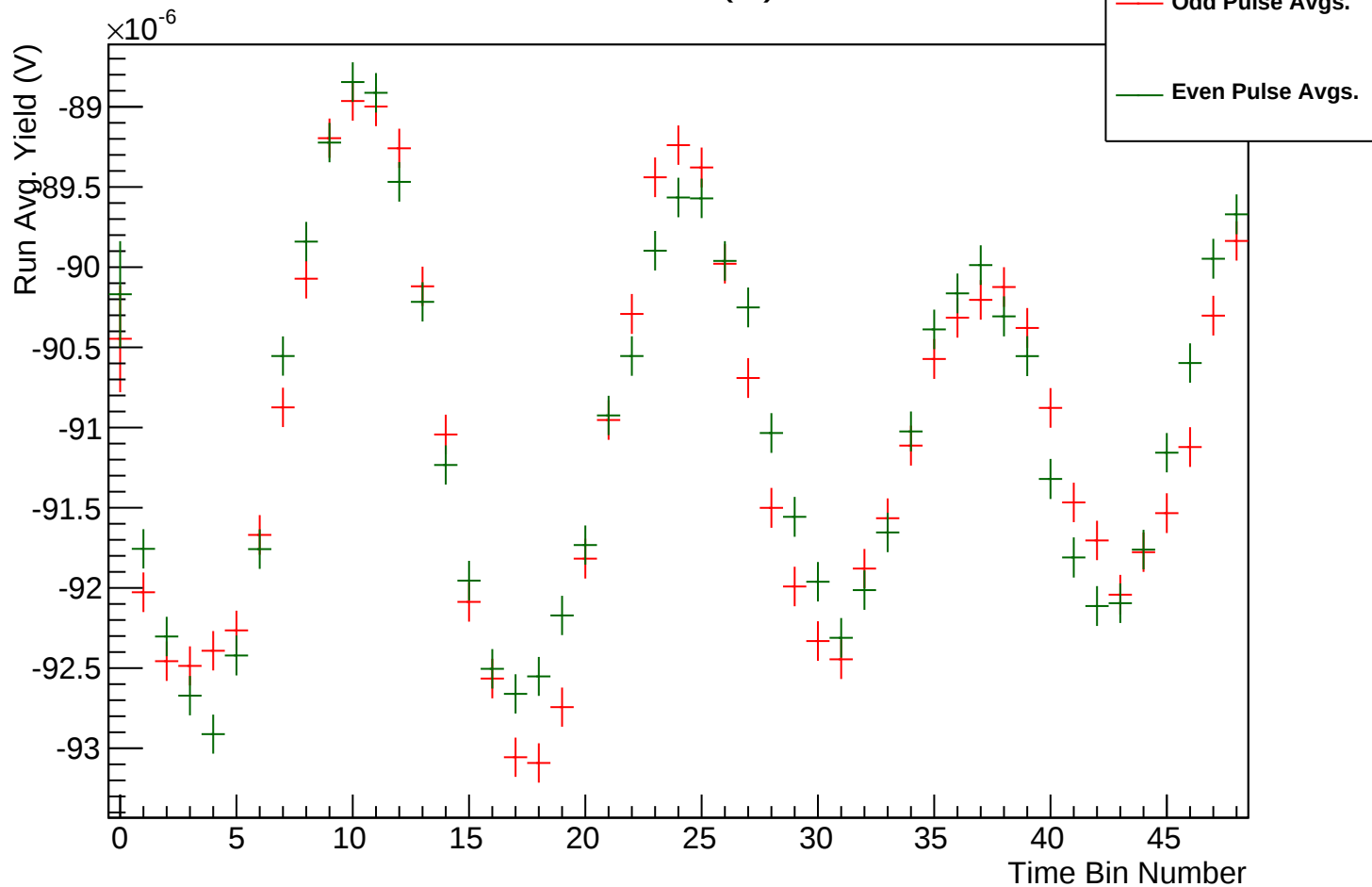
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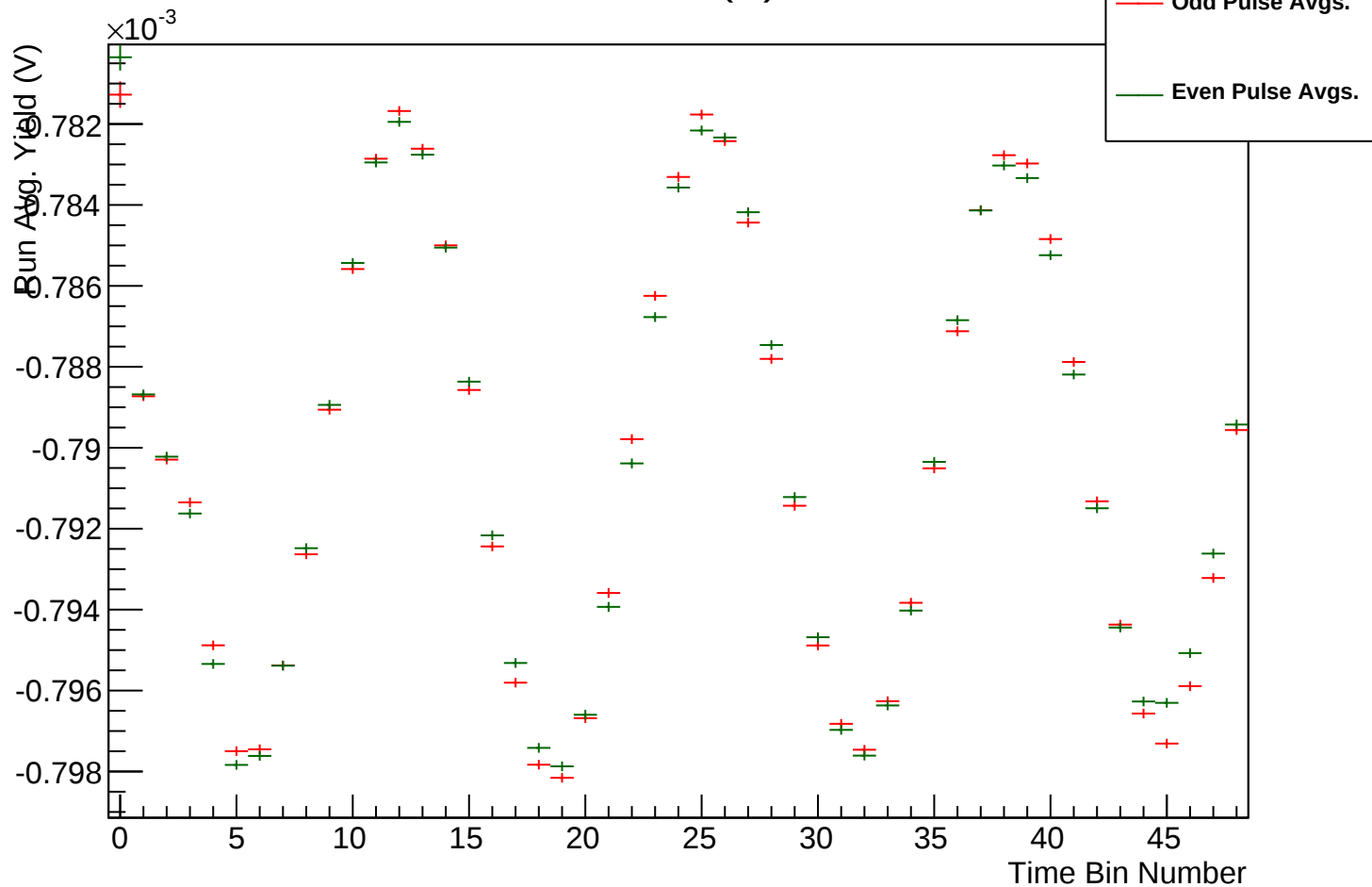
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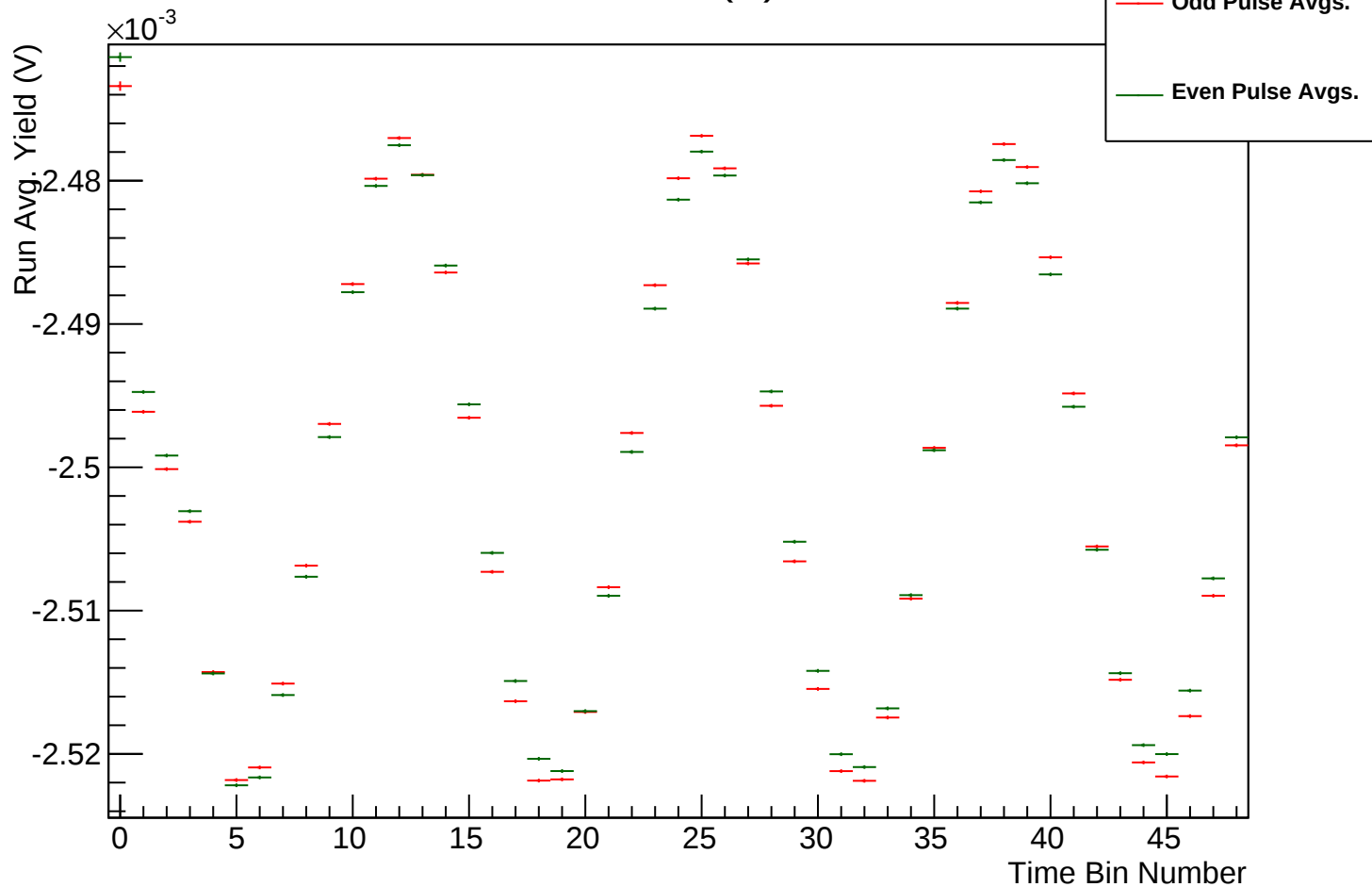
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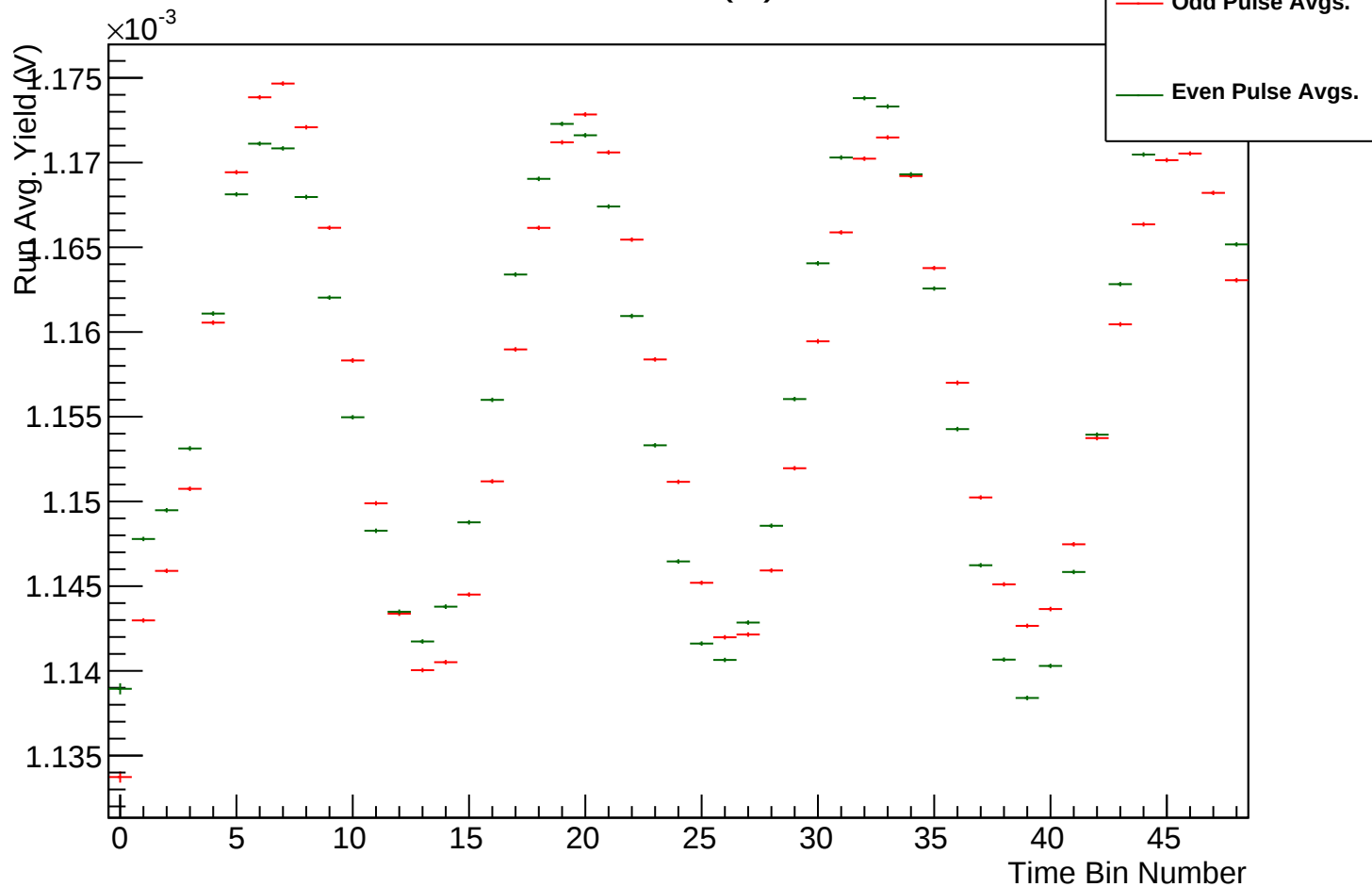
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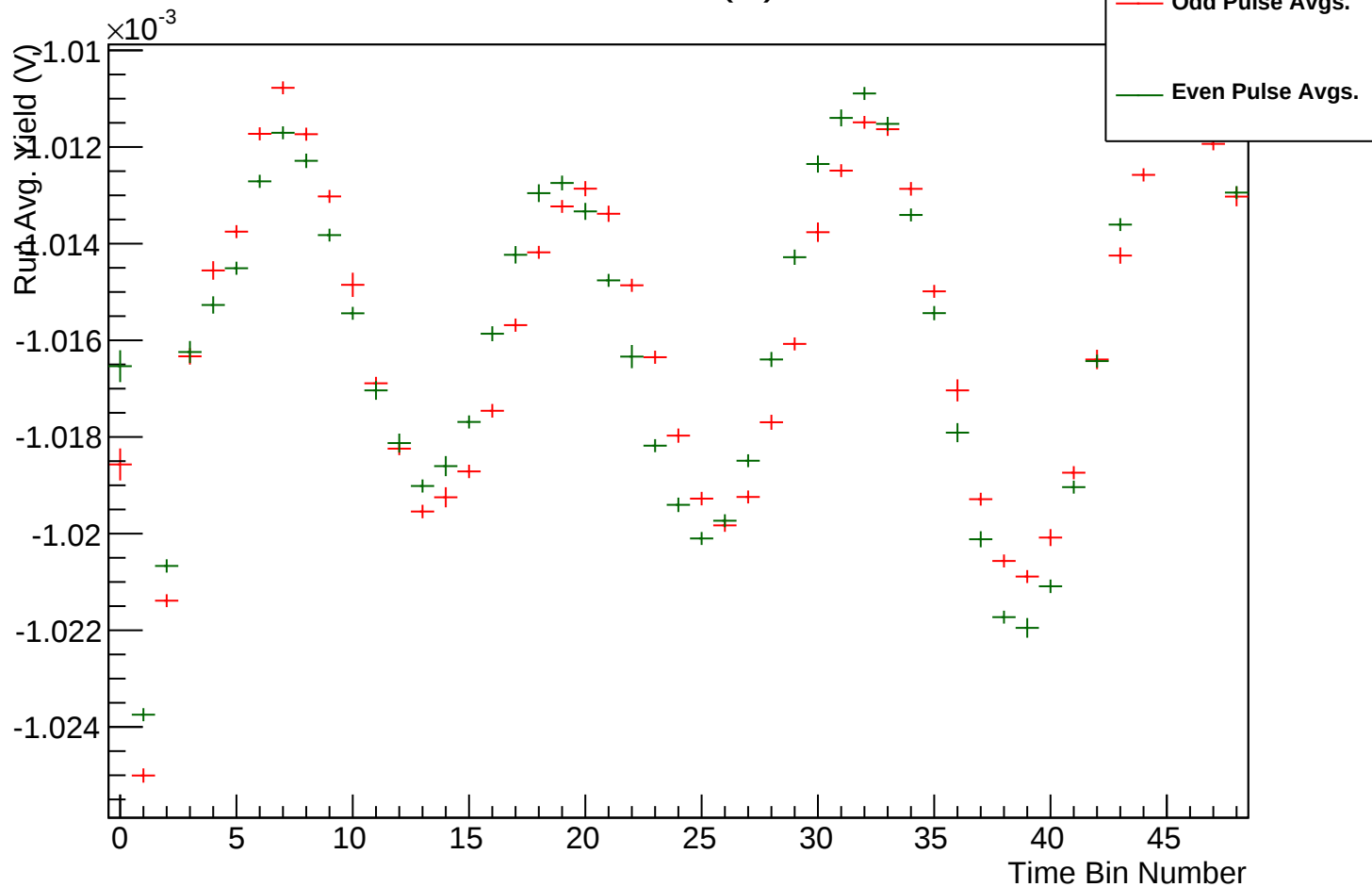
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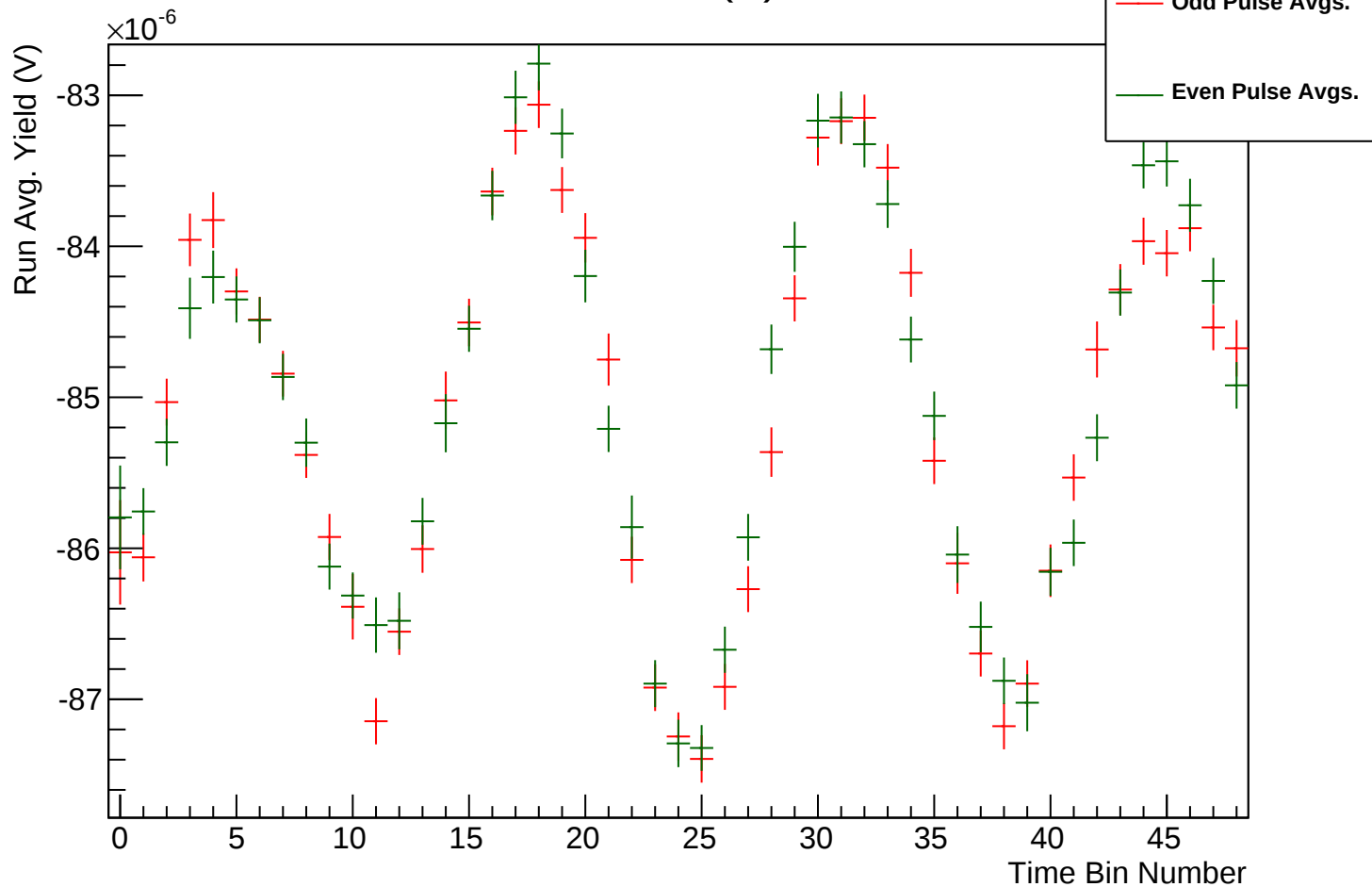
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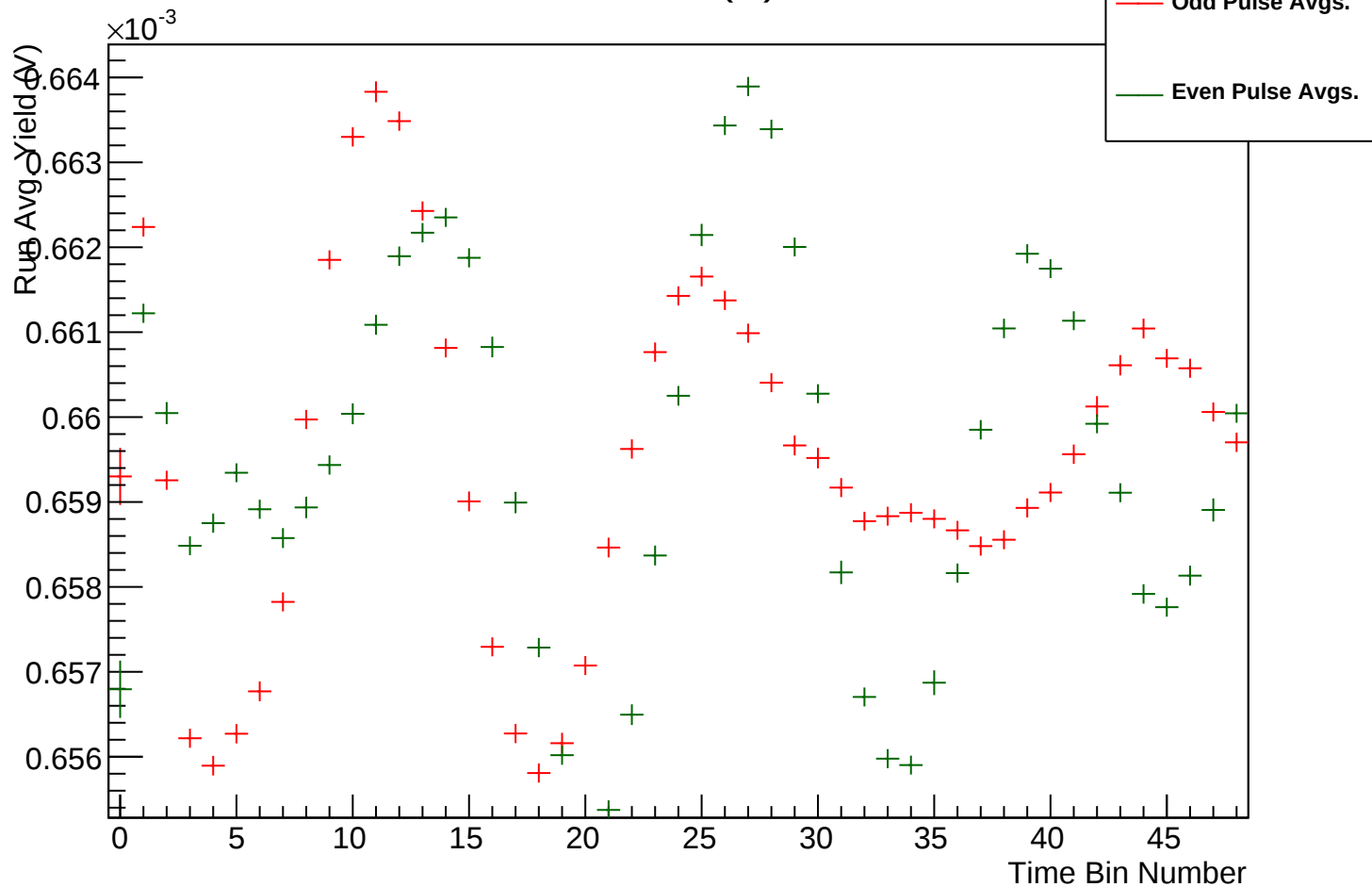
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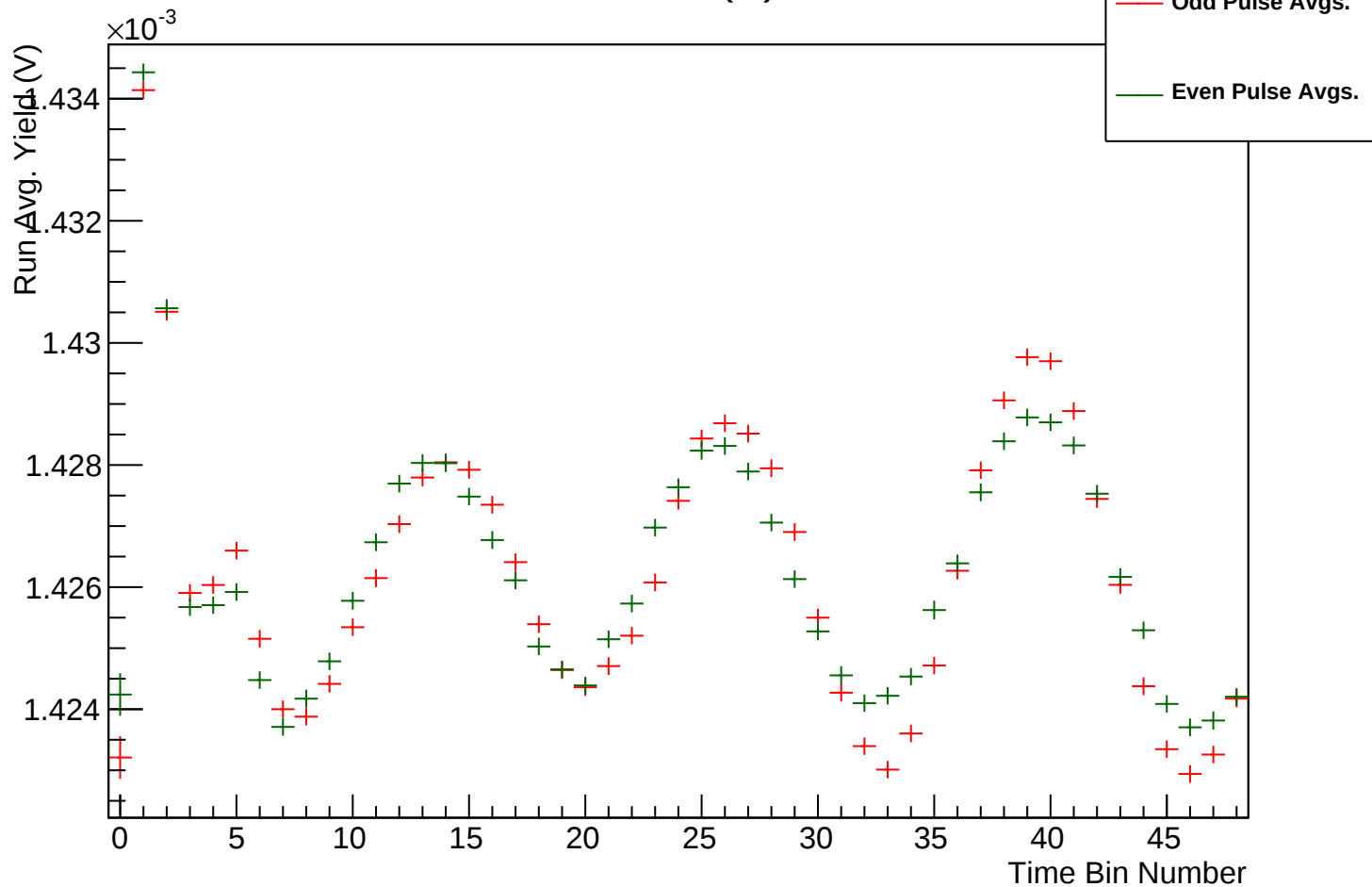
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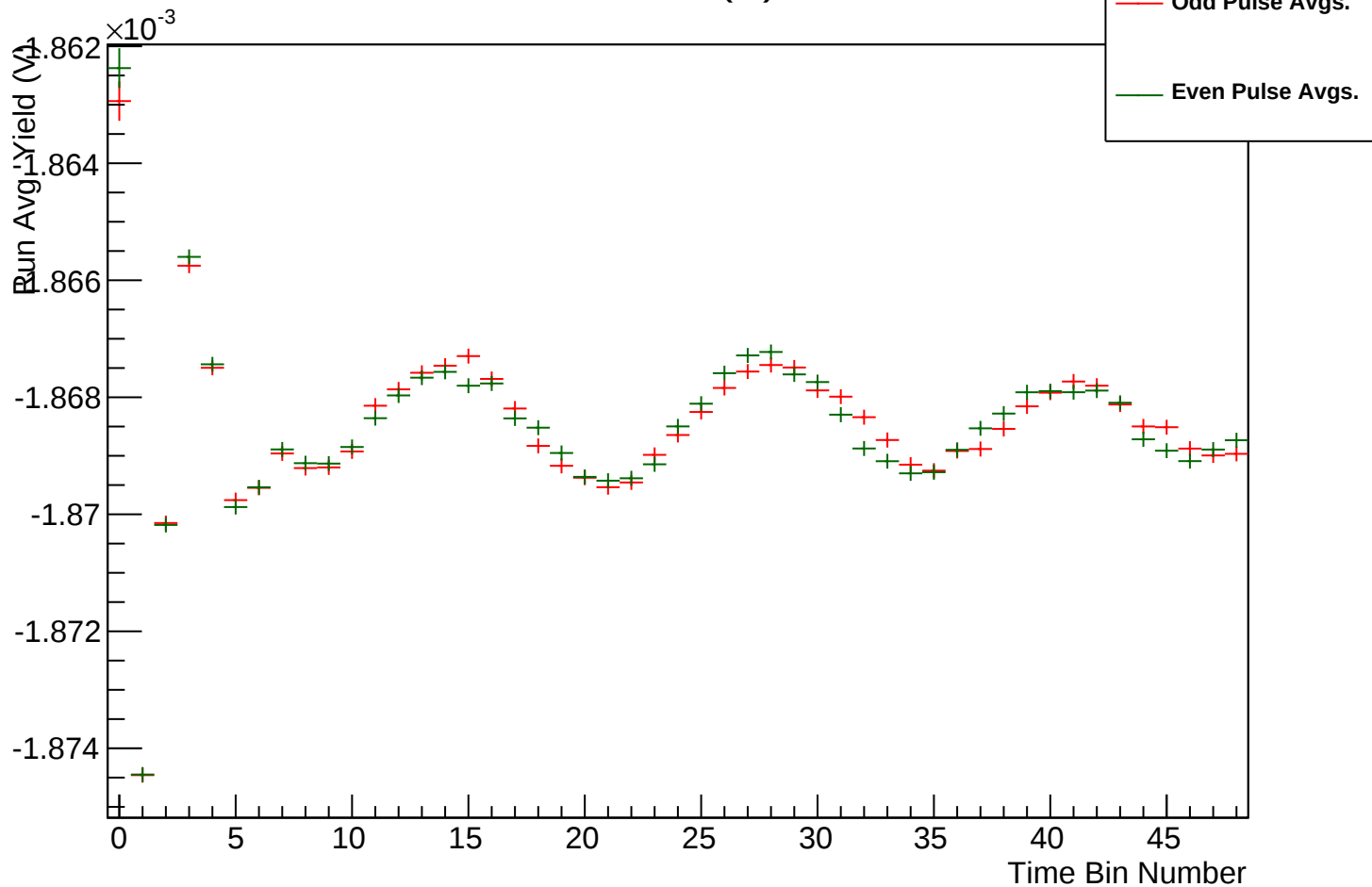
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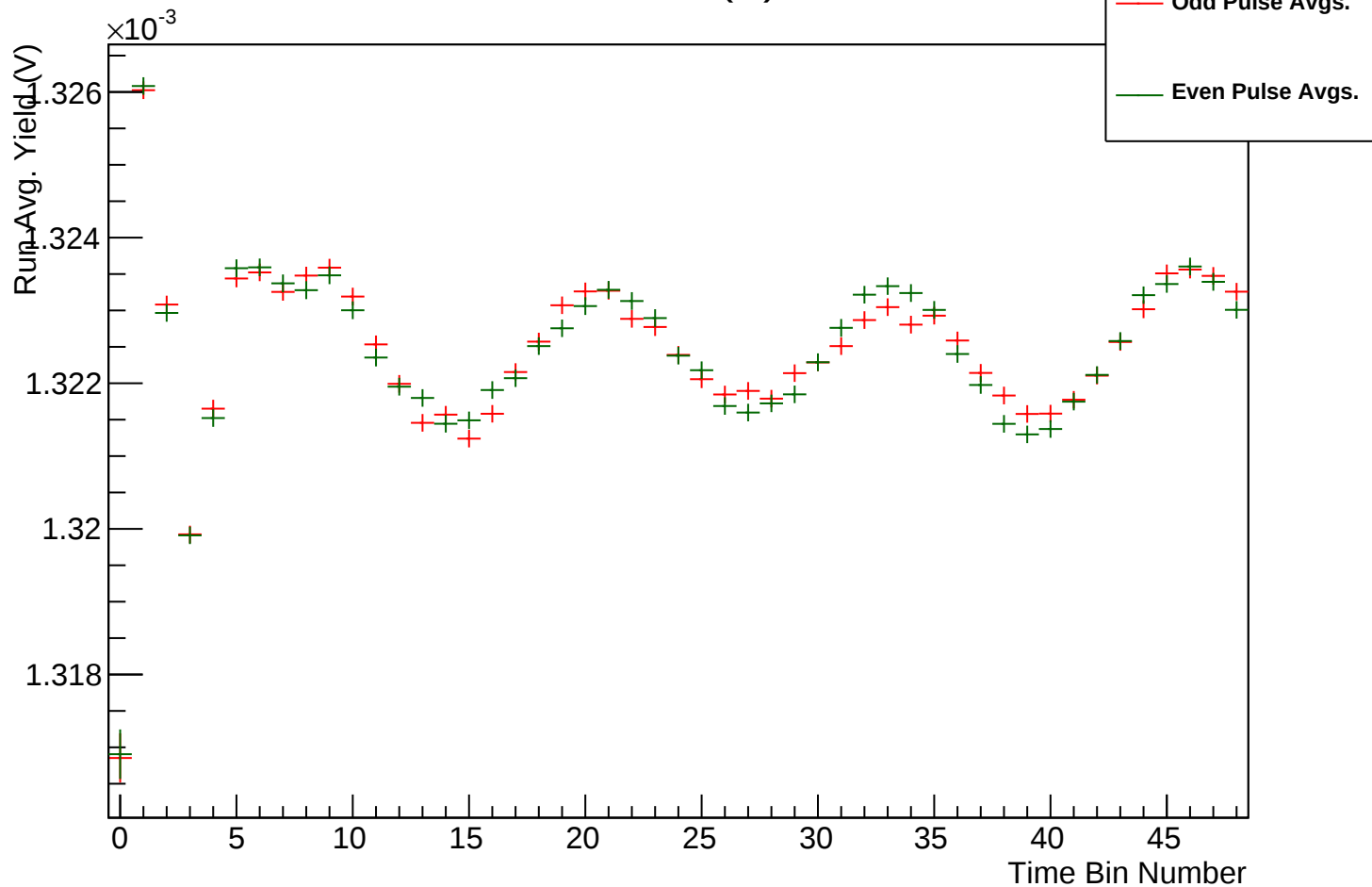
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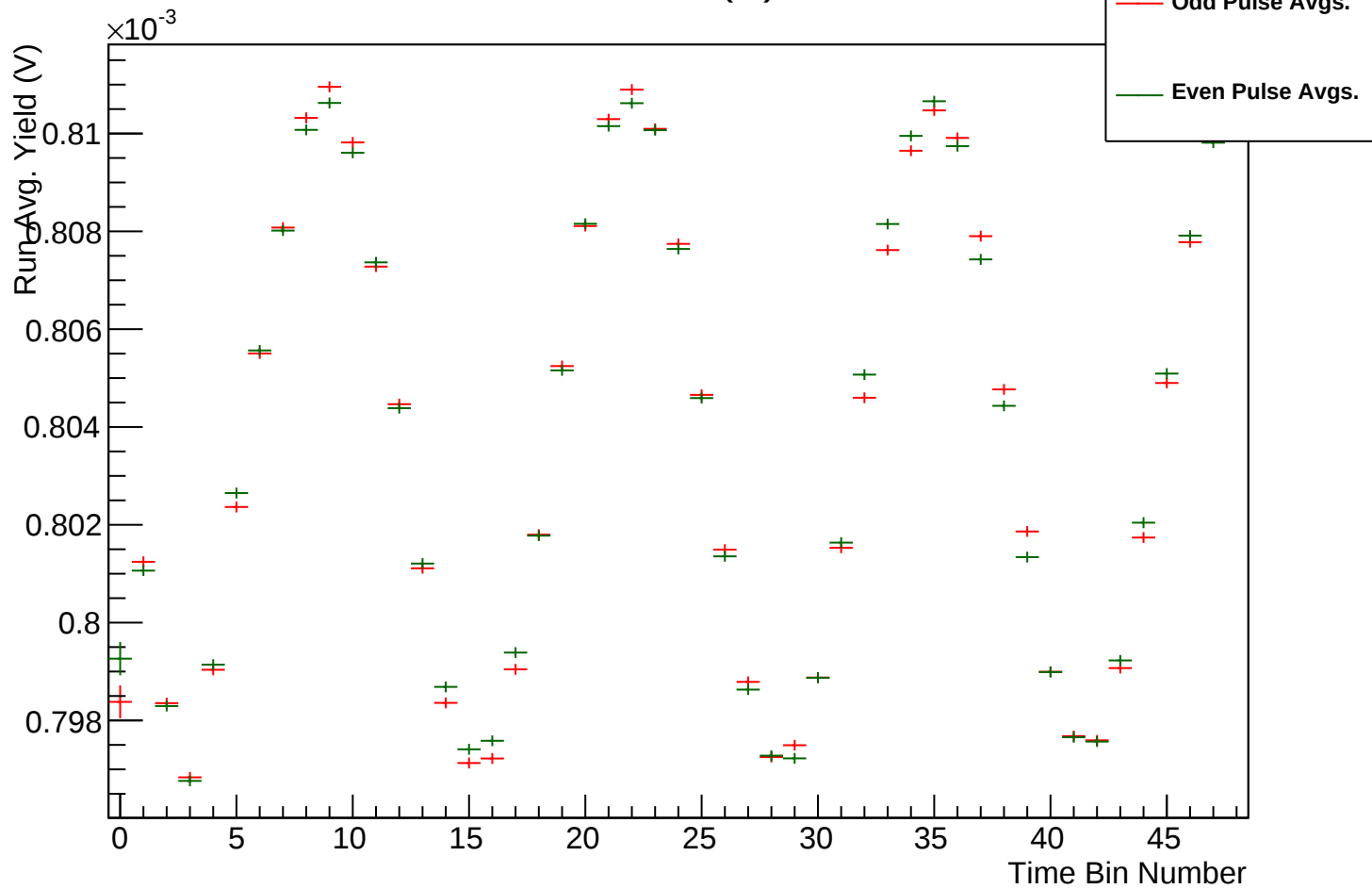
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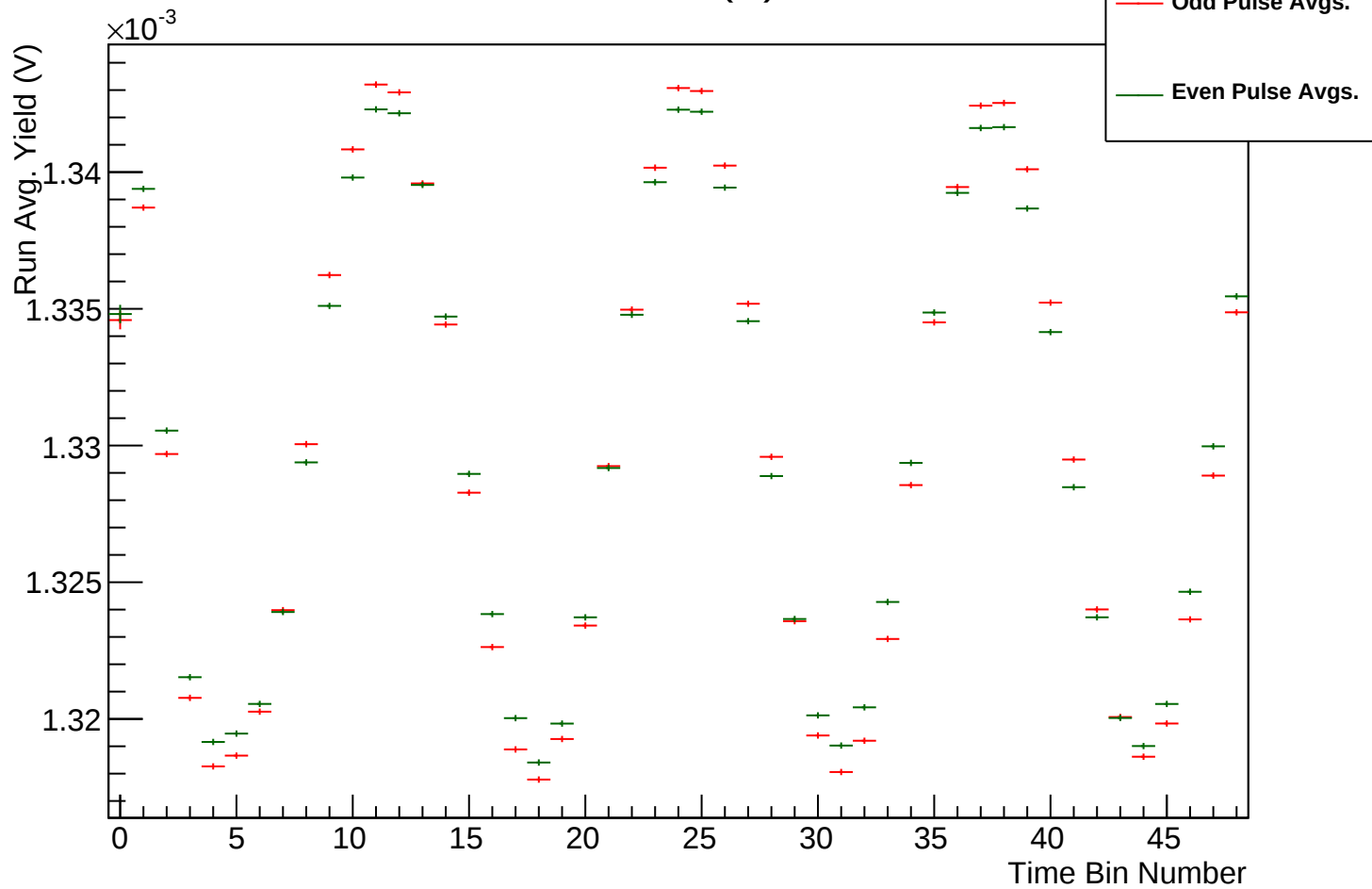
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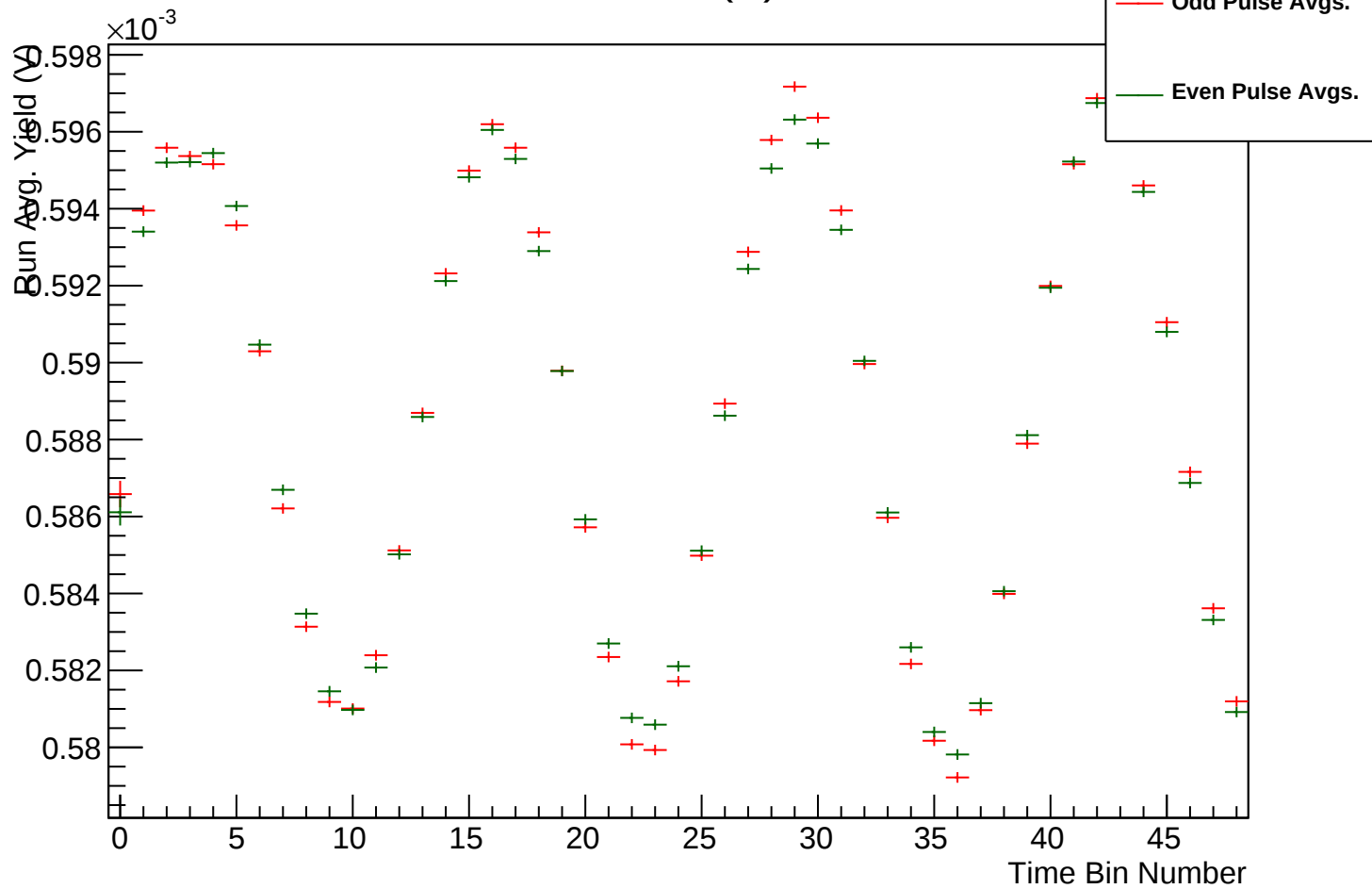
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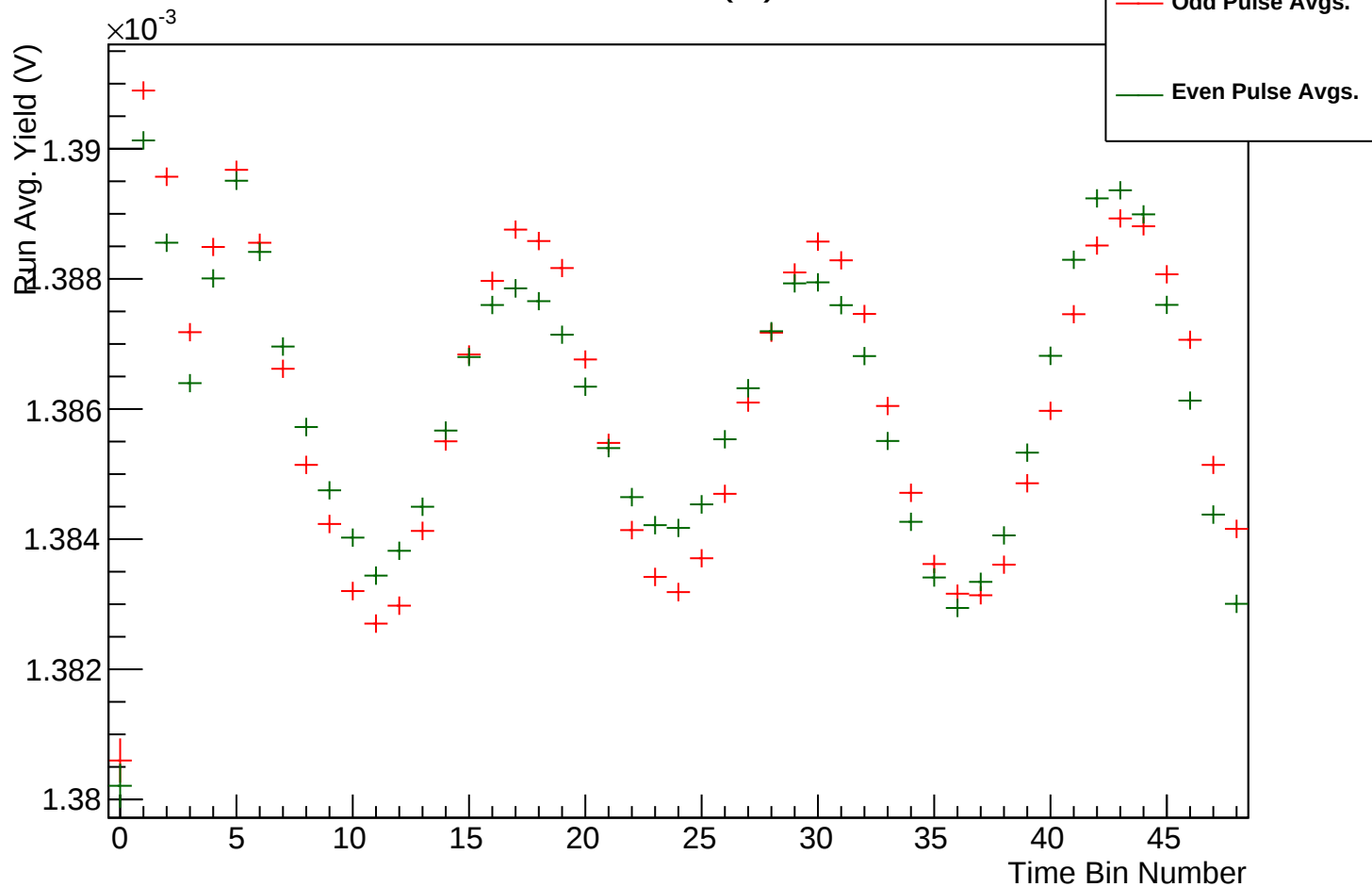
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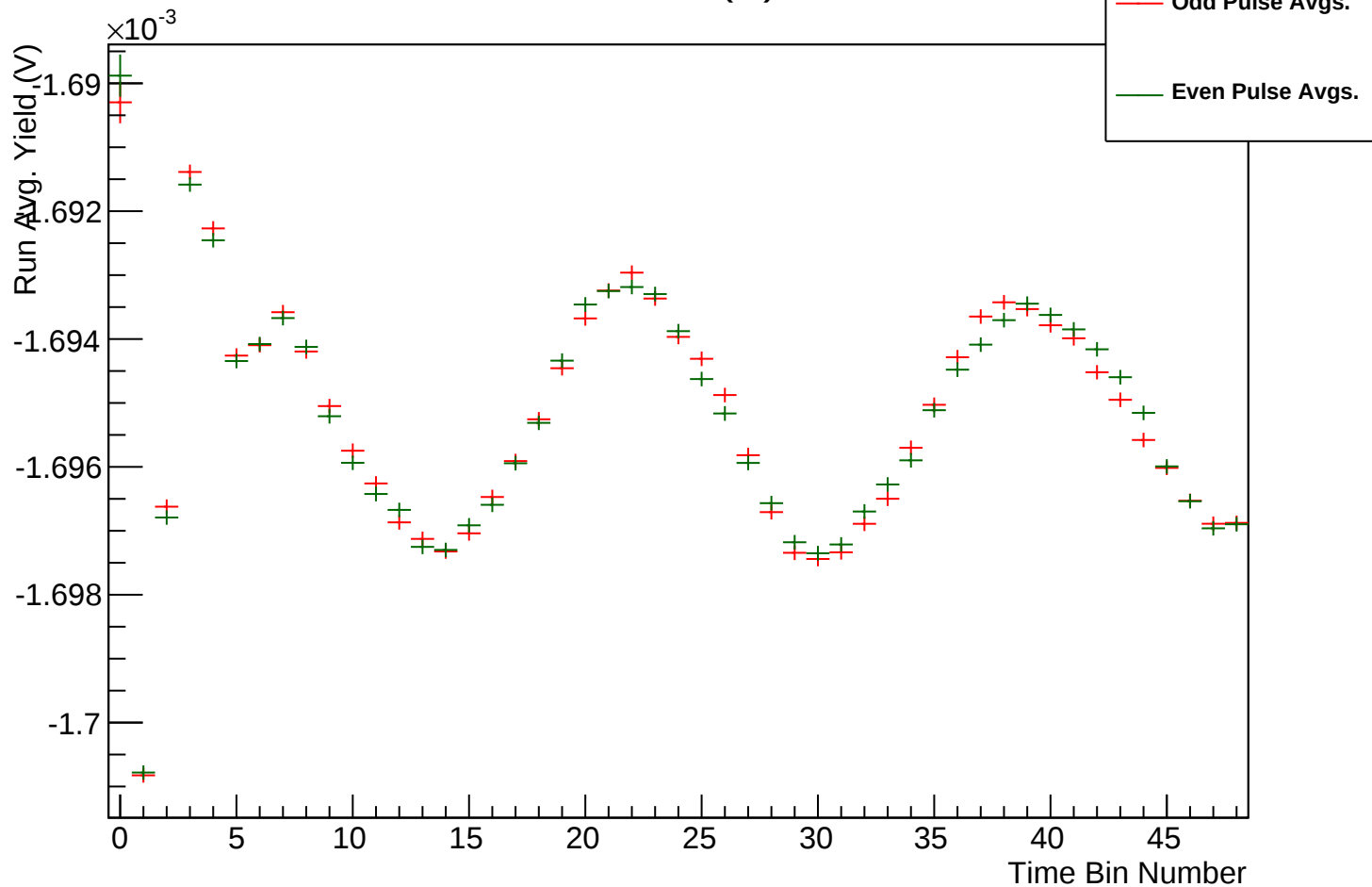
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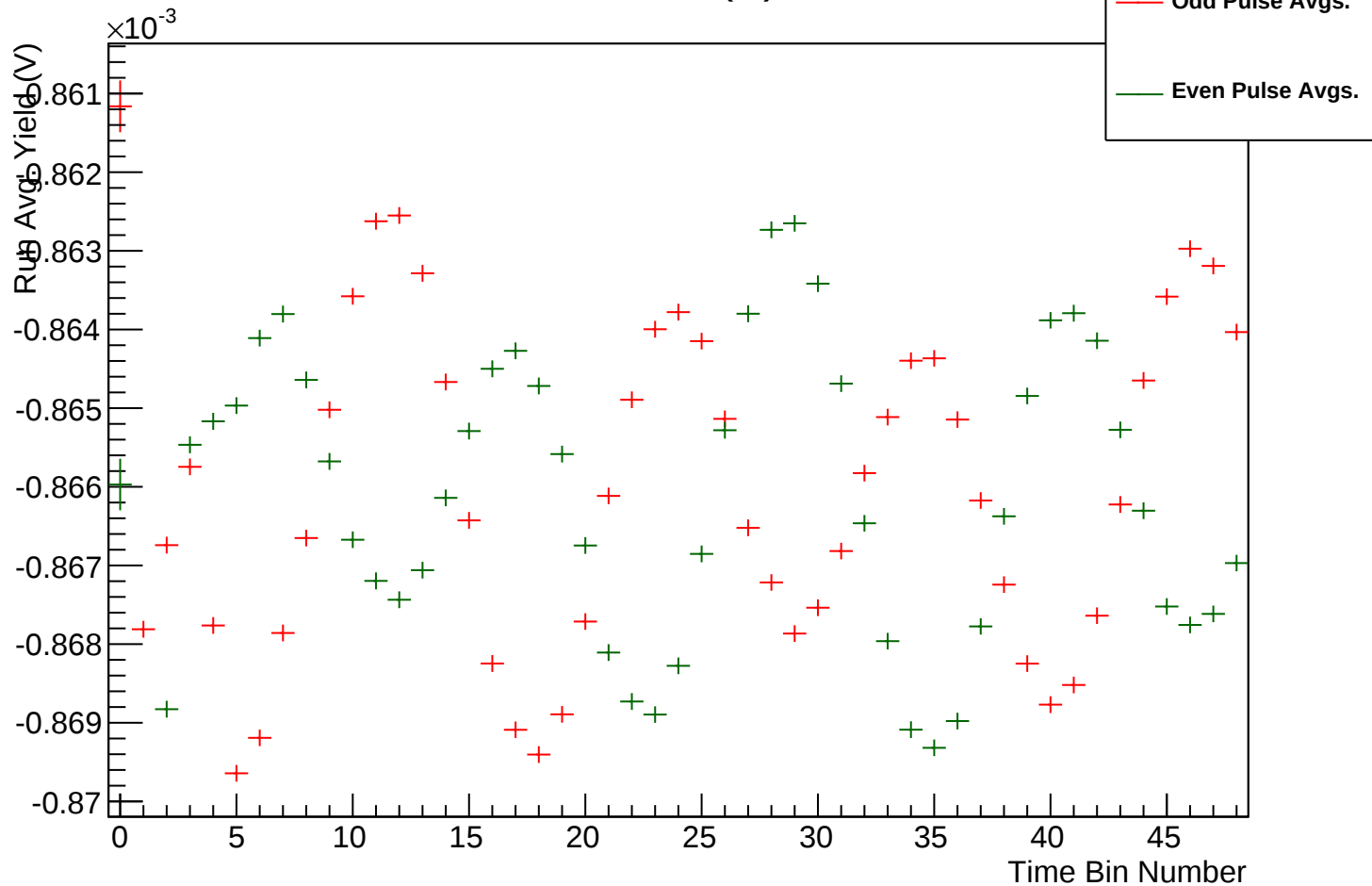
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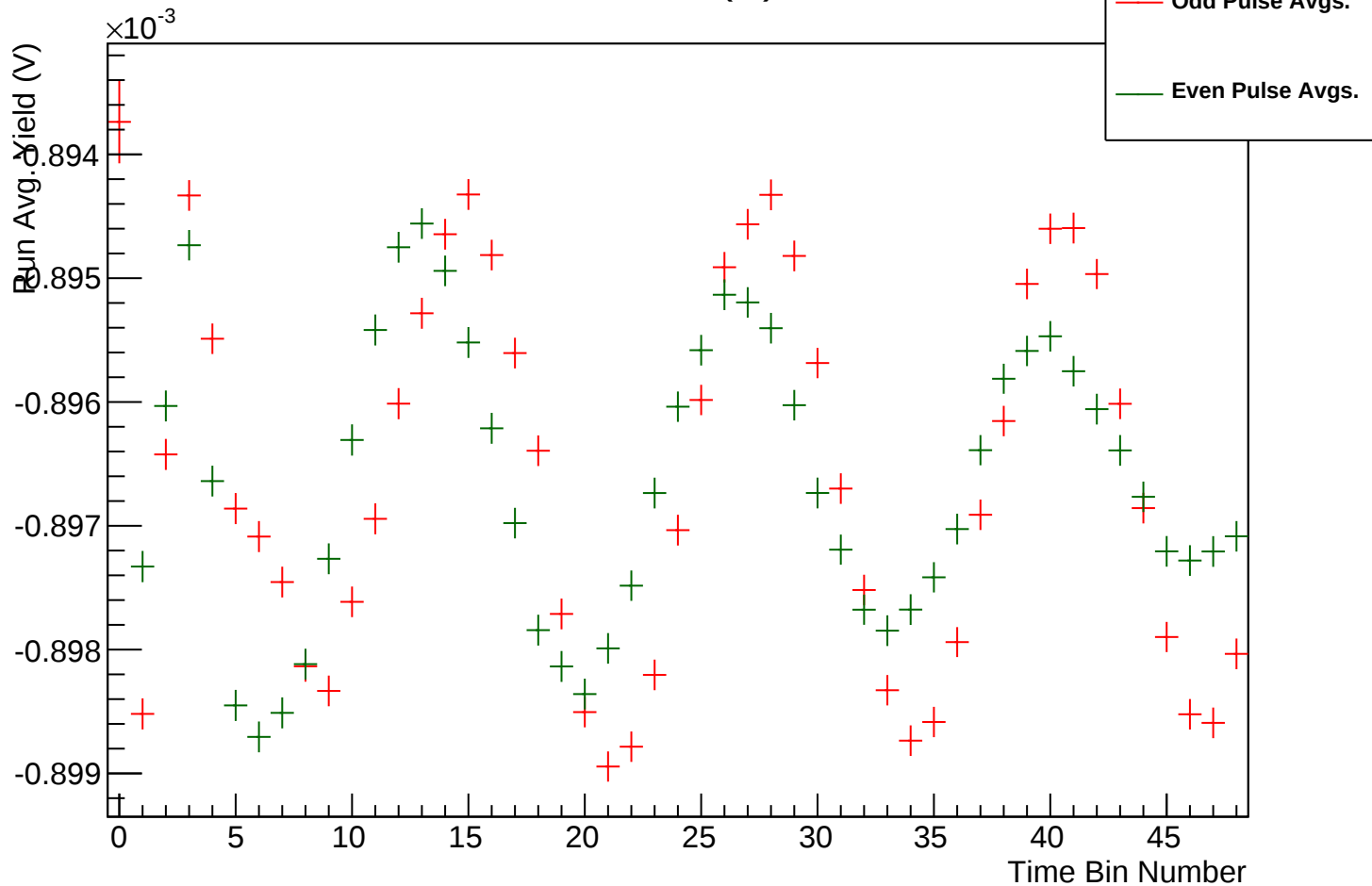
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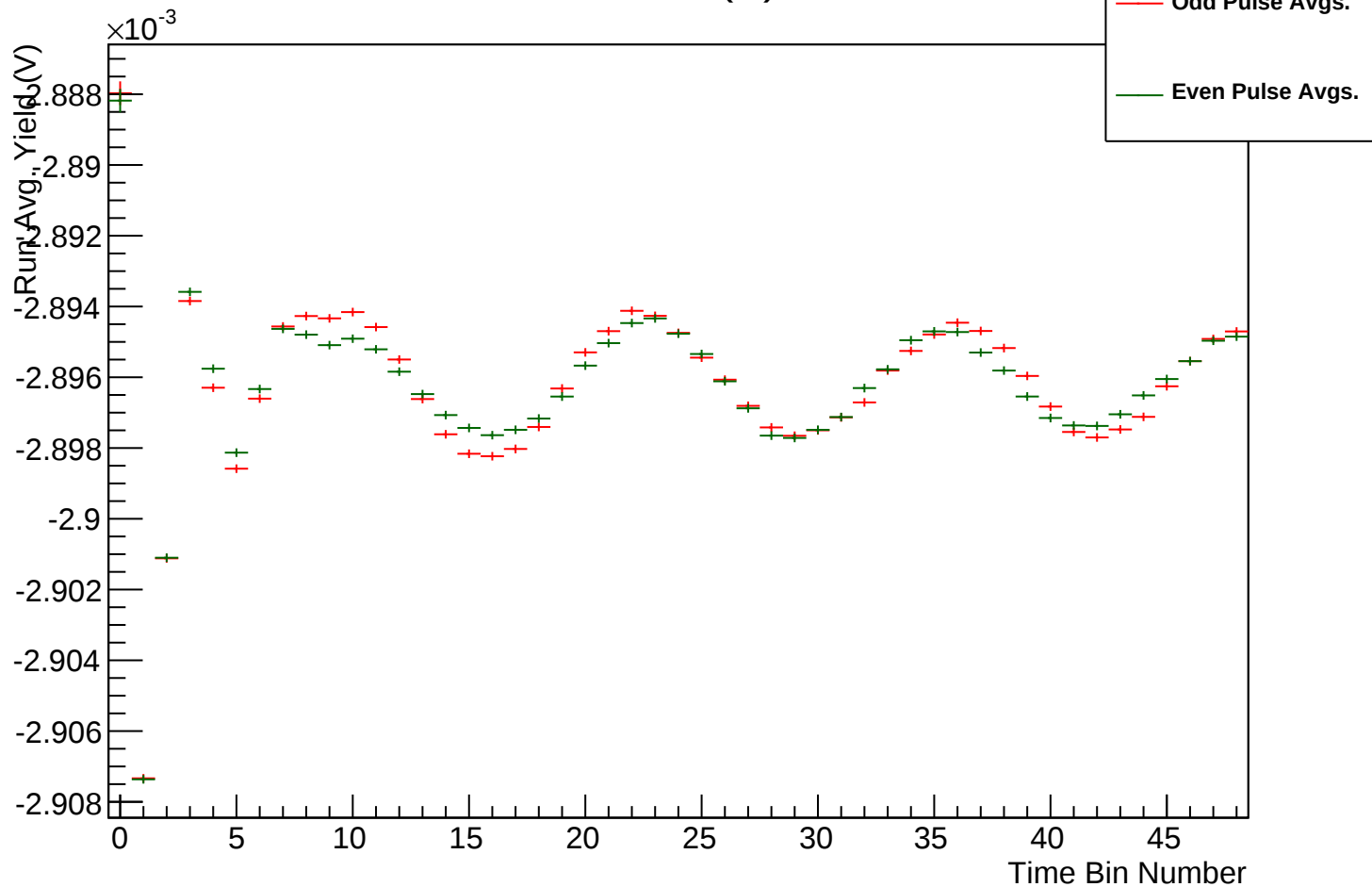
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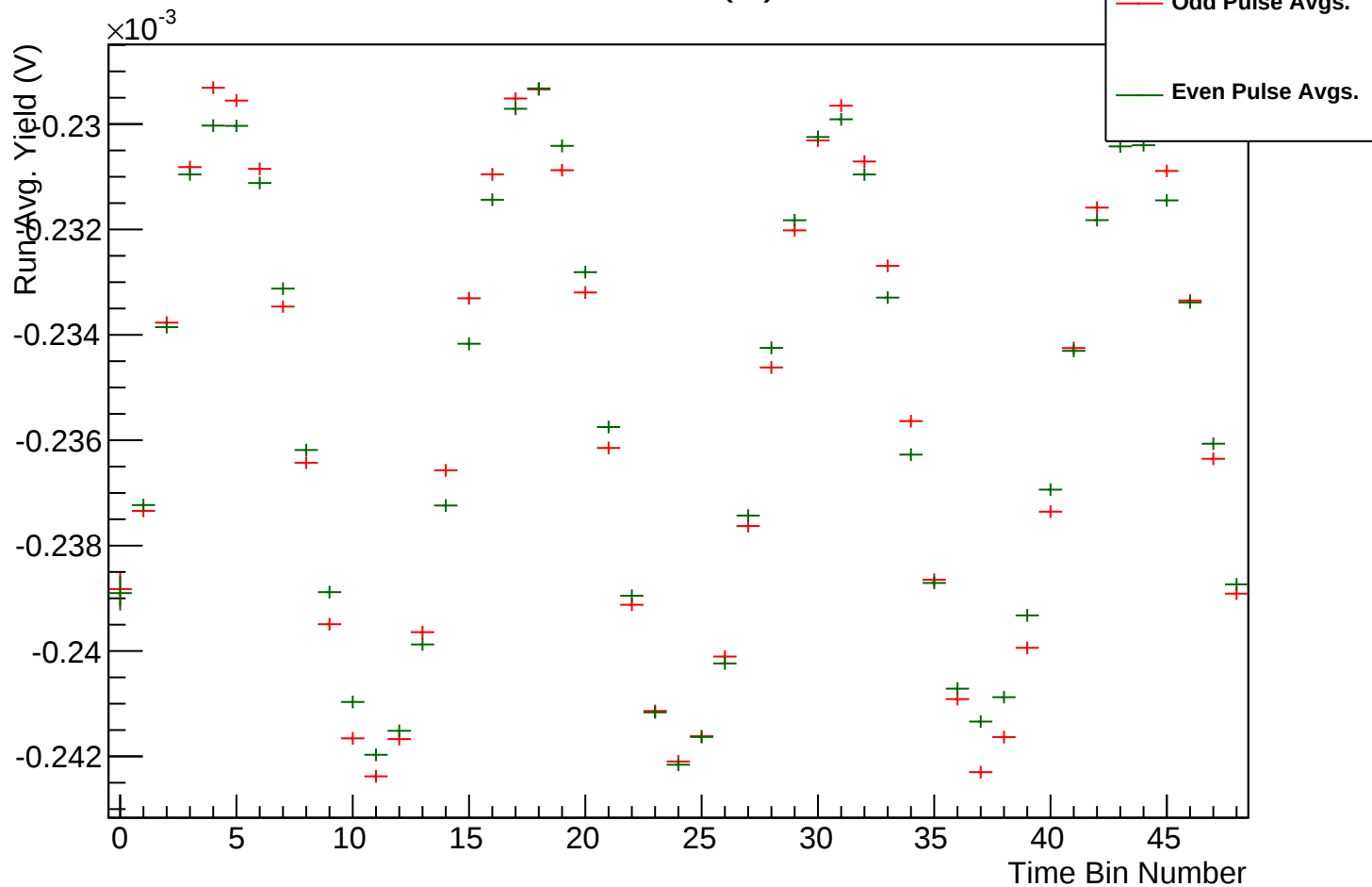
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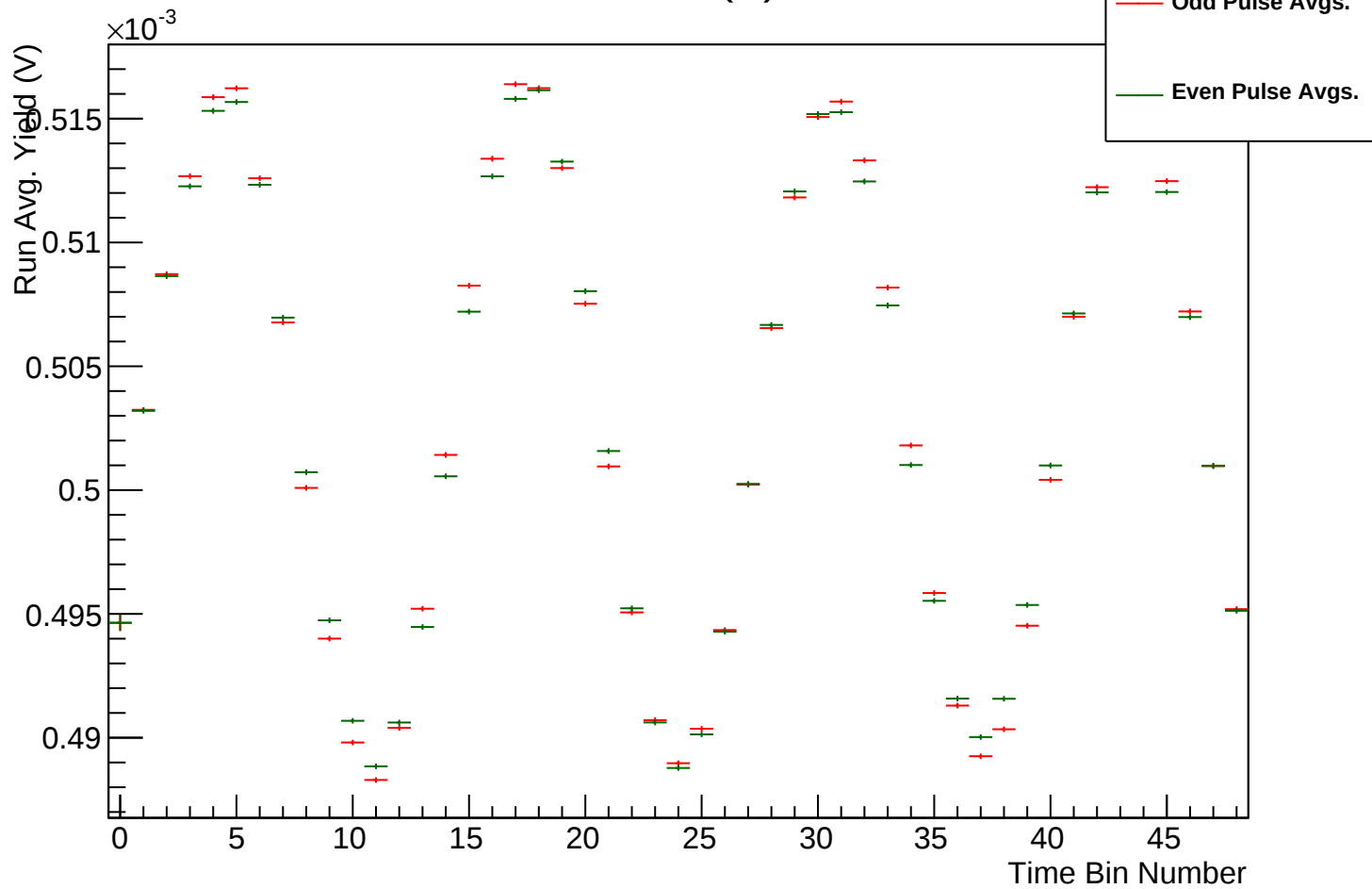
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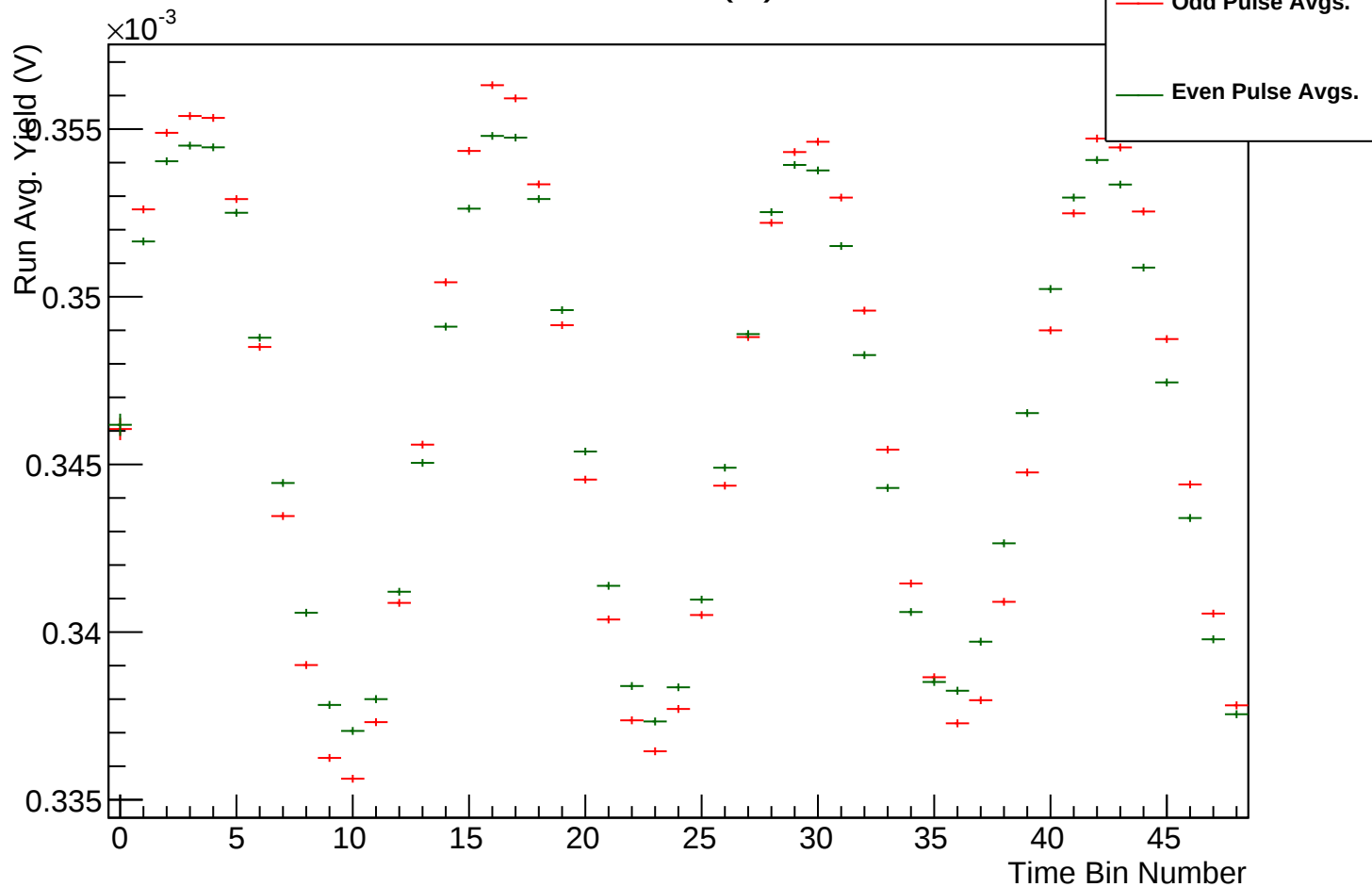
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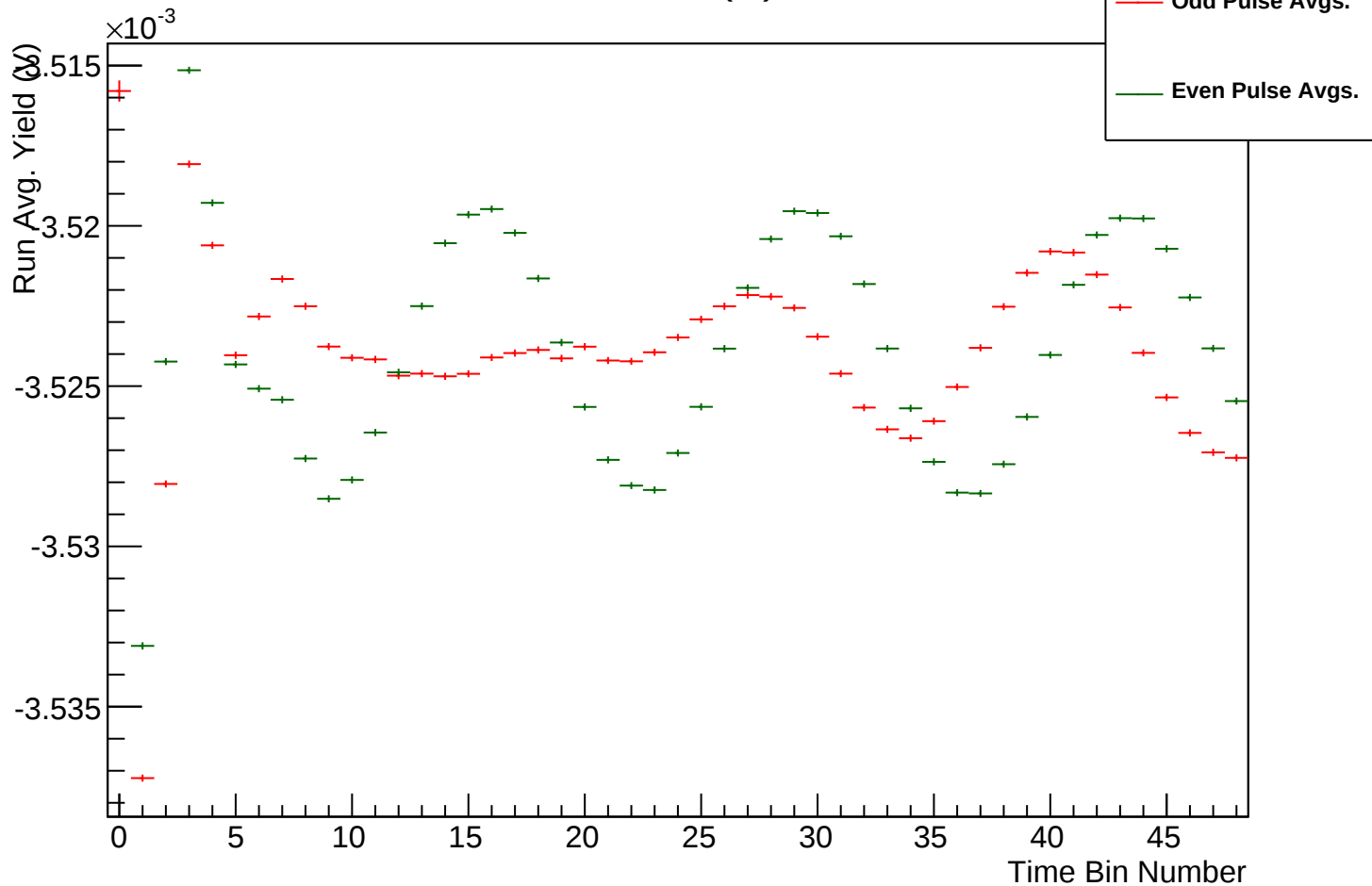
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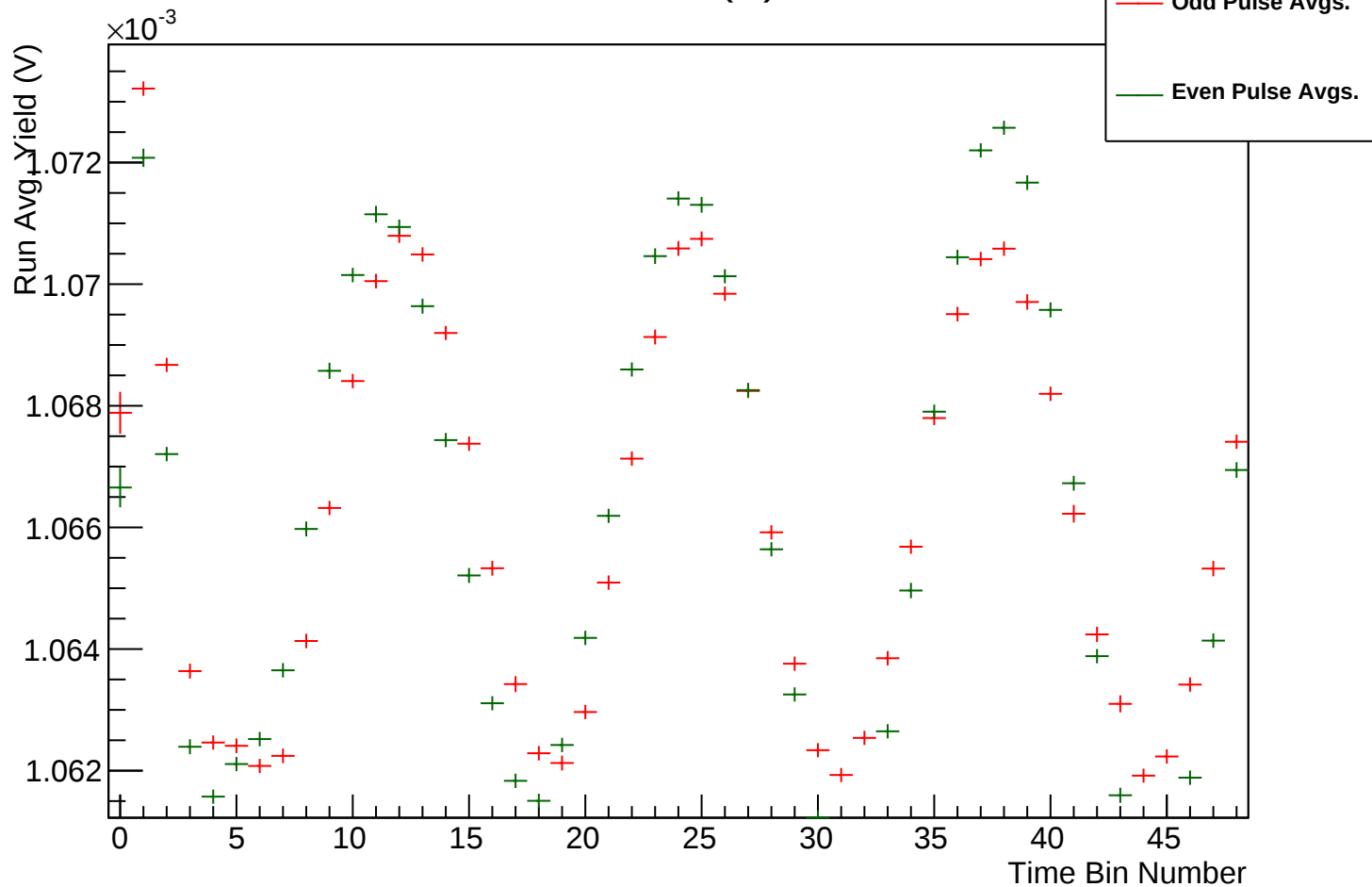
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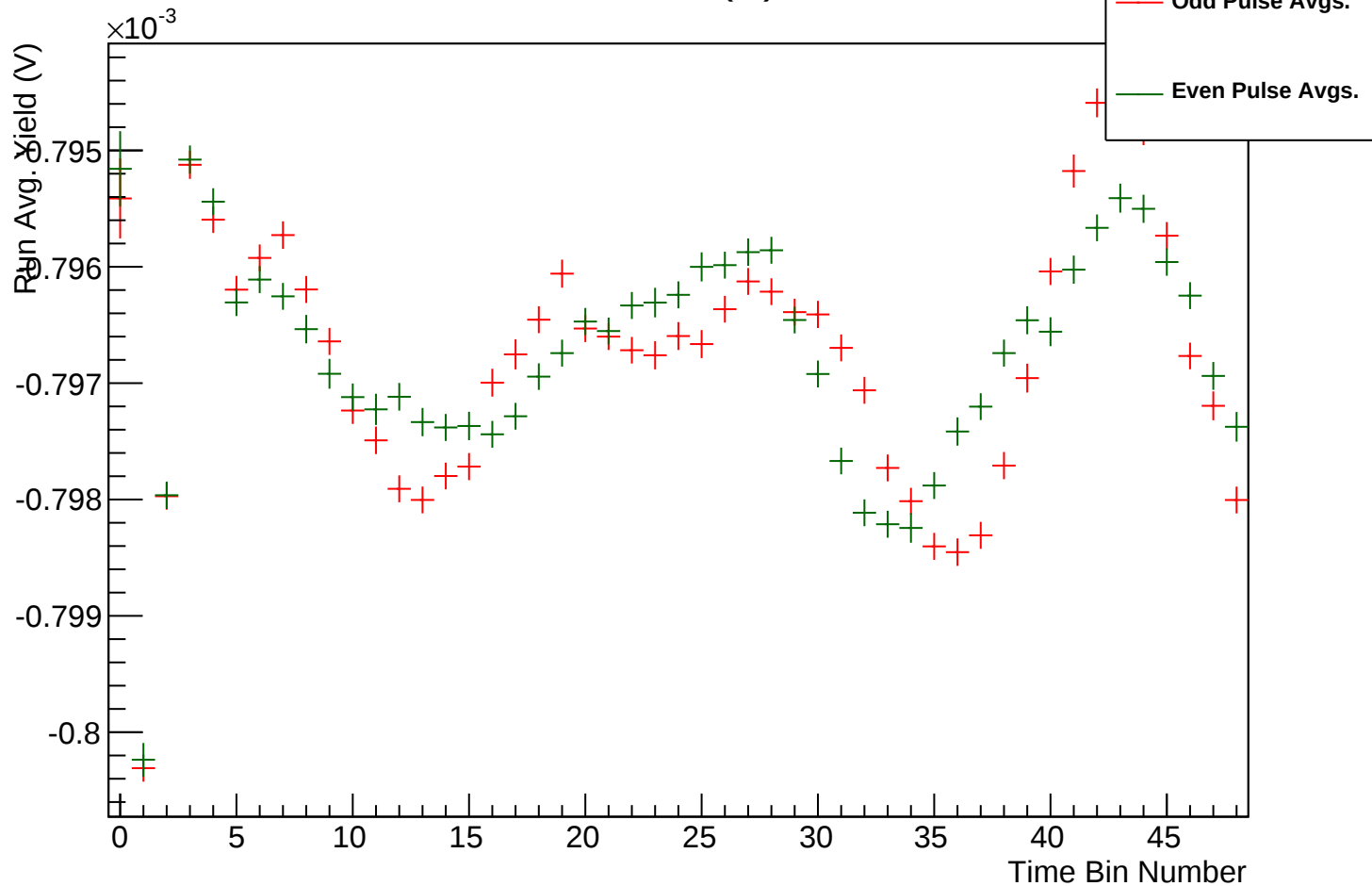
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Create on Date: Mon Aug 21 17:23:11 2017

Created by: M. McCrea

Created from: TBinPlots-WireYields.C

Date Source: TTreeRaw(38314)

Data Format Info:

this file contains the run average wire yield

for all time bins of all 144 wires for even odd and.

other pulse combinations.