Data Acquisition System(DAQ) for the n-^{3}He Experiment at SNS

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DAQ for n^{3}He

Outline

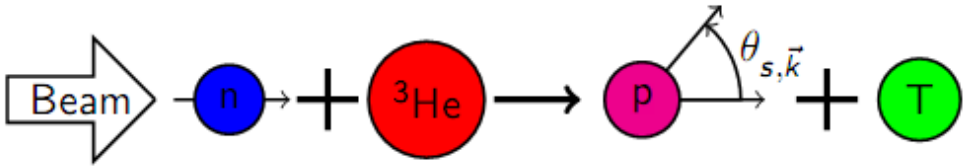
Outline

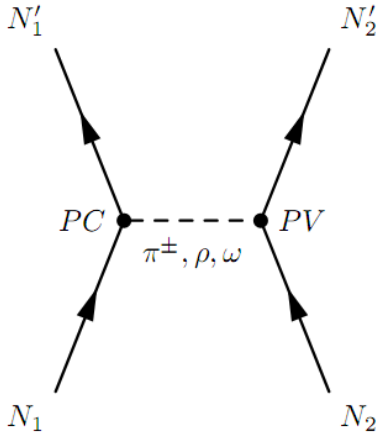
- The n-^{3}He experiment
  - Motivation
  - Experimental Setup
- DAQ for n-^{3}He experiment
  - Expectations
  - ADC modules
  - A Complete Network
- Measurements
  - ADC noise and rise time
  - Resynchronization and Jitter
  - Averaging
  - Instrumental Asymmetry
- Future Plan

The n-^{3}He Experiment

- High-precision measurement motivated to probe the hadronic weak interaction by measuring the parity violating asymmetry of the proton in the reaction -

$$\vec{n} + {}^3He \rightarrow p + T + 765keV$$





- Expected to be extremely small (of the order 10^{-7})
- Goal is to measure an asymmetry in the reaction to a precision of 2×10^{-8}

DAQ for n^{3}He

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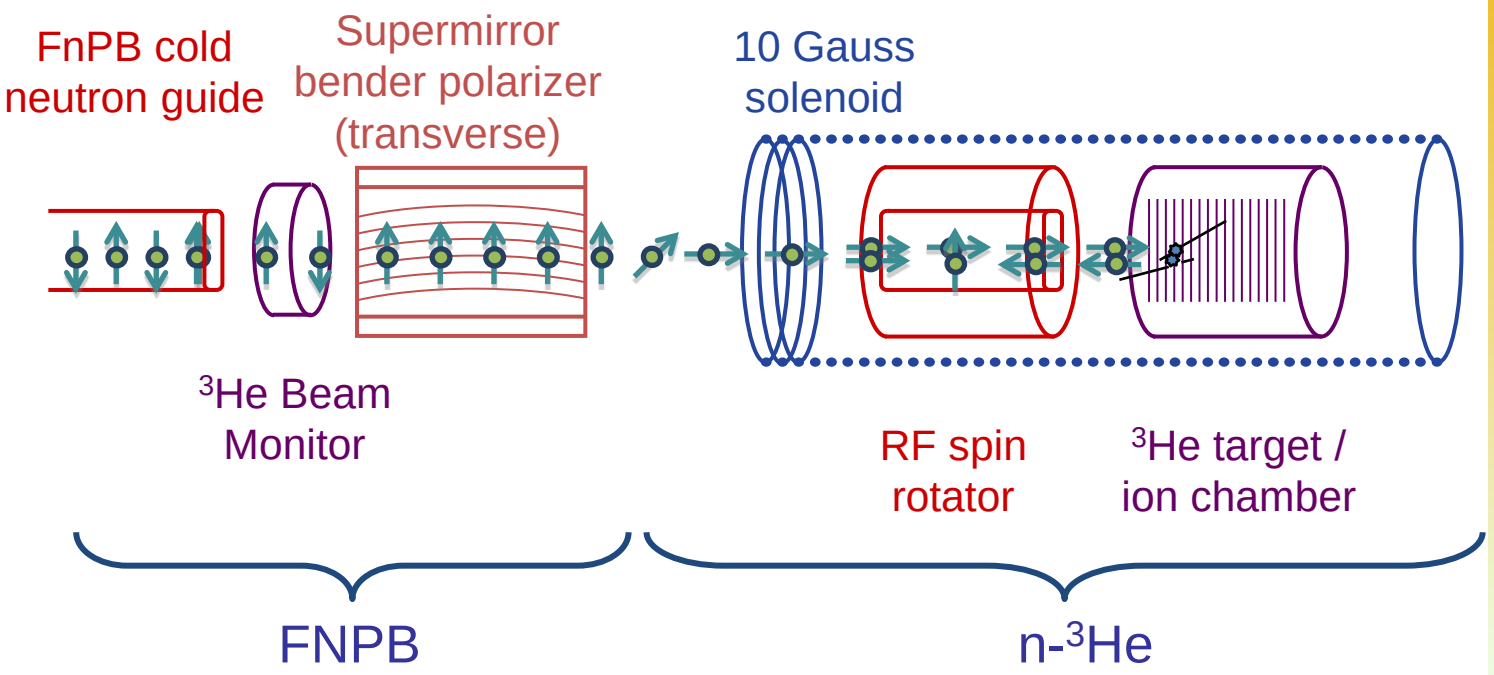
Experimental Setup



- n-^{3}He is using a spin flipper with transverse windings which allows for both longitudinal and transverse spin rotation.
- ^{3}He ion chamber – both target and detector.
- Detectors work in current mode.

DAQ for n^{3}He

DAQ for n-^{3}He – Expectations in general

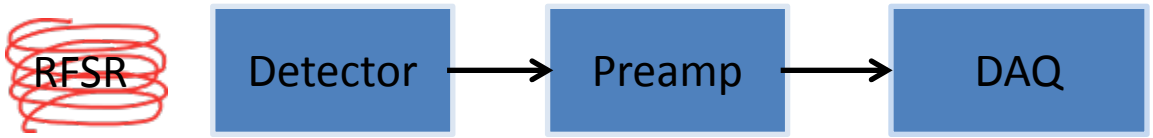
- Large amount of data, high sample rate but very low ADC noise.
- High channel density with simultaneous input.
- Jitter of the order of nanoseconds.
- Maximum sampling rate but the file size manageable /durable.
- Triggering using software taking accelerator T_0 as input.
- Can take data only in our region of interest.
- Time bin and the number of entries per run can be adjusted.
- Synchronization of all the ADC modules with T_0
- Checksum algorithm to detect corrupt data .
- Built in event header.

DAQ for n-^{3}He –Expectations for systematics

- 1st plane of the detector : 10 V → Full Scale
- Back plane of the detector: 0.1% of Full Scale
- Size of asymmetry: $A \sim 10^{-7}$
- Expected uncertainty in asymmetry : $\Delta A = 2 \times 10^{-8}$ (Statistical)
- Expected maximum contribution from systematics:

$$\Delta A_{sys} = 10\% \text{ of } \Delta A$$

- Expected $\Delta A_{sys} < 10^{-9}$



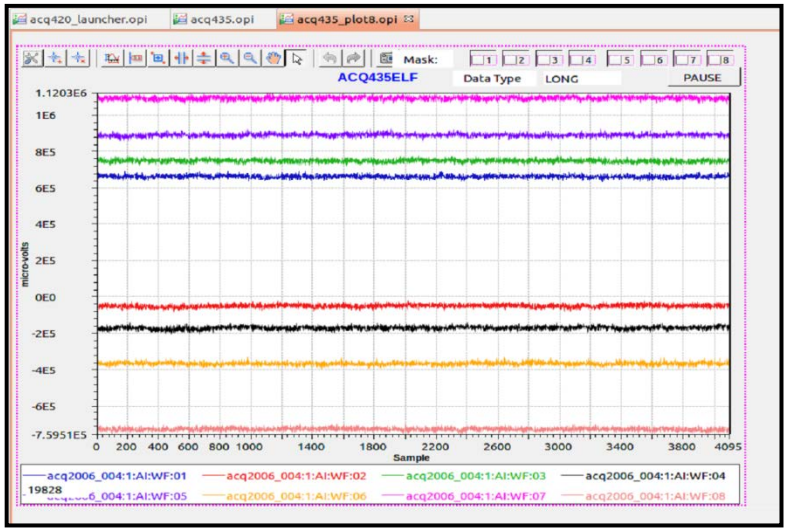
Then the biggest challenge becomes achieving this ΔA_{sys} , provided that the spin flipper in the experiment will be turning on and off at 30Hz.

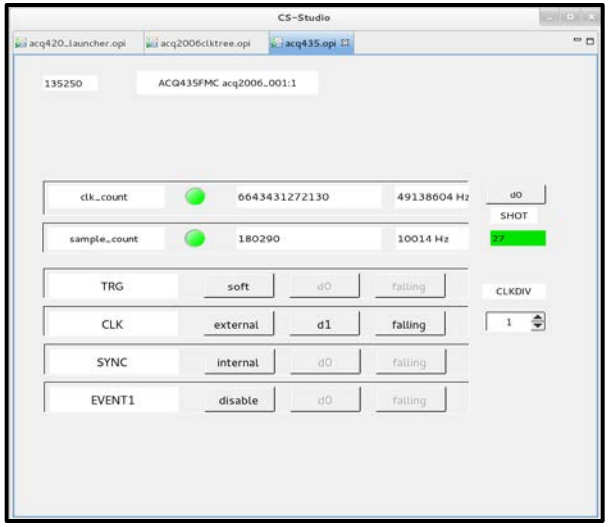
DAQ for n-^{3}He -ADC Modules

- Delta sigma technology based ADC (ACQ1002) by d-tAcq Solutions.
- Zynq 7000 –series hybrid FPGA + 2 ARM CPU cores + FMC
- 24 bit ADC per channel for true simultaneous analog input.
- Maximum sampling rate 128 kSPS (min is 8 kSPS) per channel.
- 2x24 Channels per module.
- Signal to noise ratio is 104 dB (high speed) or 108 dB (high resolution)
- 1GB DDR memory on board.
- External clock, trigger, internal clock.
- Runs embedded Linux.
- Firmware on flash memory, can be updated easily.

ADC Modules

- The DAQ can be accessed through ssh or console.
- It has several separate sites for capture and configuration.
- The data is transferred and saved to control computer using TCP/IP connection(e.g. netcat).
- Supports EPICS CSS for controlling the DAQ.
- Data and run time parameters can be viewed in real time using CSS.





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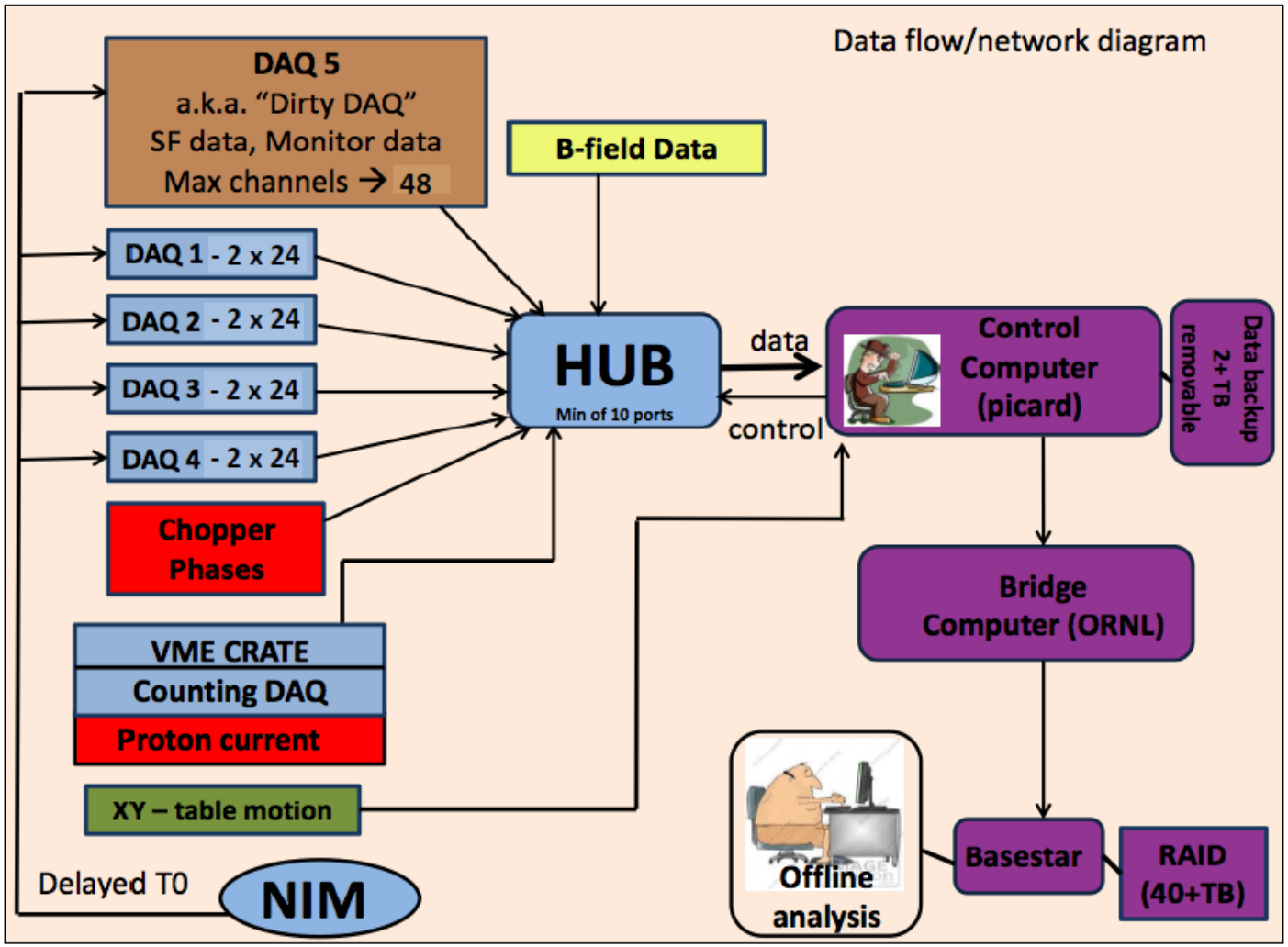
Future Plan

A Complete Network



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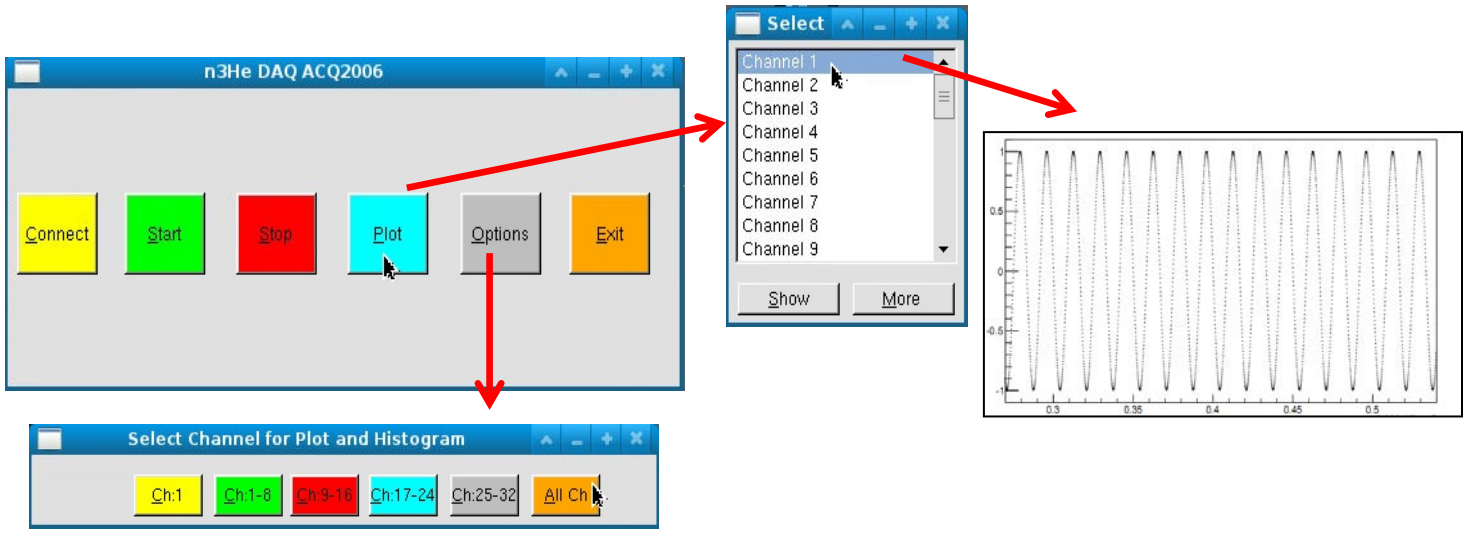
Software

- ❑Analyze the binary data with ROOT without saving as root file.
- ❑ TBranchBinary
  - Allows one to interpret binary files as ntuples without actually reading them into an ntuple.
  - Gives access to all features of TTree.
  - Access to any ROOT classes.
- ❑Prototype GUI with DAQ control and online analysis.
- ❑Prototype analysis library based on TBranchBinary.



DAQ for n^3He

Measurements : ADC noise and rise time

- Bare ADC noise was measured to be 27micro volt at 50KHz sample rate.
- Performance of ADC and its noise with different sample rate.

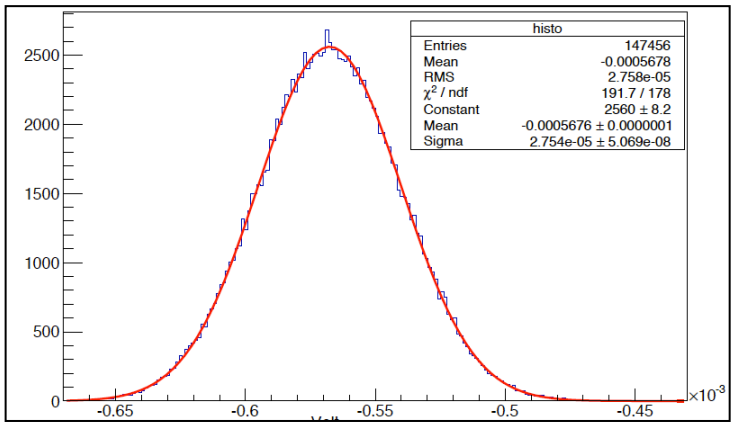


Fig: Bare ADC noise

- Based on counting statistics , running the DAQ at 50KHz and then averaging 20 successive points will give most optimal ADC noise.

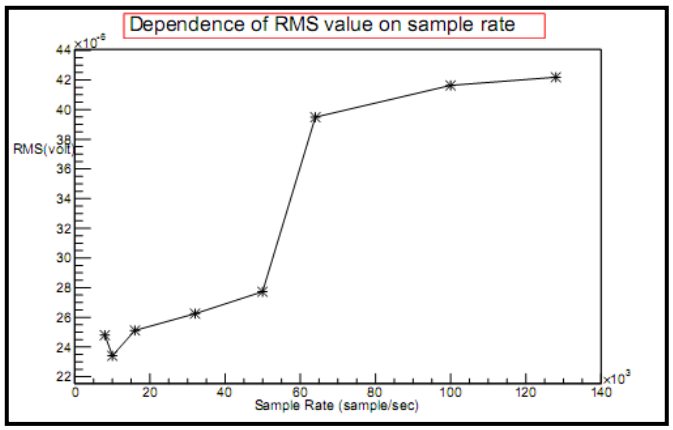


Fig: ADC noise vs sample rate

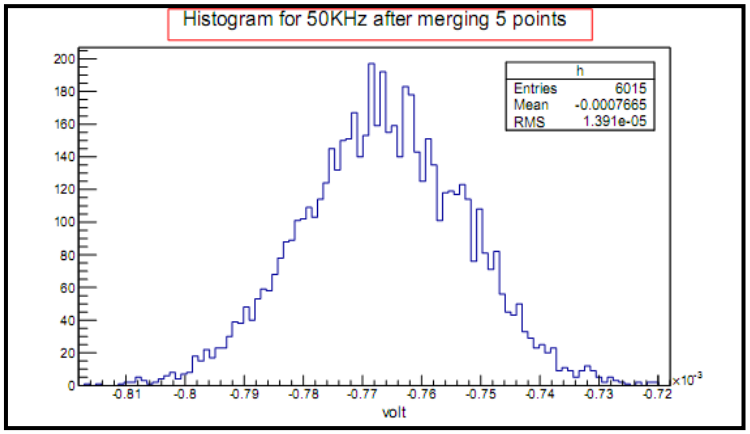


Fig: ADC noise after merging 5 points

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Measurements : ADC noise and rise time

- The rise time is found to be as expected.

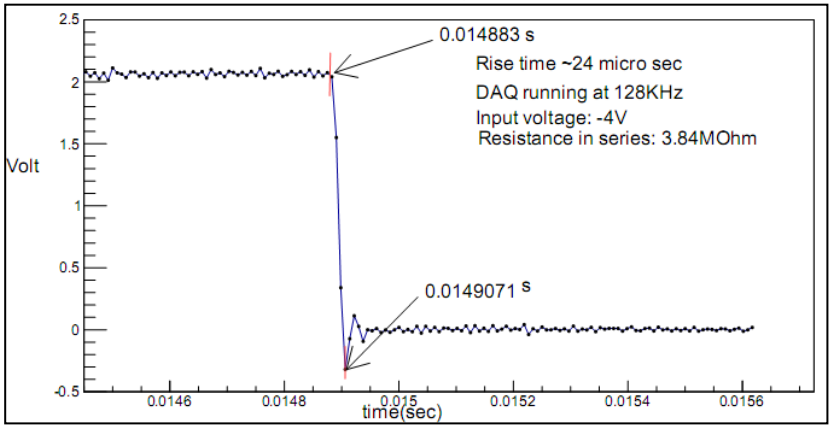

Fig: Plot for rise time

- The autocorrelation plot confirms no apparent correlation for ADC noise.

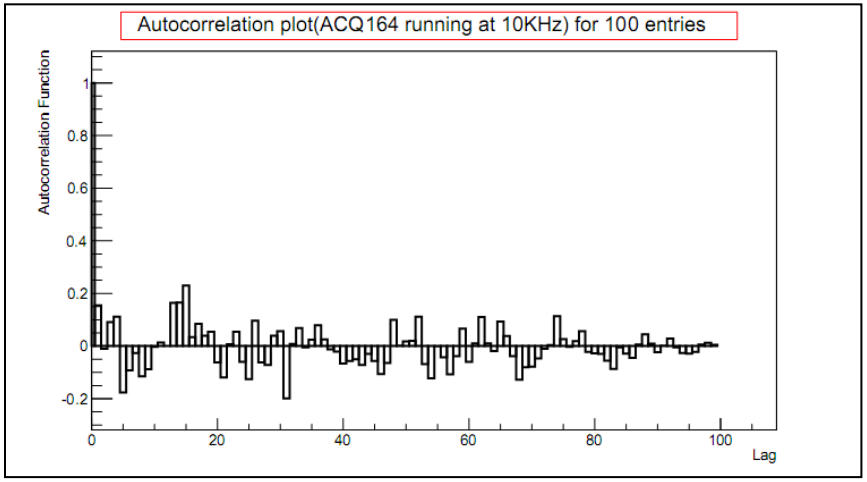

Fig: Autocorrelation plot

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Measurements : Resynchronization and Jitter

- 60 Hz pulsed signal with ramp is analyzed.
- Each rising edge of the pulse is fitted to the linear equation y=ax+b using least square method. This gives x-intercept and the slope of the rising edge.
- For each fit ,the x-value for the header is subtracted from the X-intercept of the rising edge. This constitute: $\Delta t-=t_i-t_0$ Where, t_i=Intercept from fit t_0= x-value for header This is done for all the pulses.
- Δt vs pulse number is plotted.
- A histogram for all the Δt is drawn.

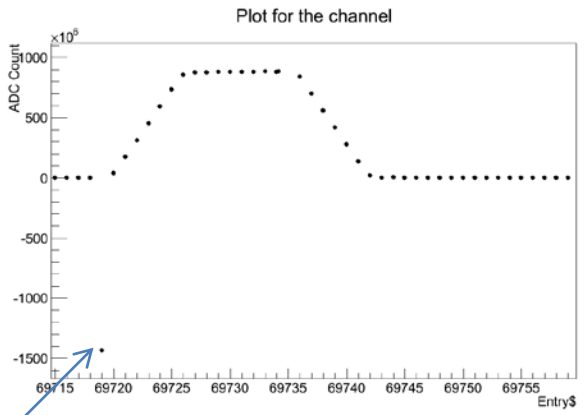

Fig: Signal with rising and falling edge with header

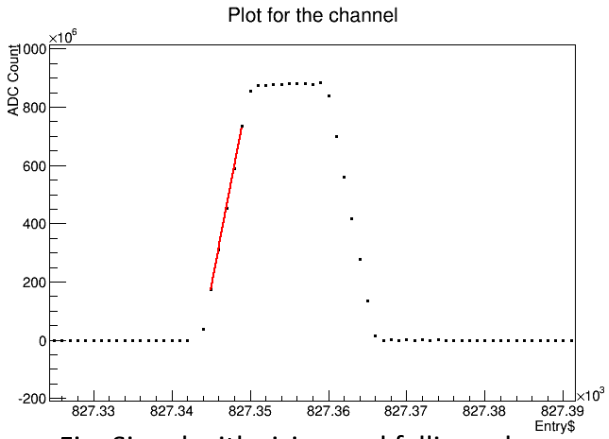

Fig: Signal with rising and falling edge

Units:
X-axis: 1 Entry= 1 Sample= 1/50KHz =20µs
Y-axis: 1 ADC count= 20Volt /2^{32} = 4.656 x10^{-09} Volt

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Measurements : Resynchronization and Jitter

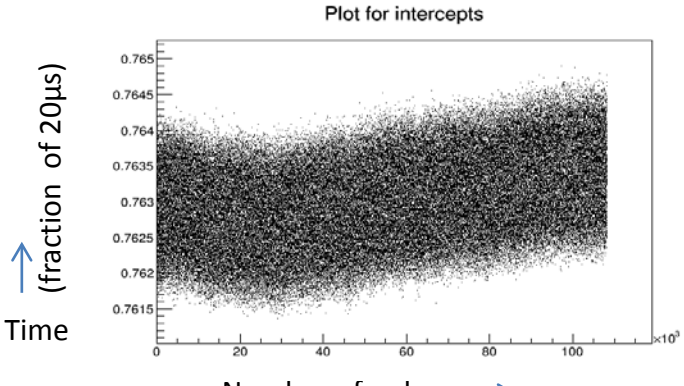

Fig: Plot for intercepts

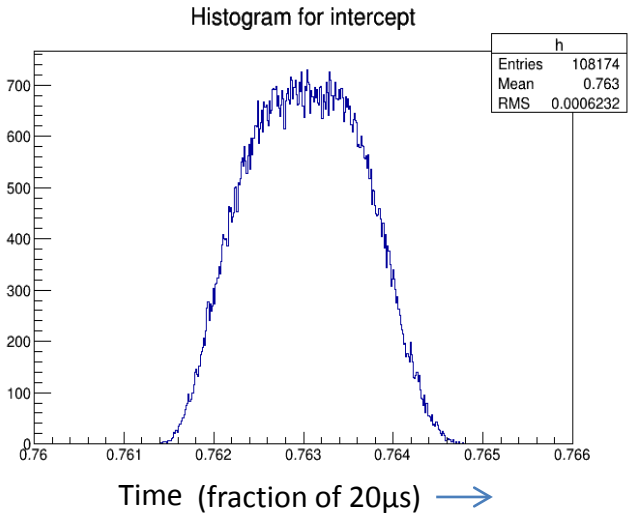

Fig: Histogram for intercepts

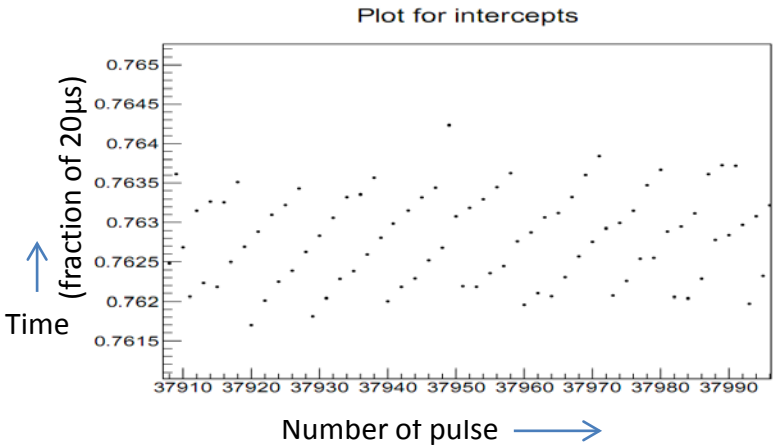

Fig: Zoomed plot for intercepts

The histogram shows that the jitter is of the order of 20 nano sec.

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Measurements : Averaging

- Suppose we have a pulse/signal like the following where all entries are effectively(close to) zero except one entry/point.

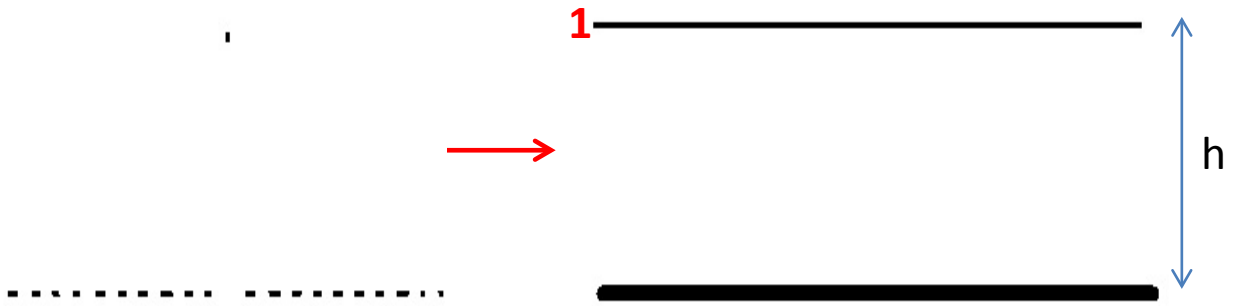


Fig: An Ideal case

- If we find the height without any averaging to be 'h' , then if you merge 'x' entries, the height of the upper line will be shifted to 'h/x' .

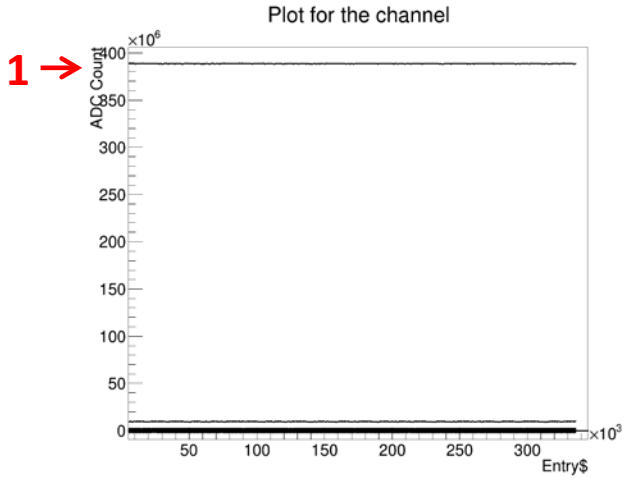


Fig: Signal with nacc=1,1

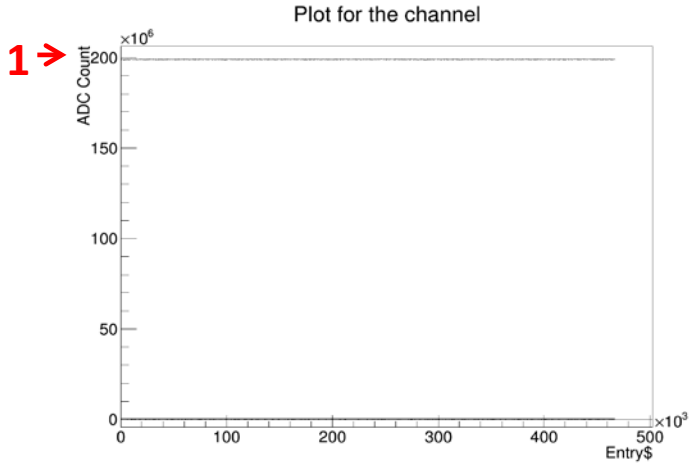


Fig: Signal with nacc=2,2

nacc=1,1 , Signal width= 10 µsec
Signal height= Line 1 height =~ 400 x 10^6 ADC count

With **nacc=2,2** the height becomes half of the height with nacc=1,1

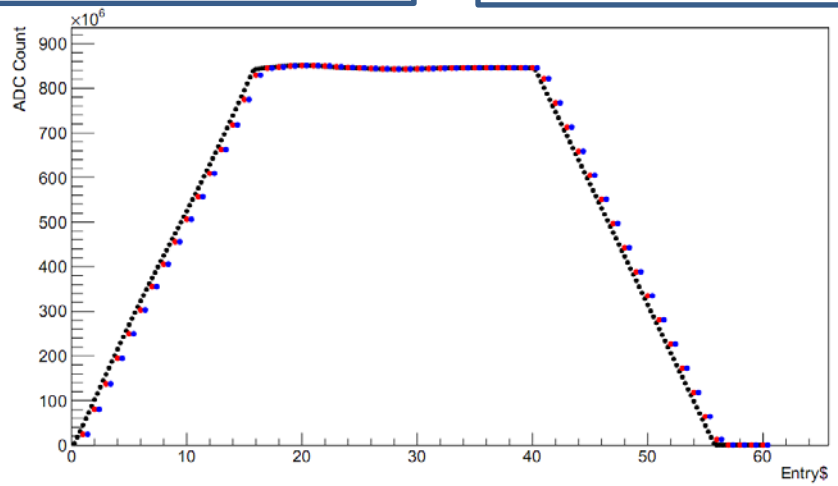
DAQ for n^3He

Measurements : Averaging

- Again in a separate analysis pulsed signal with ramp is recorded in resynchronized triggered mode.
- Then on a single canvas we compare the plot for
  1) The data set without averaging (nacc=1,1 data)
  2) The data set with merging four points (nacc=4,4 data)
  3) The data set obtained by taking average of four points from first data set/without merge (Interpolated data).

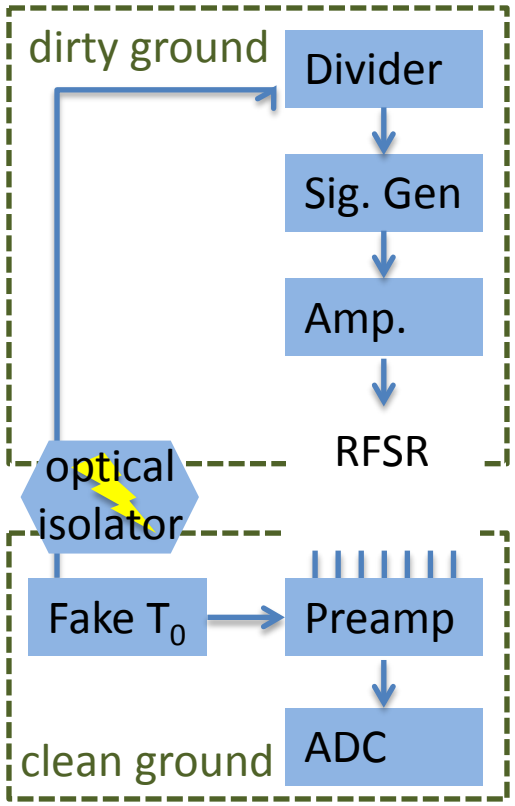
In black circle: nacc=1,1 data
In red circle: nacc =4,4 data
In blue circle : Interpolated data

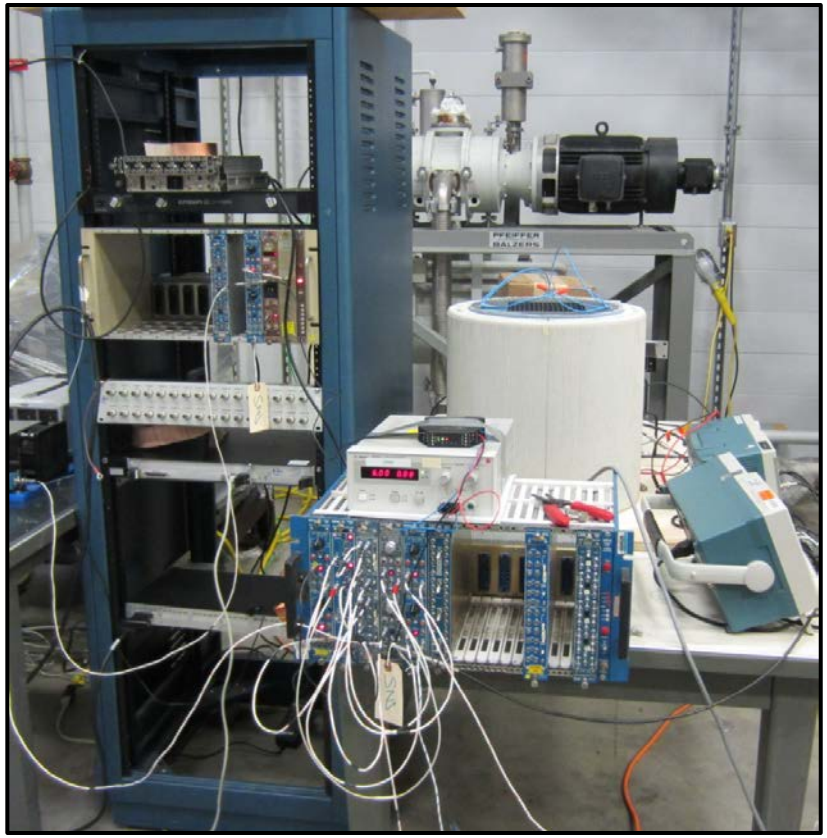
Note: A tiny X+(+0.4) offset for blue points has been added by hand so that we can see both blue and red.

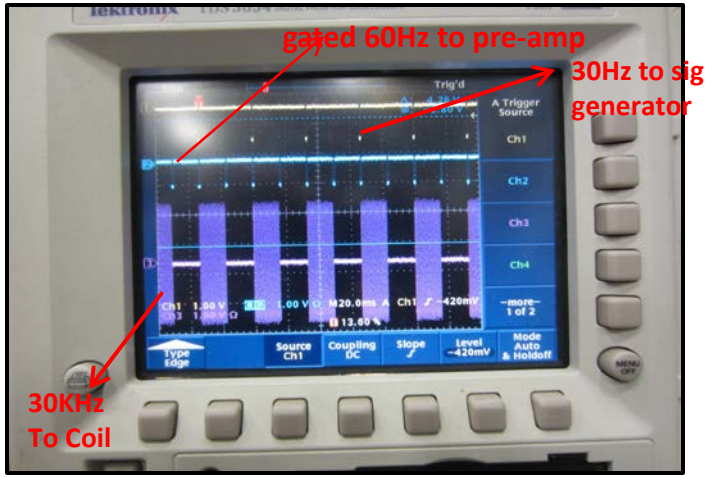


X axis Unit:
Blue points: 1 Entry$ = 1 x 1 Entry
Red Points: 1 Entry$ = 1 x 1 Entry
Black Points: 1 Entry$ = 4 x 1 Entry

Instrumental asymmetries with RFSF







Sources of false asymmetries:
- Ground loops
- Electrostatic couplings
- Power supply couplings
- Circuit to circuit couplings
- and many others …. …

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Instrumental asymmetries with RFSF

- Took equal number of entries between two T_0 pulses.
- Subtracted two adjacent (ON/OFF)states then normalized by the full scale of the ADC(20 Volts)

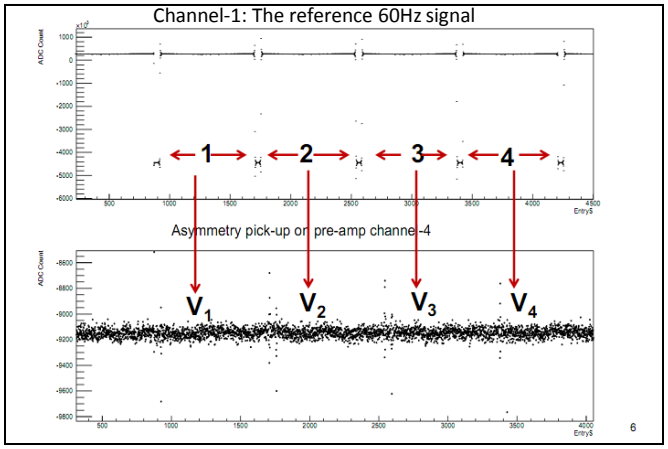
$$A_1=(V_1-V_2)/20$$

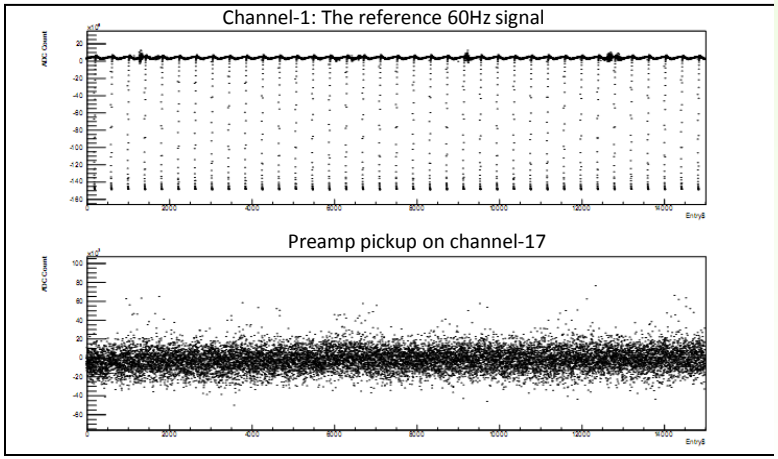
$$A_2=(V_3-V_4)/20 \ \ldots.\text{etc.}$$

$$\text{Asymmetry, } A=(A_1+A_2+A_3+\ldots\ldots+A_N)/N$$

- To calculate uncertainty in false asymmetry, made a histogram for asymmetry of individual pair, A_K, k-1,2,….N
- Calculated width σ (sigma or RMS) of the histogram. Then,

$$\Delta A = \sigma / \sqrt{N}$$





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Instrumental asymmetries with RFSF

- Analysis of 5 hour of data at 25KHz shows that-

Asymmetry = 2.64 x 10^{-10} ± 1.64 x 10^{-10}

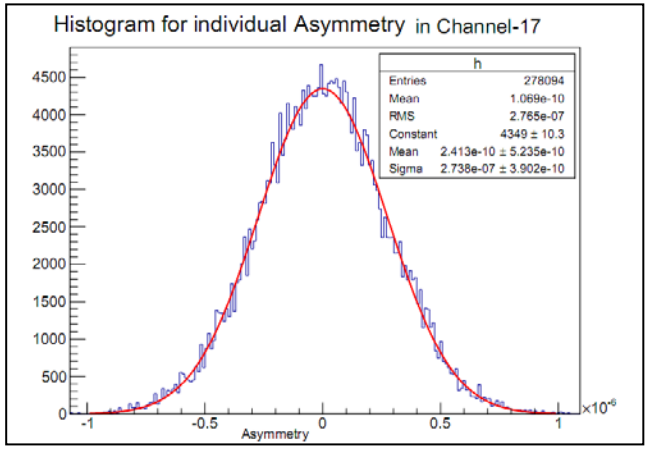

Fig: Typical histogram for asymmetry for a channel

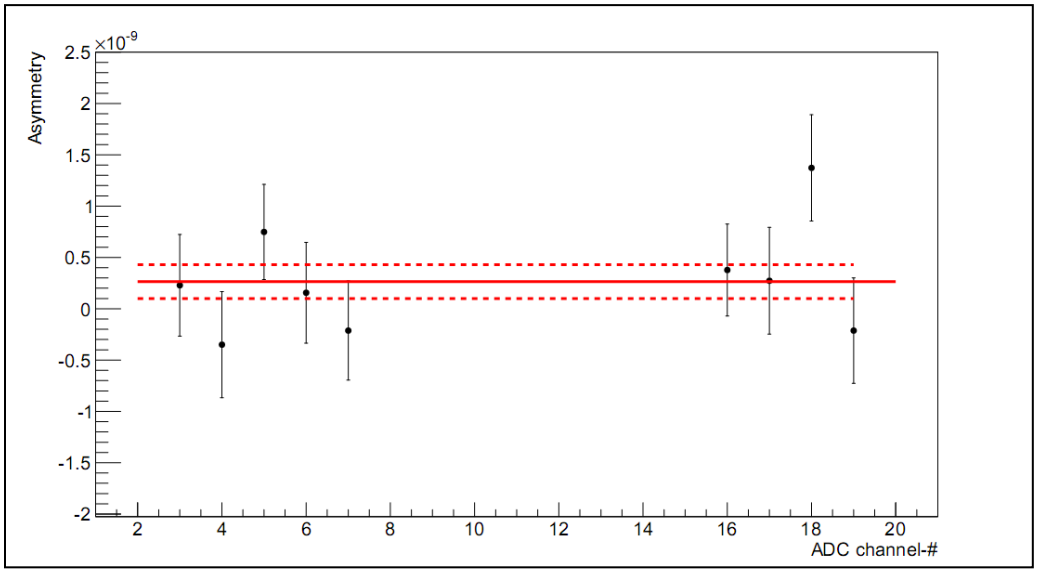

Fig: Instrumental asymmetry for different ADC channels

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Conclusion :

- We have a DAQ system which fulfills all of our expectations and gives instrumental asymmetry as small as $(2.64\pm1.64)\times10^{-10}$ Thus we achieved our goal.

Future Plan :

- Measure the instrumental asymmetry with the whole system.
- Data taking starts in one month.
- Analysis of the data.

n-^{3}He Collaboration

Institution	Researcher	Category	2014 Effort
Duke University, Triangle Universities Nuclear Laboratory			
	Pil-Neo Seo	Research Staff	10
Istituto Nazionale di Fisica Nucleare, Sezione di Pisa			
	Michele Viviani	Research Staff	15
Oak Ridge National Laboratory			
	Seppo Pentillä	Research Staff	70
	David Bowman	Research Staff	70
	Vince Cianciolo	Research Staff	10
University of Kentucky			
	Chris Crawford	Faculty	50
	Kabir Latiful	Grad Student	100
Western Kentucky University			
	Ivan Novikov	Faculty	70
	TBD	Undergraduate	100
University of Manitoba			
	Michael Gericke	Faculty	30
	V. Tvaskis	Postdoc	10
	Mark McCrea	Grad Student	100
	Carlos Olguin	Grad Student	100
Universidad Nacional Autónoma de México			
	Libertad Baron	Faculty	50
	Andrés Naranjas	Grad Student	100
University of New Hampshire			
	John Calarco	Faculty	50
University of South Carolina			
	Vladimir Gudkov	Faculty	5
	Young-Ho Song	Postdoc	5
Univeristy of Tennessee			
	Geoff Greene	Faculty	30
	Nadia Fomin	Faculty	30
	Irakli Garribaldi	Postdoc	50
	Chris Hayes	Grad Student	100
	Chris Coppola	Grad stduent	100
Univeristy of Tennessee at Chattanooga			
	Josh Hamblen	Faculty	75
	Caleb Wickersham	Undergraduate	100
University of Virginia			
	S. Baessler	Faculty	20

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Backup Slides

Autocorrelation Plots for ACQ164 ADC Noise

1.Formalism Followed:

Autocorrelation plots are formed by

- **Vertical axis: Autocorrelation coefficient**

$$R_h = C_h / C_0$$

where C_h is the autocovariance function

$$C_h = \frac{1}{N} \sum_{t=1}^{N-h} (Y_t - \bar{Y})(Y_{t+h} - \bar{Y})$$

and C_0 is the variance function

$$C_0 = \frac{\sum_{t=1}^{N} (Y_t - \bar{Y})^2}{N}$$

Note that R_h is between -1 and +1.

- **Horizontal axis: Time lag h (h = 1, 2, 3, ...)**

2. In the data set there were few (3 or 4) values which were completely out of any scale (10^9 times out of scale), those ADC values were replaced by hand by the average of previous and next ADC value.

3. X-axis unit: 1 lag= 100 micro second(for 10Khz) or 20 micro second (for 50KHz), Y-axis unit: Unitless

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The n-^{3}He experiment
- -Motivation
- -Experimental Setup

DAQ for n-^{3}He
- -Expectations
- -ADC modules
- -A Complete Network

Measurements
- -ADC noise and rise time
- -Resynchronization and Jitter
- -Averaging
- -Instrumental Asymmetry

Future Plan

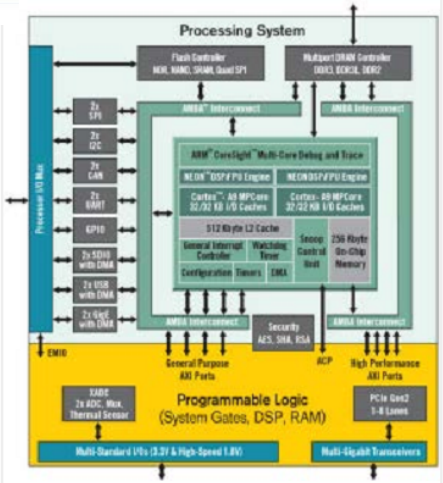
Zynq-7000 All Programmable SoC

Based on the Xilinx All programmable SoC architecture, the Zynq®-7000 All Programmable SoCs enable extensive system level differentiation, integration, and flexibility through hardware, software, and I/O programmability.

Using the Zynq-7000 platform, you can design smarter systems with tightly coupled software based control and analytics with real time hardware-based processing and optimized system interfaces — with vastly lower BOM costs, lower NRE costs, lower design risk, and of course much faster time to market. All six Zynq devices (Z-7010, Z-7015, Z-7020, Z-7030, Z-7045, Z-7100) are optimized for specific combinations of system power, cost, and size to meet the needs of smarter control, smarter vision and smarter networks.

This comprehensive Platform offers:

- Silicon Devices - Zynq-7000 Full-Featured Processing Platform
- Development Platforms - Traditional hardware development and virtual development platforms
- Operating Systems - Open Source Linux, Android, FreeRTOS
- Design Tools - Vivado® Design Suite, Xilinx SDK, PetaLinux SDK
- IP - Plug and Play



Click to expand

Smartest Solution for a Wide Range of System Design Problems

Xilinx Zynq-7000 All Programmable SoCs are the Smartest Solution for a wide range of system-design problems in all markets, across the entire application spectrum. Learn more about the 9 reasons why:

Enabling Smarter Systems	• Most efficient ARM + FPGA for analytics & control • Extensive OS, middleware & stack ecosystem • Highest level of security & reliability Learn More >
Unmatched Performance and Power	• Highest Performance SoC • Largest & Highest Performance Memory System • Lowest Power and Fastest Logic Fabric Learn More >
Proven Productivity	• Industry-leading high-level synthesis • Widest selection of software environments and tools • Largest portfolio of IP, design kits, and reference designs Learn More >

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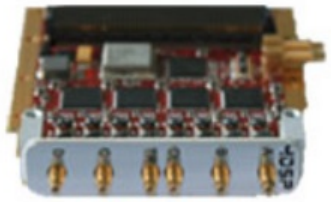
Recently, there has emerged a greater need for different front panel IO functionality within systems. Typically, this front panel IO functionality was fixed on 3U or 6U form factor cards, or it was configured with PMC or XMC modules. Previously, 3U and 6U form factor card design used a fixed front panel IO, which addressed a particular function. Changing the front panel IO functionality meant replacing the 3U or 6U cards. PMC and XMC modules provided configurable front panel IO for 3U and 6U form factor cards. However, PMC and XMC modules use much of the 3U and 6U carrier card area.


Xilinx: FMC-SM


4DSP: FMC104


Alpha Data: ADPE-XRC-5T


Faster Technology: FM-S18

FPGA Mezzanine Card, or FMC, as defined in VITA 57, provides a specification describing an I/O mezzanine module with connection to an FPGA or other device with reconfigurable I/O capability. The low profile design allows use on popular industry standard slot card, blade and motherboard form factors, including VME, VPX, CompactPCI, AdvancedTCA, MicroTCA, PCI, PXI, and many other low profile motherboards. The compact size is highly adaptable to many configuration needs and compliments existing common low profile mezzanine technology such as PMC, XMC, and AMC.

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