2013-12-04 DAQ phc.

Wednesday, December 4, 2013
8:12 AM

* Nadia got computer, setting up.

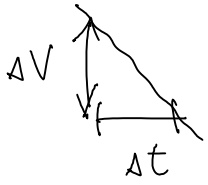
* ISR/OSR
  + tried and didn't understand it.

* Irakli – need stable machine

* Nadia – take data @ 100 kHz
  → nsamples 6MB ~ 2500 × 64 ch.

* Vince:
  10 MHz 1 bit
  2.5 kHz to disk ↘ average over 128 kHz, 8 kHz, 52 kHz.

  + if chip was boxcar average then no difference



  + if ADC chip better, then 8 kHz.

  • jitter due to timing: sample clock (10MHz) or ISR (8-128 kHz)

  + jitter of T_ϕ signal?

    trigger of mains → absolute clock.

proton pulse has jitter

RMS 700μs proton width.

- 10 MHz – 100 ns overkill

8μs – good enough?

125μs – not good enough?

* David: repeated gating.

16.4 ms wide gate, triggered by generator
gates through delay system
oscilloscope to align phase
measurements happened at different phase

start continuous, store all events w/ trigger

+ manual clearly out of date

+ TBlocks: 6.4MB 25k samp * 32 bit * 64 ch.
associated with triggers / events?

if stop befor TBlock full
put blocks still copies full data.

+ Put blocks
use "expect" → curl?

built on tcl.

+ distribution: busy box. – for embedded

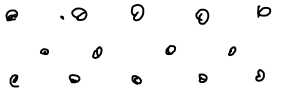
* Vince:

simplest way to go:
run in continuous mode
link sample clock to TØ

divided down from 10 MHz.

clock counter: TØ → start counter
derive sample clock from counter.

that firmware start on TØ clock edge.

* 

9 x 4 x 4 preamps
wires layers

435

2006

5 x 40
3 x 60

32+8

delay:

* respin: Jan could put board
manufacture: Feb, Mar →
deliver: April 2nd.

8wks: if new spin, loan motherboards.

quote: 5 boxes same, 3-boxes lower

6 sites, only populating 4 sites.

144 ch. in one box?