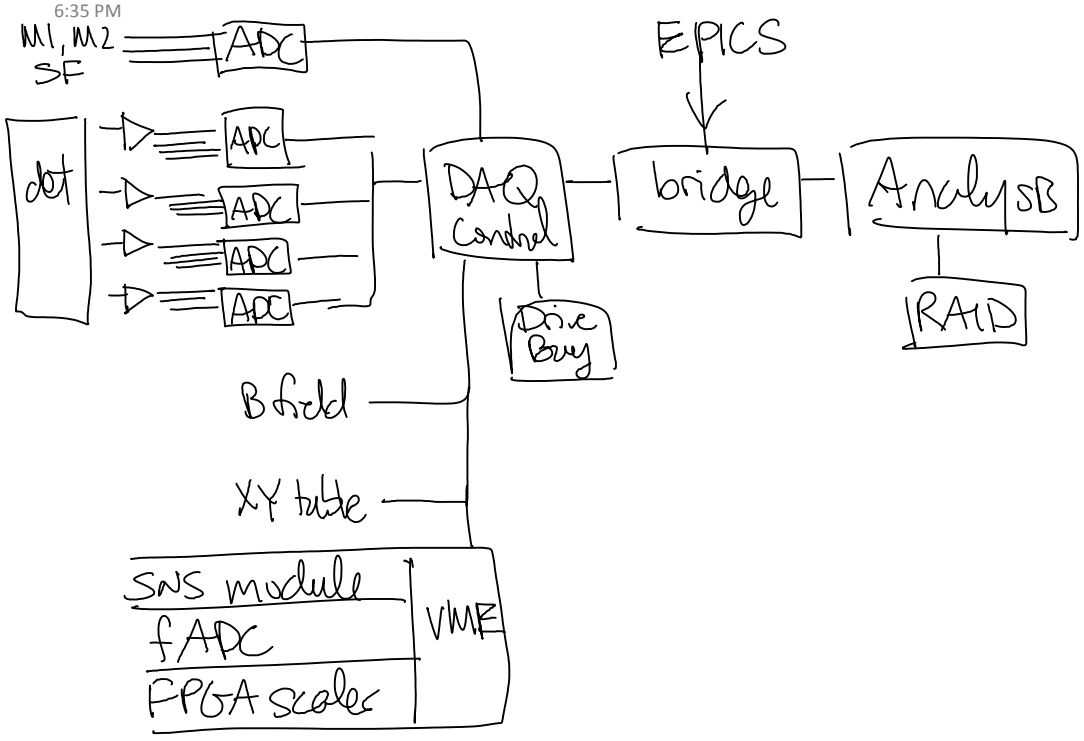
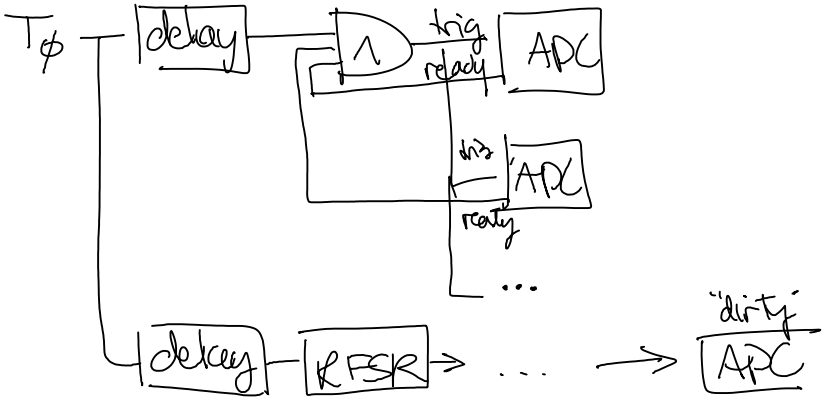
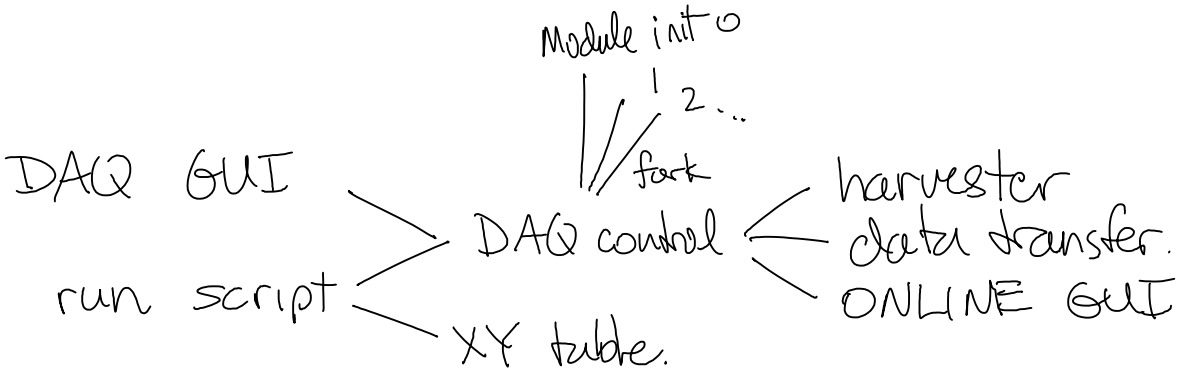
DAQ schematic

Thursday, November 7, 2013
6:35 PM







- one data file / run for each module.

- conglomerated into single TTreeRaw.
- slow DAQ stored à la Chael. (continuous running)
  - coordinated with fast runs in TBranch by timestamp

1) DAQ → Module init → starts DAQ, wait for trigger.
2) Module waits for T_ϕ buffers data, FTPs back
3) Harvester combines fragments. ↳ including header.

Timing

ΔΣ: 10 MHz
ADCout: 8 - 128 kSPS 52 kSPS high resolution.
boxcar: 1 - 32 sums.
CPU: n sums