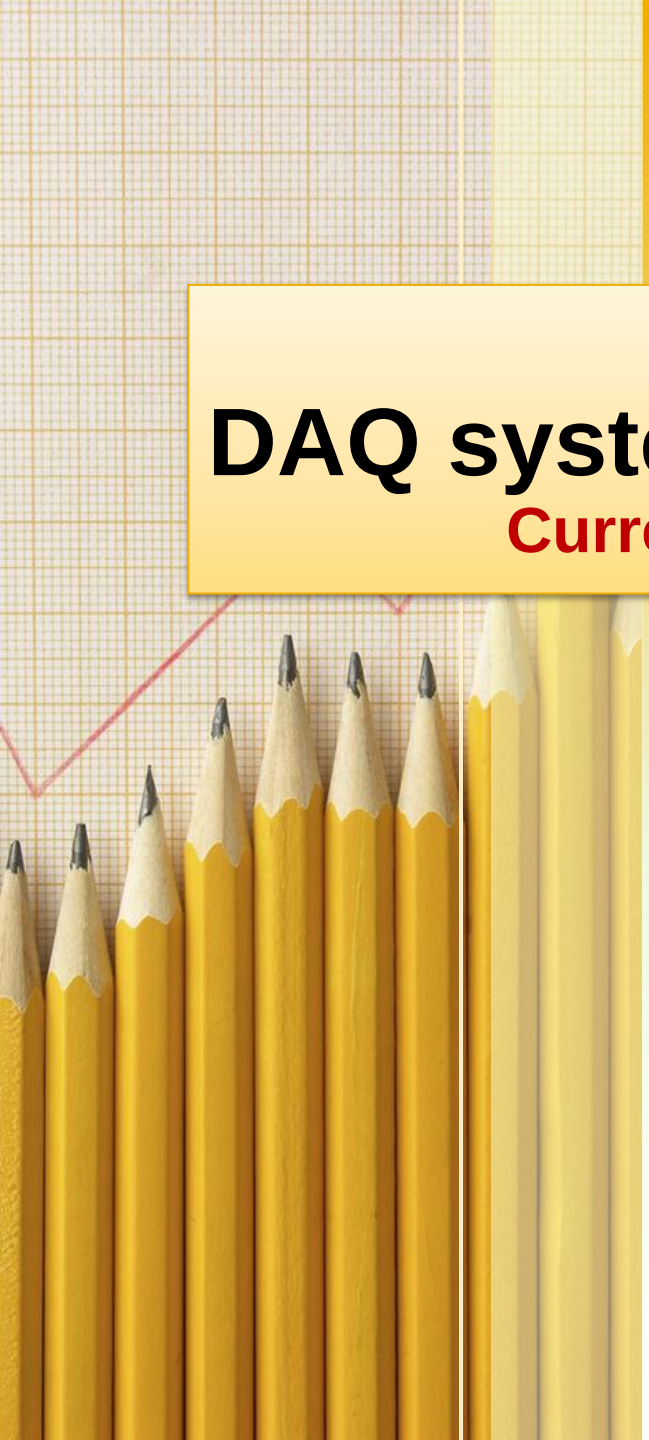
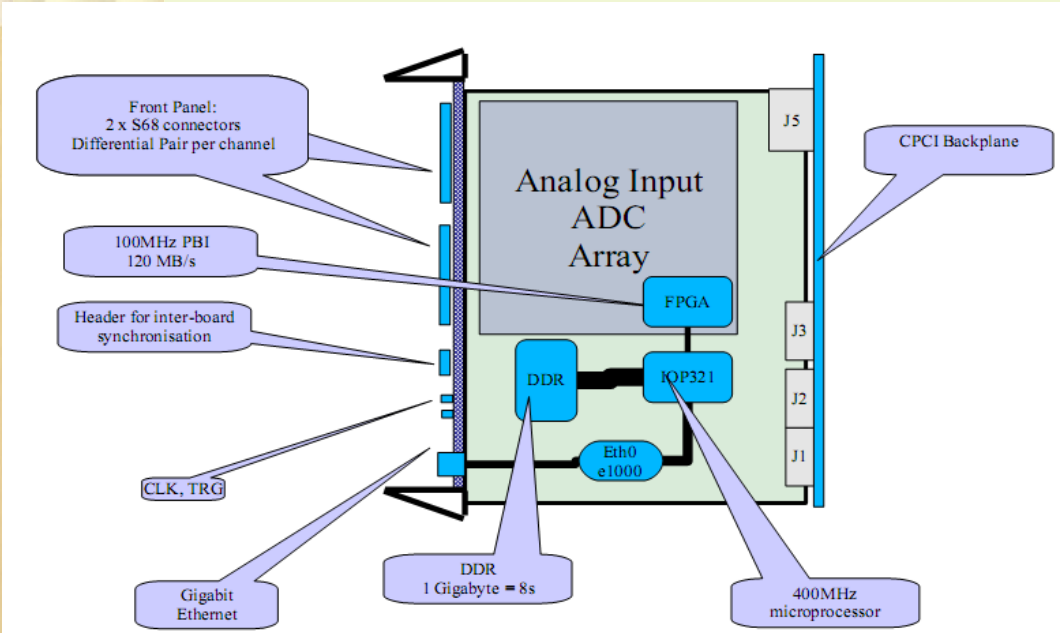


DAQ system for n3He Experiment

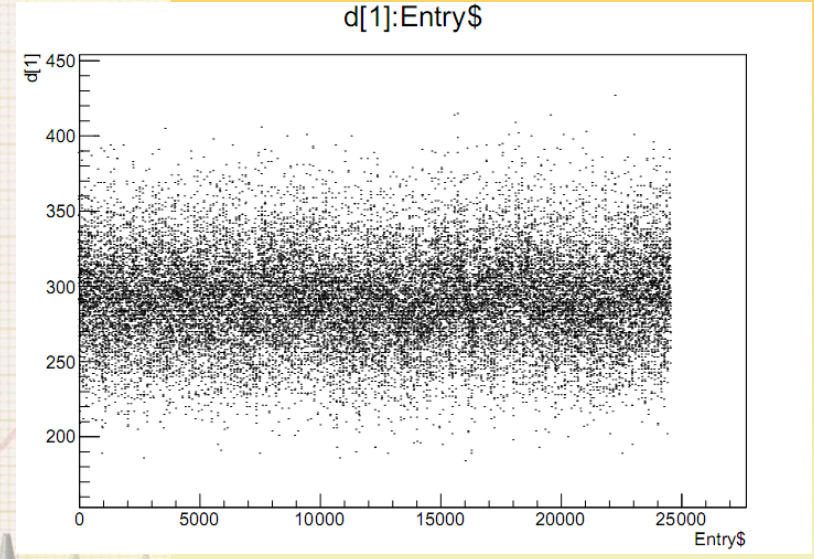
Current Status and Future Plan

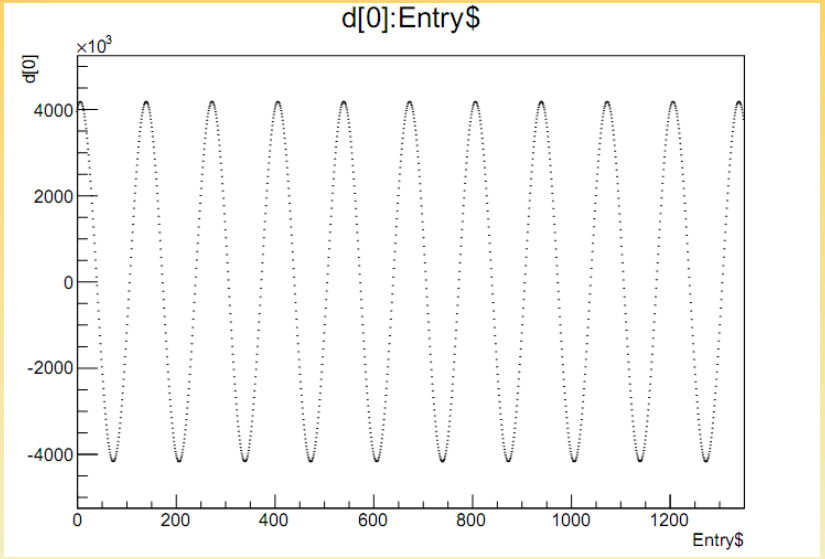
Overview

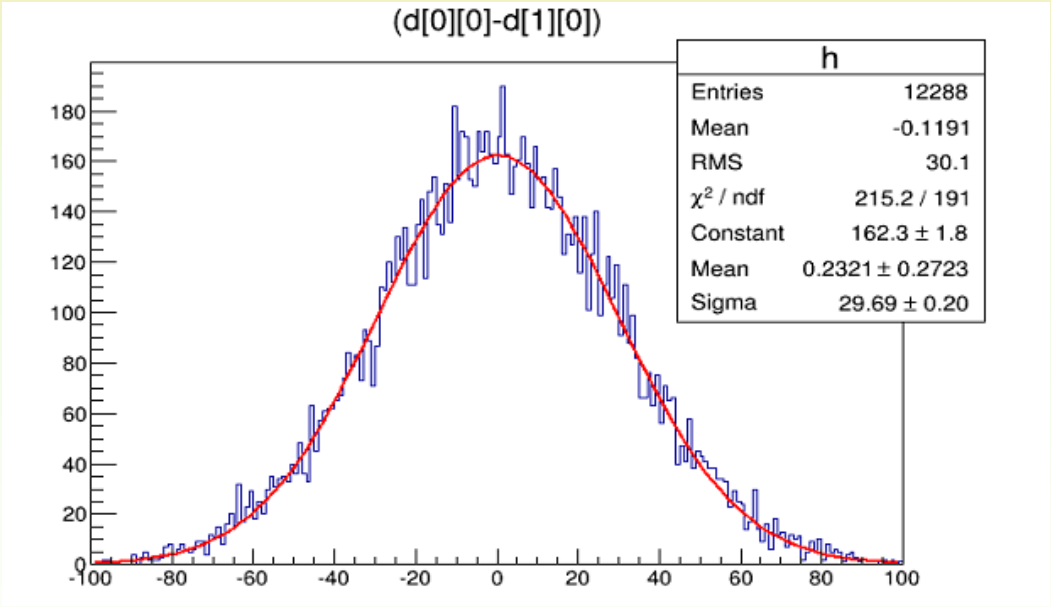
- Delta sigma technology based ADC (ACQ164) by
- 24 bit ADC per channel for true simultaneous analog input.
- Maximum sampling rate 128 kSPS (minimum is 8 kSPS) per channel.
- 64 Channels
- Signal to noise ratio is 104 dB (high speed) or 108 dB (high
- resolution)
- **1GB** DDR memory on board
- External clock, trigger, internal clock.



Accomplished

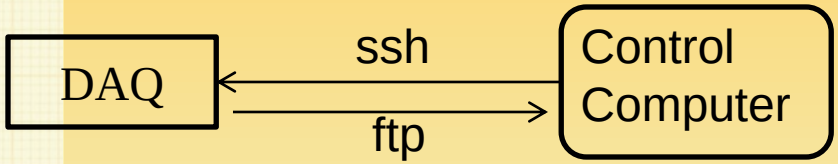


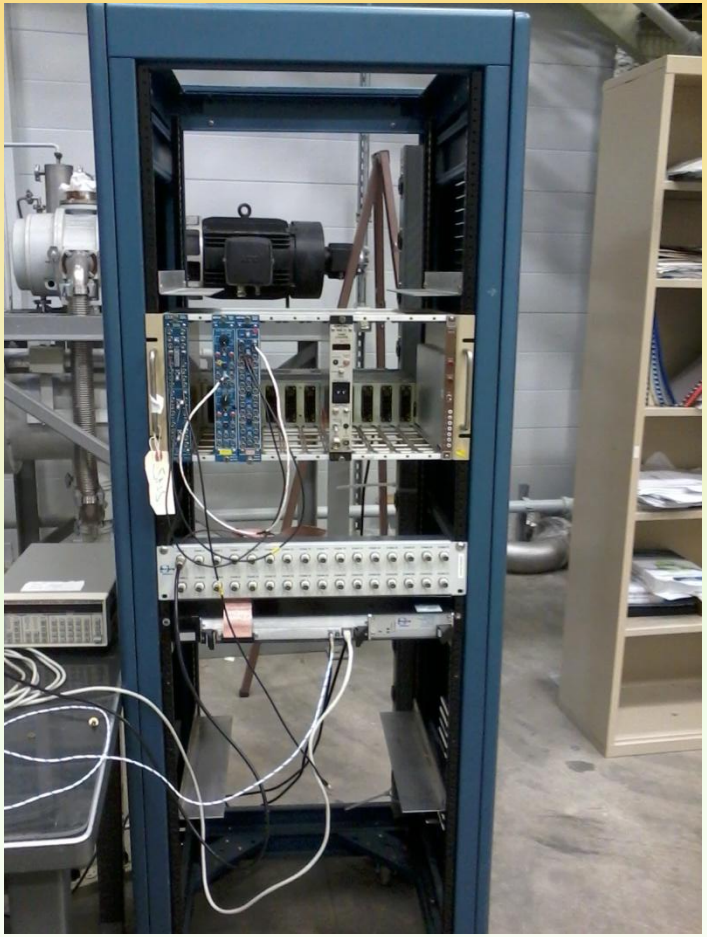




$\delta A \sim 10^{-10}$ (with in couple of hours data taking)

Currently Working On

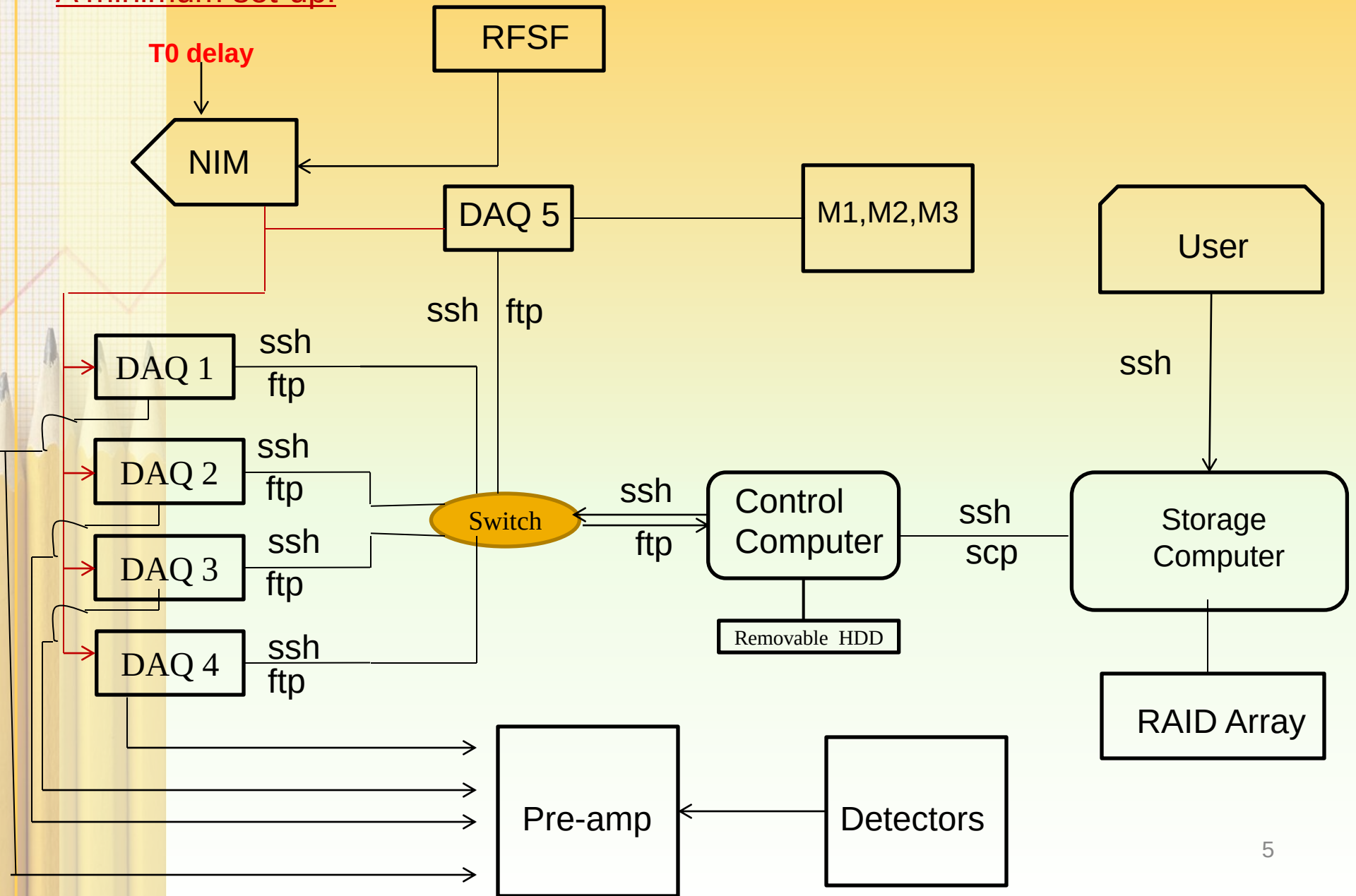




- We made starting and stopping data taking process simple.
- Now working on triggering/clock & test NIM modules.
- Soon we want to mock-up pre-amp and RFSF for background noise.

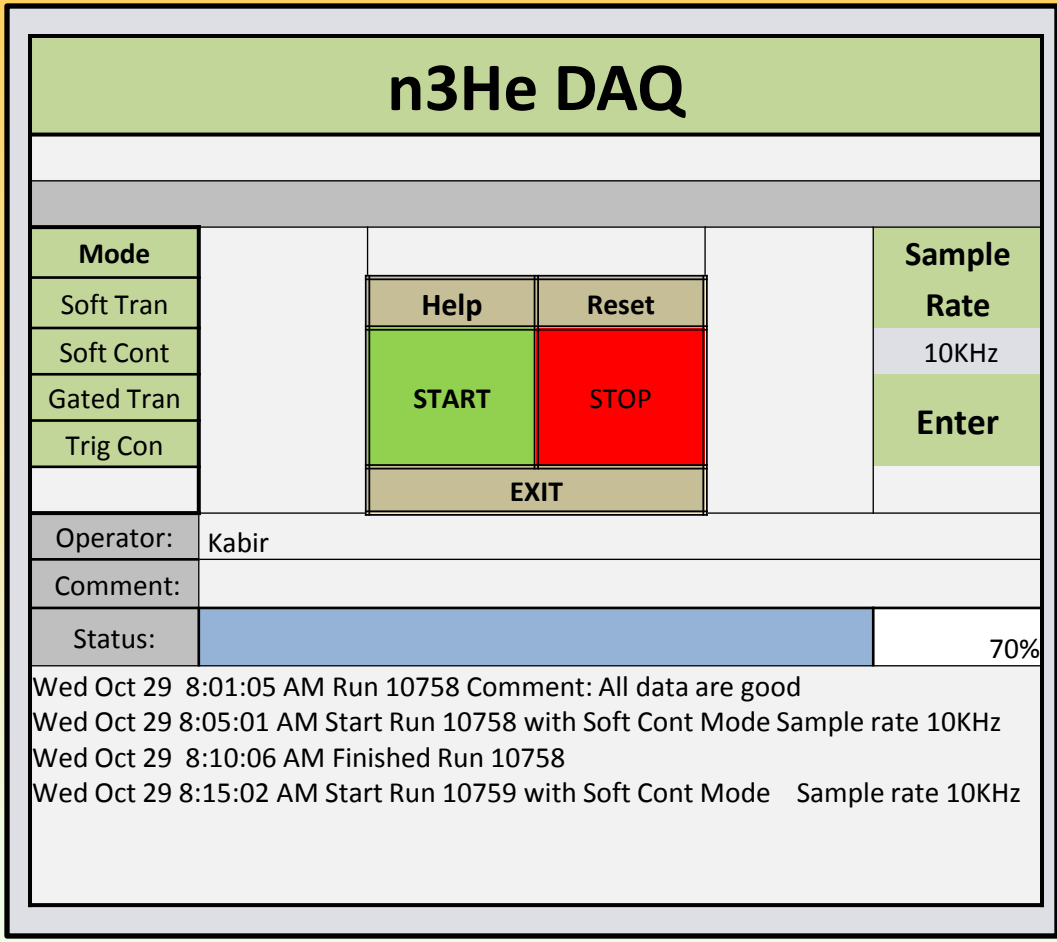
Future Plan

A minimum set-up:



Data acquisition

1. DAQ Control
2. Electronic logbook
3. Run database
4. Programs on ADC module
5. Copy all the chunks to a big file.



Analysis

1. ROOT TBranchBinary trees
2. Run set management
3. WebOOT for data availability (histogram generator)
4. Online analysis

Other Scripts:

1. File renaming and copying
2. Script to operate XY-table
3. Out-of-bounds alarms

Issues need to be settled

- What ADC sample rate to be used ?
- What will be the number of pulses per sequence ?
- Are we going to use special spin sequence ?
- How many entries will be used per run ?
- How many computers are preferred for DAQ set-up ? We urgently need at least one.

Appendix: Specifications

Analog Input Performance (Typical)

	High Speed	*High Resolution*
Number Of Channels	64/32	
Sample Rate	128 kSPS/channel	52 kSPS/channel
Resolution	24 bits	
Coupling	DC, Differential Input	
Sampling	Simultaneous	
Input Impedance	20kΩ common mode, 1 MΩ to 0V	
Voltage Range	±10V default ±5V, ±2.5V (factory fit options)	
Common Mode Range	±13V	
Input Voltage Withstand	±30V	
Offset Error	DAC Offset trim to 0.01% FS [2]	
Gain Error	Numerical adjust to 0.01% FS [3]	
INL	±0.002% FS	
CMRR	>60dB FS @ 1 kHz	
THD	-106 dB [1]	
SFDR	107 dBc [1]	
SNR	104 dB [1]	108 dB [1]
Analog Input BW (-3dB)	80 kHz	
Digital Filter Characteristics	Pass Band = 0.453 FSAMPLE -3dB = 0.49 FSAMPLE Stop Band = 0.547 FSAMPLE Stop Band Attenuation = 95dB	
Crosstalk (3 dB)	<90 dB @ 1 kHz FS Input	
Digital I/O		
External Clock, Trigger Signals	Front Panel Lemos - 2 lines Backplane PXI - 6 lines	
External Clock Input Rate	Minimum Clock Input = 600kHz Maximum Clock Input = 20 MHz [4]	
Switching Characteristics	TTL - Opto-Coupled	
Sample Clock Rate	Derived from internal or external clock source, clock multiplier is programmable, output rate controllable in 8Hz steps.	
High Time for Trigger	100 nS min	
Low Time for Trigger	100 nS min	